DataSheet

AS1152
Quad LVDS Driver

1 General Description

The AS1152 is a Quad Flow-Through LVDS (Low-Voltage Differential Signaling) Line Driver which accepts and converts LVTTL/LVCMOS input levels into LVDS output signals. The device is perfect for low-power low-noise applications requiring high signaling rates and reduced EMI emissions.

The device is guaranteed to transmit data at speeds up to 500Mbps (250MHz) over controlled impedance media of approximately 100Ω. Supported transmission media are PCB traces, backplanes, and cables.

The AS1152 is capable of setting all four outputs to a high-impedance state through two Enable Inputs (EN and ENn – internally pulled down to GND), dropping the device to an ultra-low-power state of 16mW (typical) during high impedance. The Enable Inputs are common to all four drivers.

Outputs conform to the *ANSI TIA/EIA-644 LVDS* standards. Flow-through pinout simplifies PC board layout and reduces crosstalk by separating the LVTTL/LVCMOS inputs and LVDS outputs.

The AS1152 operates from a single +3.3V supply and is specified for operation from -40 to +85°C.

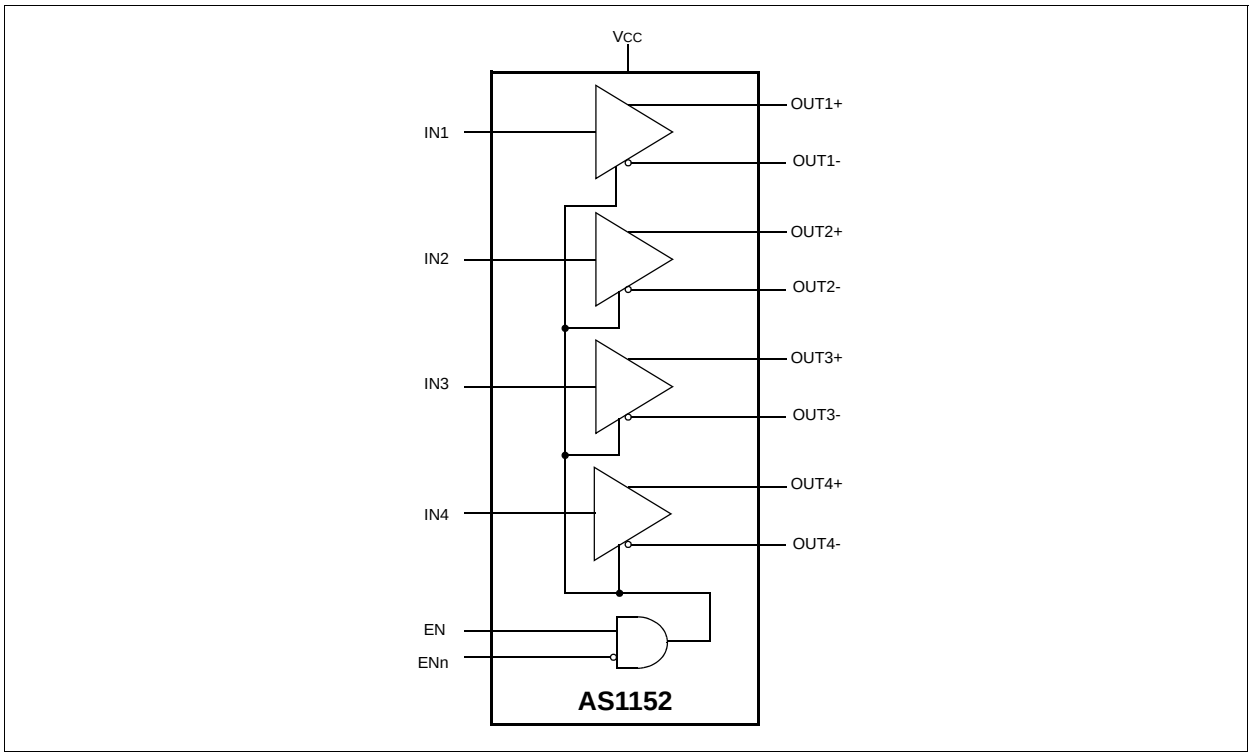
2 Key Features

- Flow-Through Pinout
- Guaranteed 500Mbps Data Rate (paired with AS1150)
- 350ps Pulse Skew (Max)
- Conforms to *ANSI TIA/EIA-644* LVDS Standards
- Single +3.3V Supply
- Operating Temperature Range: -40 to +85°C
- 16-Pin TSSOP Package

3 Applications

Digital Copiers, Laser Printers, Cellular Phone Base Stations, Add/Drop Muxes, Digital Cross-Connects, DSLAMs, Network Switches/Routers, Backplane Interconnect, Clock Distribution Computers, Intelligent Instruments, Controllers, Critical Microprocessors and Microcontrollers, Power Monitoring, and Portable/Battery-Powered Equipment.

Figure 1. Block Diagram



4 Absolute Maximum Ratings

Stresses beyond those listed in Table 1 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 1. Absolute Maximum Ratings

Parameter	Limits	Units	Notes
V_{CC} to GND	-0.3 to +5.0	V	
IN*x*, EN, ENn to GND	-0.3 to (V_{CC} + 0.3)	V	
OUT*x*+, OUT*x*- to GND	-0.3 to +5	V	
Short Circuit Duration (OUT*x*+, OUT*x*-)	Continuous		
Continuous Power Dissipation (T_A = +70°C)	755	mW	Derate 9.4mW/°C Above +70°C
Storage Temperature Range	-65 to +150	ºC	
Maximum Junction Temperature	+150	ºC	
Operating Temperature Range	-40 to +85	ºC	
Package Body Temperature	260	ºC	The reflow peak soldering temperature (body temperature) specified is in compliance with *IPC/ JEDEC J-STD-020C "Moisture/ Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices"*.
ESD Protection	±4	kV	Human Body Model, IN*x*, OUT*x*+, OUT*x*--

5 Electrical Characteristics

DC Electrical Characteristics

(V_{CC} = +3.0 to +3.6V, T_A = -40 to +85°C , R_L = 100Ω, f ≤ 150Mhz
Typical values are at V_{CC} = +3.3V, T_A = +25°C, Unless Otherwise Noted.)[1, 2]

Table 2. DC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LVDS Output (OUTx+, OUTx-)						
Differential Output Voltage	V_{OD}	Figure 20 on page 12	250	370	450	mV
Change in Magnitude of V_{OD} Between Complementary Output States	ΔV_{OD}	Figure 20 on page 12		1	35	mV
Offset Voltage	V_{OS}	Figure 20 on page 12	1.125	1.25	1.375	V
Change in Magnitude of V_{OS} Between Complementary Output States	ΔV_{OS}	Figure 20 on page 12		4	25	mV
Output High Voltage	V_{OH}				1.6	V
Output Low Voltage	V_{OL}		0.90			V
Differential Output Short-Circuit Current [3]	I_{OSD}	Enabled, V_{OD} = 0			-9	mA
Output Short-Circuit Current	I_{OS}	OUTx+ = 0 at INx = V_{CC} or OUTx- = 0 at INx = 0, enabled		-3.8	-9	mA
Output High-Impedance Current	I_{OZ}	EN = low and ENn = high, OUTx+ = 0 or V_{CC}, OUTx- = 0 or V_{CC}, R_L = ∞	-10		10	µA
Power-Off Output Current	I_{OFF}	V_{CC} = 0 or open, OUTx+ = 0 or 3.6V, OUTx- = 0 or 3.6V, R_L = ∞	-20		20	µA
Inputs (INx, EN, ENn)						
High-Level Input Voltage	V_{IH}		2.0		V_{CC}	V
Low-Level Input Voltage	V_{IL}		GND		0.8	V
Input Current	I_{IN}	INx, EN, ENn = 0 or V_{CC}	-20		20	µA
Supply Current						
No-Load Supply Current	I_{CC}	R_L = ∞ , INx = V_{CC} or 0 for all channels		4	6	mA
Loaded Supply Current	I_{CCL}	R_L = 100Ω, INx = V_{CC} or 0 for all channels		18	25	mA
Disabled Supply Current	I_{CCZ}	Disabled, INx = V_{CC} or 0 for all channels, EN = 0, ENn = V_{CC}		3.5	5.5	mA

Notes:

1. Maximum and minimum limits over temperature are guaranteed by design and characterization. Devices are 100% tested at T_A = +25°C.
2. Currents into the device are positive, and current out of the device is negative. All voltages are referenced to ground except V_{OD}.
3. Guaranteed by correlation data.

Switching Characteristics

(V_{CC} = +3.0 to +3.6V, R_L = 100Ω ±1%, f ≤ 150MHz, T_A = -40 to +85°C
Typical values are at V_{CC} = +3.3V, T_A = +25ºC, Unless Otherwise Noted.) [1, 2, 3]

Table 3. Switching Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Differential Propagation Delay, High-to-Low	t_{PHLD}	Figure 18 on page 11 and Figure 19 on page 11	1.1		1.7	ns
Differential Propagation Delay, Low-to-High	t_{PLHD}	Figure 18 on page 11 and Figure 19 on page 11	1.1		1.7	ns
Differential Pulse Skew [4]	t_{SKD1}	Figure 18 on page 11 and Figure 19 on page 11		0.04	0.35	ns
Differential Channel-to-Channel Skew [5]	t_{SKD2}	Figure 18 on page 11 and Figure 19 on page 11		0.07	0.60	ns
Differential Part-to-Part Skew [6]	t_{SKD3}	Figure 18 on page 11 and Figure 19 on page 11		0.13	0.8	ns
Differential Part-to-Part Skew [7]	t_{SKD4}	Figure 18 on page 11 and Figure 19 on page 11		0.43	1.0	ns
Rise Time	t_{TLH}	Figure 18 on page 11 and Figure 19 on page 11	0.2	0.39	2.6	ns
Fall Time	t_{THL}	Figure 18 on page 11 and Figure 19 on page 11	0.2	0.39	2.6	ns
Disable Time, High-to-Z	t_{PHZ}	Figure 21 on page 12 and Figure 22 on page 12		3	4	ns
Disable Time, Low-to-Z	t_{PLZ}	Figure 21 on page 12 and Figure 22 on page 12		3	4	ns
Enable Time, Z-to-High	t_{PZH}	Figure 21 on page 12 and Figure 22 on page 12		2	3	ns
Enable Time, Z-to-Low	t_{PZL}	Figure 21 on page 12 and Figure 22 on page 12		2	3	ns
Maximum Operating Frequency [8, 9]	f_{MAX}		250			MHz

Notes:

1. Parameters are guaranteed by design and characterization.
2. C_L includes probe and jig capacitance.
3. Signal generator conditions for dynamic tests: V_{OL} = 0, V_{OH} = 3V, f = 100MHz, 50% duty cycle, RO = 50Ω, t_R ≤ 1ns, t_F ≤ 1ns (0 to 100%).
4. t_{SKD1} is the magnitude difference of differential propagation delay. $t_{SKD1} = |t_{PHLD} - t_{PLHD}|$.
5. t_{SKD2} is the magnitude difference of t_{PHLD} or t_{PLHD} of one channel to the t_{PHLD} or t_{PLHD} of another channel on the same device.
6. t_{SKD3} is the magnitude difference of any differential propagation delays between devices at the same V_{CC} and within 5°C of each other.
7. t_{SKD4} is the magnitude difference of any differential propagation delays between devices operating over the rated supply and temperature ranges.
8. f_{MAX} signal generator conditions: V_{OL} = 0, V_{OH} = 3V, 50% duty cycle, RO = 50Ω, t_R ≤ 1ns, t_F ≤ 1ns (0 to 100%).
9. Conforms to ANSI TIA/EIA 644 LVDS Standards ≤150MHz. Maximum operating frequency of 250MHz is possible using an AS1150 receiver.

6 Typical Operating Characteristics

V_{CC} = *+3.3V,* V_{CM} = *+1.2V,* $|V_{ID}|$ = *0.2V,* C_{LOAD} = *15pF,* Tamb = *+25ºC, unless otherwise noted*

Figure 2. Output High Voltage vs. V_{CC}

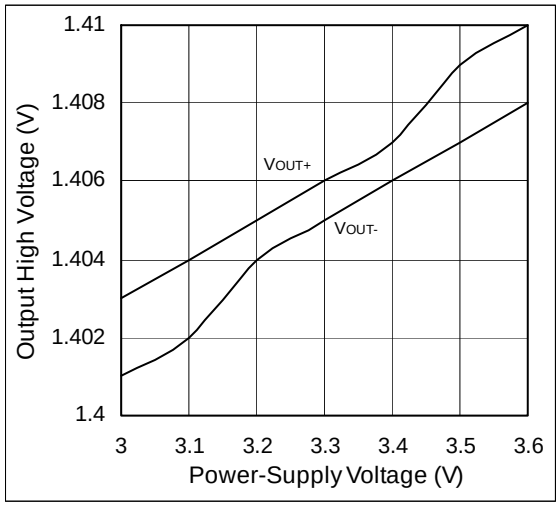


Figure 3. Output Low Voltage vs. V_{CC}

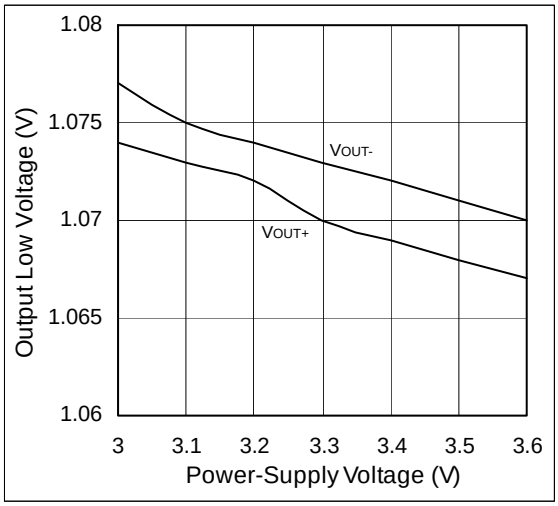


Figure 4. Output Short-Circuit Current vs. V_{CC}; V_{IN} = V_{CC} or GND

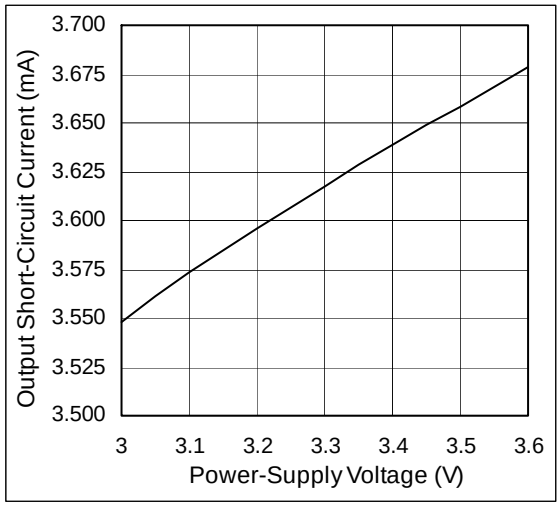


Figure 5. Output High-Impedance State Current vs. V_{CC}; V_{IN} = V_{CC} or GND

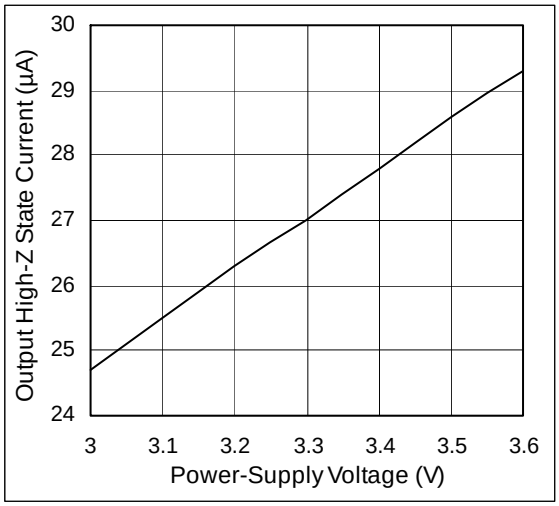


Figure 6. Differential Output Voltage vs. V_{CC}

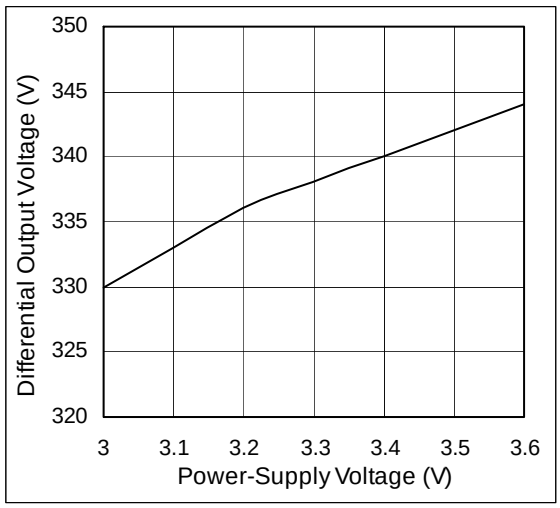


Figure 7. Differential Output Voltage vs. Load Resistor

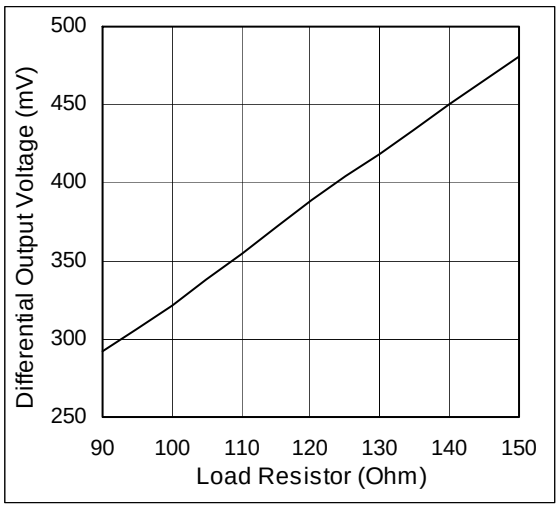


Figure 8. Offset Voltage vs. VCC

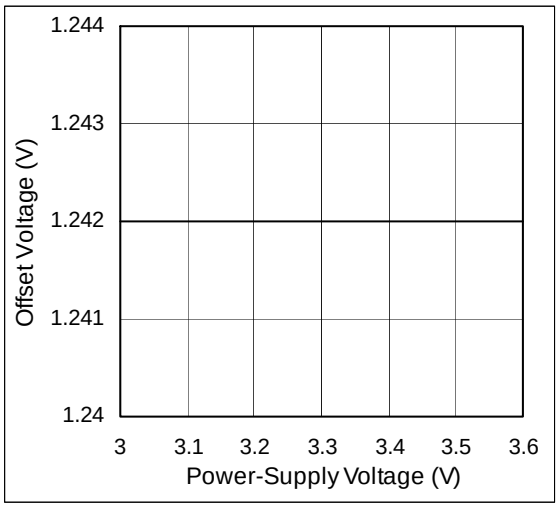


Figure 9. Power Supply Current vs. Frequency; VIN = 0 to 3V

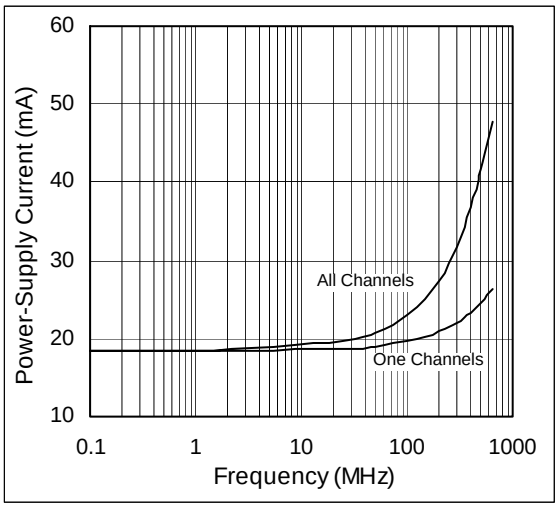


Figure 10. ICC vs. VCC; Freq = 1MHz

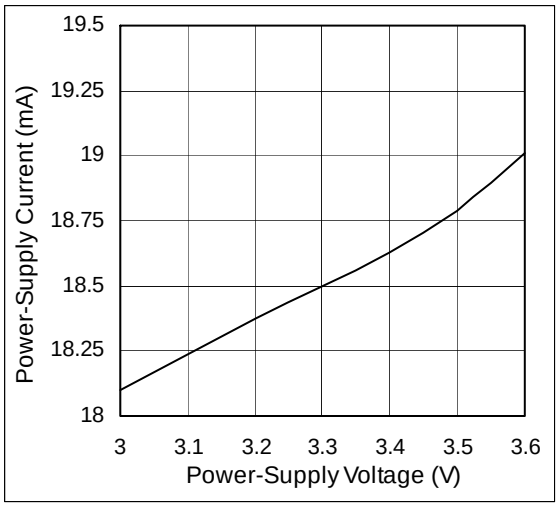


Figure 11. ICC vs. Temperature; Freq = 1MHz

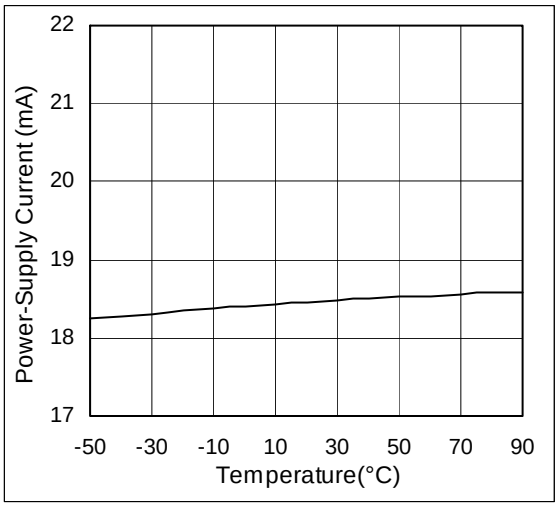


Figure 12. Differential Propagation Delay vs. VCC; Freq = 1MHz

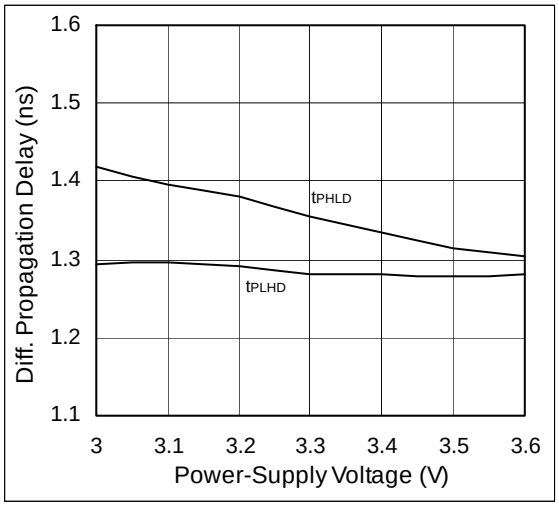


Figure 13. Differential Propagation Delay vs. Temperature; Freq = 1MHz

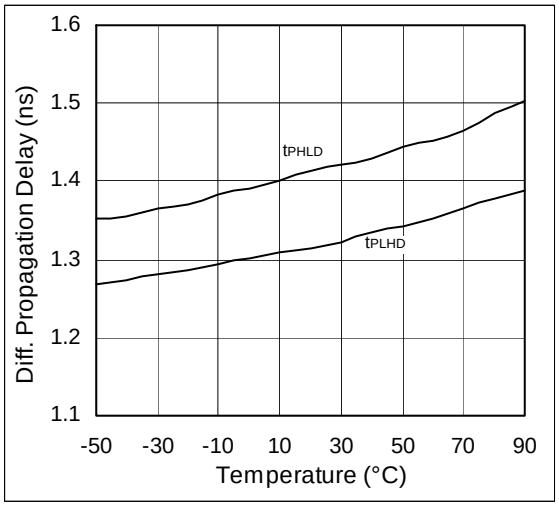


Figure 14. Differential Skew vs. VCC; Freq = 1MHz

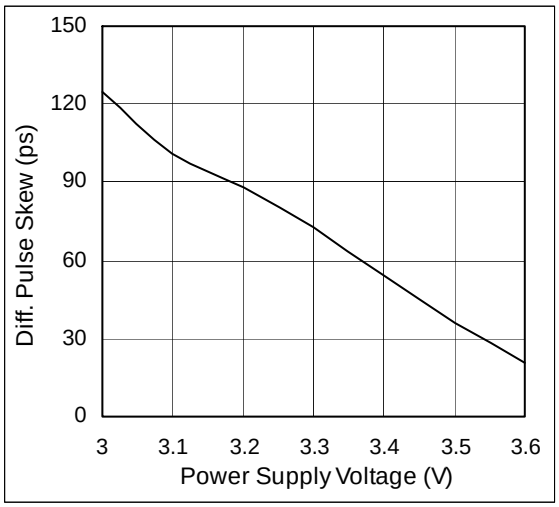
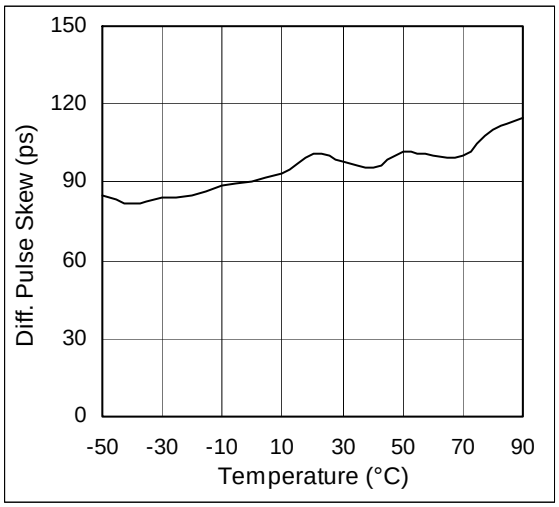


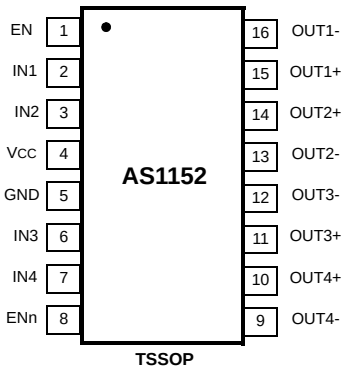
Figure 15. Differential Skew vs. Temperature; Freq = 1MHz



7 Pinout and Packaging

Pin Assignments

Figure 16. AS1152 Pin Assignments (Top View)



Pin Descriptions

Table 4. AS1152 Pin Descriptions

Pin Number	Pin Name	Description
1	EN	Driver Enable Input. Internally pulled down to GND. When EN = high and ENn = low or open, the driver outputs are active. For other combinations of EN and ENn, the outputs are disabled and in high impedance.
2	IN1	LVTTL/LVCMOS Driver Input
3	IN2	LVTTL/LVCMOS Driver Input
4	VCC	Power Supply Input. Bypass VCC to GND with 0.1µF and 0.001µF ceramic capacitors.
5	GND	Ground
6	IN3	LVTTL/LVCMOS Driver Input
7	IN4	LVTTL/LVCMOS Driver Input
8	ENn	Driver Enable Input. Internally pulled down to GND. When EN = high and ENn = low or open, the driver outputs are active. For other combinations of EN and ENn, the outputs are disabled and in high impedance.
9	OUT4-	Inverting LVDS Driver Output
10	OUT4+	Noninverting LVDS Driver Output
11	OUT3+	Noninverting LVDS Driver Output
12	OUT3-	Inverting LVDS Driver Output
13	OUT2-	Inverting LVDS Driver Output
14	OUT2+	Noninverting LVDS Driver Output
15	OUT1+	Noninverting LVDS Driver Output
16	OUT1-	Inverting LVDS Driver Output

8 Detailed Description

LVDS Interface

The LVDS interface standard is a signaling method intended for point-to-point communication over a controlled-impedance medium as defined by the *ANSI/TIA/EIA-644* and *IEEE 1596.3* standards. The LVDS standard uses a lower voltage swing than other common communication standards, achieving higher data rates with reduced power consumption while reducing EMI emissions and system susceptibility to noise.

The AS1152 is an 500Mbps quad differential LVDS driver that is designed for high-speed, point-to-point, low-power applications. This device accepts LVTTL/LVCMOS input levels and translates them to LVDS output signals.

The AS1152 generates a 2.5mA to 4.5mA output current using a current-steering configuration. This current steering approach induces less ground bounce and no shoot-through current, enhancing noise margin and system speed performance. The driver outputs are short-circuit current limited, and enter a high-impedance state when the device is not powered or is disabled.

The current-steering architecture of the AS1152 requires a resistive load to terminate the signal and complete the transmission loop. Because the device switches current and not voltage, the actual output voltage swing is determined by the value of the termination resistor at the input of an LVDS receiver (AS1150, AS1151). Logic states are determined by the direction of current flow through the termination resistor.

With a typical 3.7mA output current, the AS1152 produces an output voltage of 370mV when driving a 100Ω load.

Note: The AS1152 is conform to the ANSI TIA/EIA 644 LVDS Standards when operating ≤150MHz. Paired with the AS1150 the datarate can be increased to 500Mbps. While operating faster then 150MHz, the rise and fall time, as well as the setup and hold time are not conform to the ANSI TIA/EIA 644 LVDS Standards.

Termination

Because the AS1152 is a current-steering device, no output voltage will be generated without a termination resistor. The termination resistors should match the differential impedance of the transmission line. Output voltage levels depend upon the value of the termination resistor.

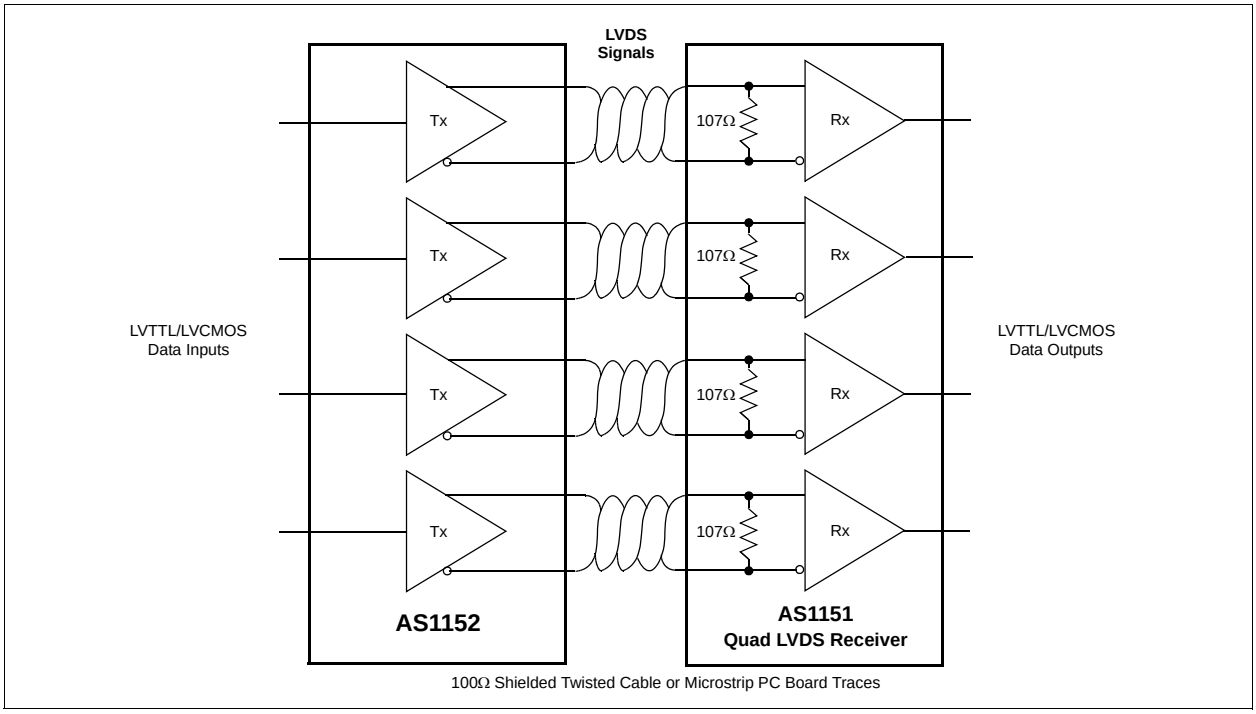
The AS1152 is optimized for point-to-point interface with 100Ω termination resistors at the receiver inputs. Termination resistance values may range between 90 and132Ω, depending on the characteristic impedance of the transmission medium.

9 Applications

Table 5. Function Table

Enable Pins		Input		Output
EN	**ENn**	**IN*x*+**	**IN*x*-**	**OUT*x***
H	L or Open	L	L	H
H	L or Open	H	H	L
Other Combinations of Enable Pin Settings		Don't Care	Z	Z

Figure 17. Typical Application Circuit



Power-Supply Bypassing

To bypass VCC, use high-frequency surface-mount ceramic 0.1µF and 0.001µF capacitors in parallel as close to the device as possible, with the smaller valued capacitor closest to pin VCC.

Differential Traces

Input trace characteristics can adversely affect the performance of the AS1152.

- Use controlled-impedance PC board traces to match the cable characteristic impedance. The termination resistor is also matched to this characteristic impedance.
- Eliminate reflections and ensure that noise couples as common mode by running the differential traces near each other.
- Reduce skew by using matched trace lengths. Tight skew control is required to minimize emissions and proper data recovery of the devices.
- Route each channel's differential signals very close to each other for optimal cancellation of their respective external magnetic fields. Use a constant distance between the differential traces to avoid irregularities in differential impedance.
- Avoid 90° turns (use two 45° turns).
- Minimize the number of vias to further prevent impedance irregularities.

Cables and Connectors

Supported transmission media include printed circuit board traces, backplanes, and cables.

- Use cables and connectors with matched differential impedance (typically 100Ω) to minimize impedance mismatches.
- Balanced cables such as twisted pair offer superior signal quality and tend to generate less EMI due to magnetic field canceling effects. Balanced cables pick up noise as common mode, which is rejected by the LVDS receiver.
- Avoid the use of unbalanced cables such as ribbon cable or simple coaxial cable.

Board Layout

The device should be placed as close to the interface connector as possible to minimize LVDS trace length.

- Keep the LVDS and any other digital signals separated from each other to reduce crosstalk.
- Use a four-layer PC board that provides separate power, ground, LVDS signals, and input signals.
- Isolate the input LVDS signals from each other and the output LVCMOS/LVTTL signals from each other to prevent coupling.
- Separate the input LVDS signals from the output signals planes with the power and ground planes for best results.

Figure 18. Driver Propagation Delay and Transition Time Waveforms

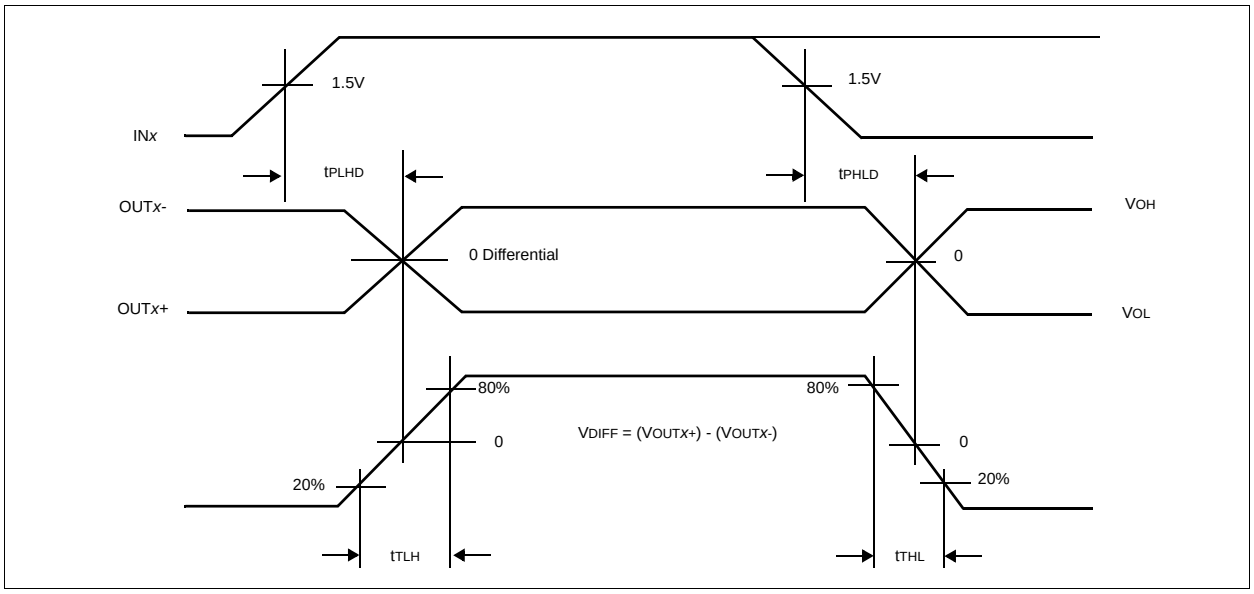


Figure 19. Driver Propagation Delay and Transition Time Test Circuit

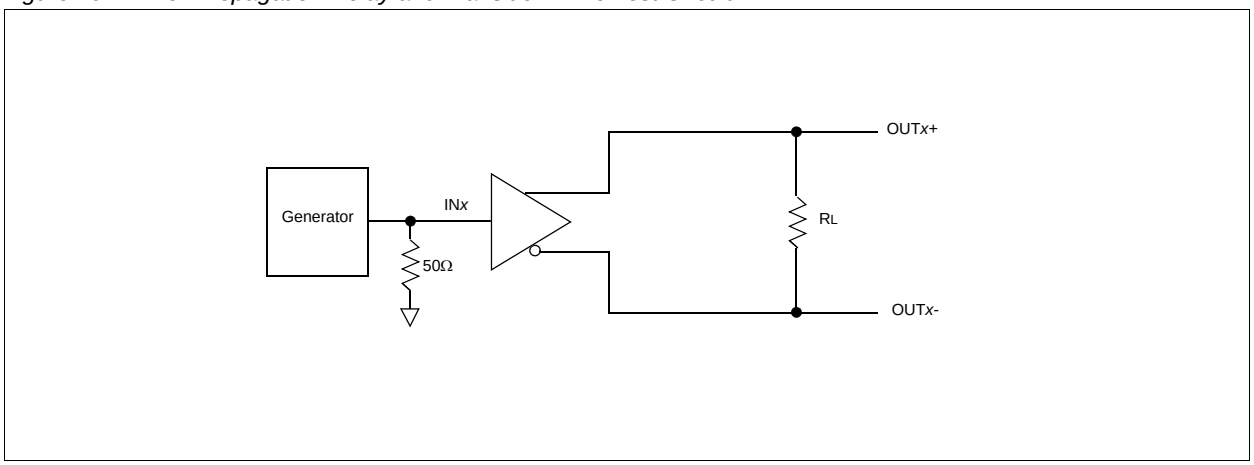


Figure 20. Driver VOD and VOS Test Circuit

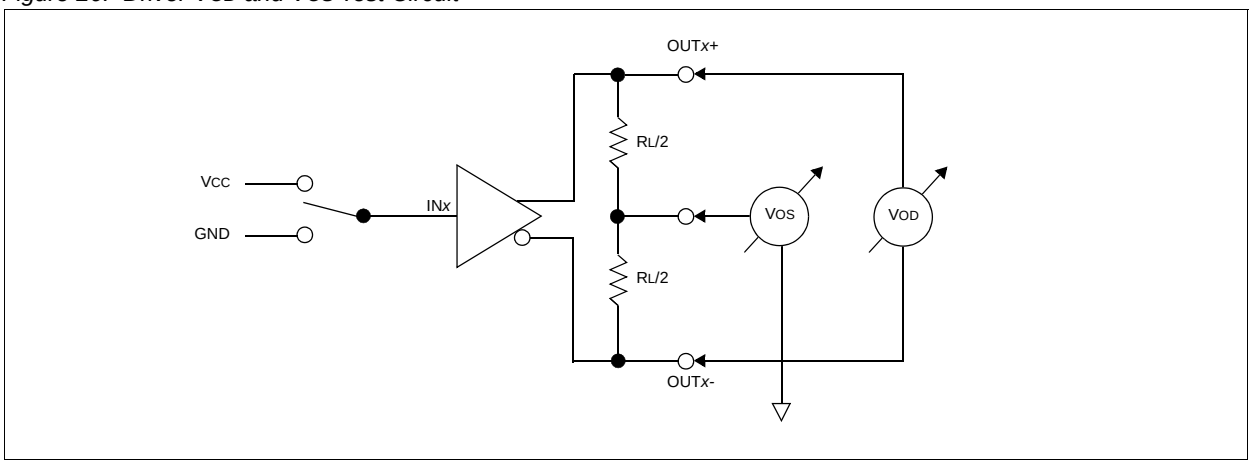


Figure 21. Driver High Impedance Delay Waveforms

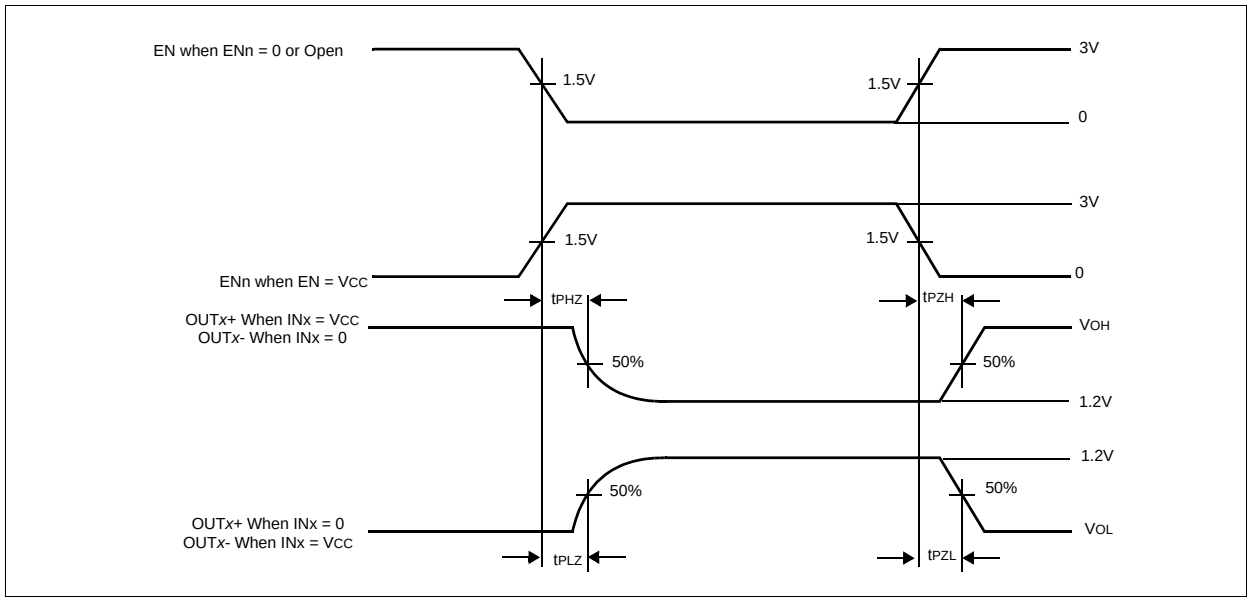
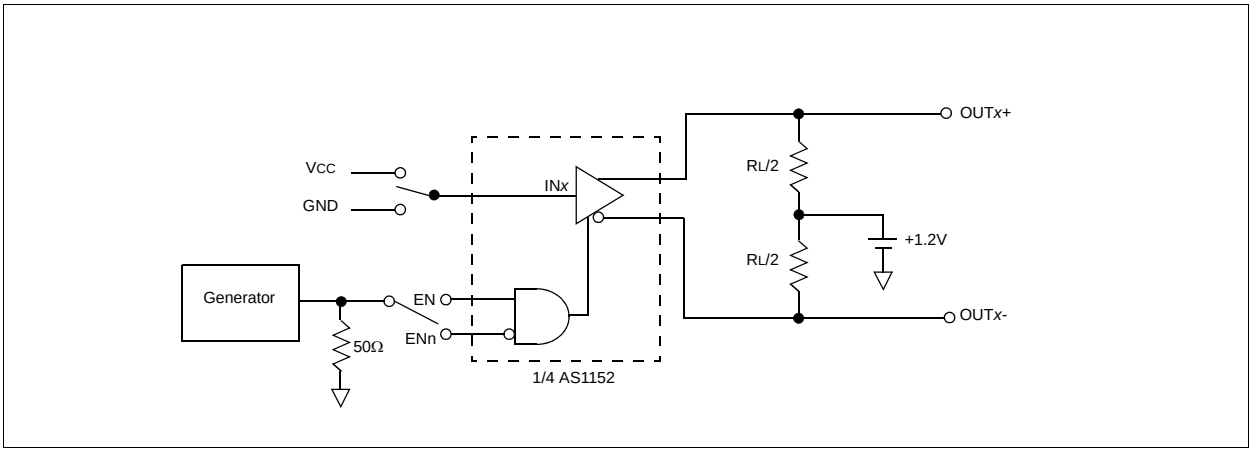
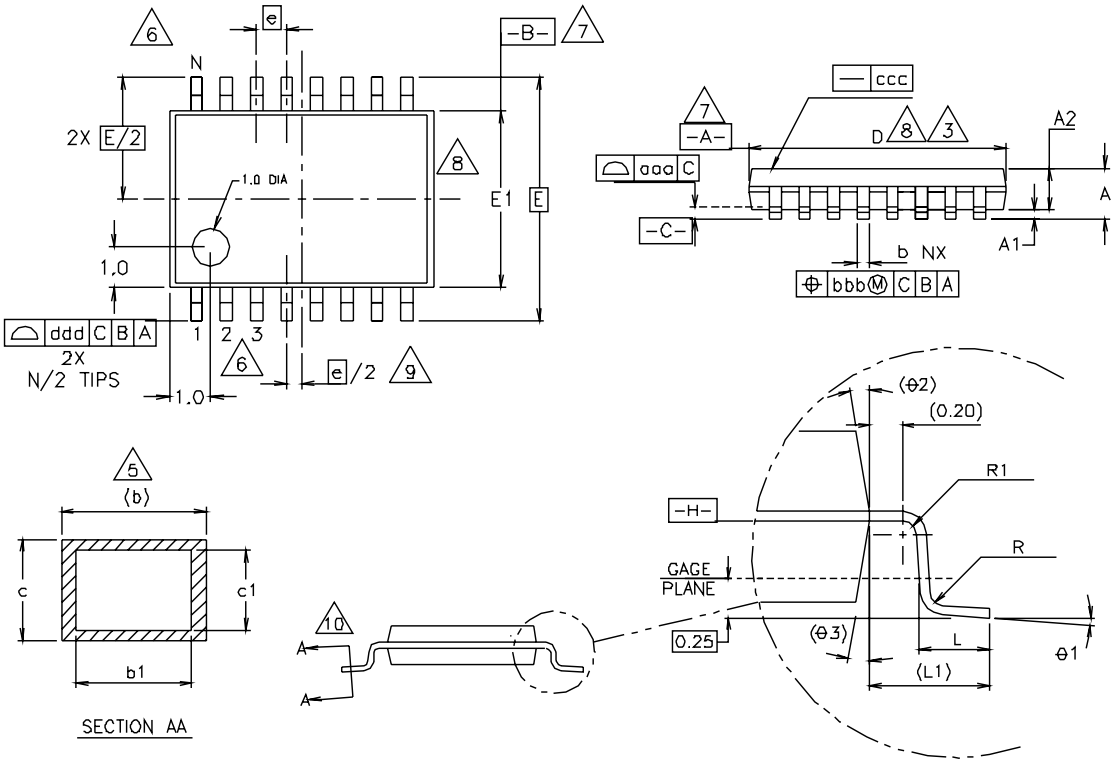


Figure 22. Driver High-Impedance Delay Test Circuit



10 Package Drawings and Markings

Figure 23. 16-pin TSSOP Package



Notes:

1. All dimensions are in millimeters; angles in degrees.
2. Dimensioning and tolerancing per *ASME Y14.5M – 1994*.
3. Dimension D does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, and gate burrs shall not exceed 0.15mm per side.
4. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusions shall not exceed 0.25mm per side.
5. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot.
6. Terminal numbers are for reference only.
7. Datums A and B to be determined at datum plane H.
8. Dimensions D and E1 are to be determined at datum plane H.
9. This dimension applies only to variations with an even number of leads per side.
10. Cross section A-A to be determined at 0.10 to 0.25mm from the leadtip.

Symbol	Min	Typ	Max	Notes
A	-	-	1.10	1,2
A1	0.05	-	0.15	1,2
A2	0.85	0.90	0.95	1,2
L	0.50	0.60	0.75	1,2
R	0.09	-	-	1,2
R1	0.09	-	-	1,2
b	0.19	-	0.30	1,2,5
b1	0.19	0.22	0.25	1,2
c	0.09	-	0.20	1,2
c1	0.09	-	0.16	1,2
θ1	0º	-	8º	1,2
L1	1.0REF			1,2
aaa	0.10			1,2
bbb	0.10			1,2
ccc	0.05			1,2
ddd	0.20			1,2
e	0.65BSC			1,2
θ2	12ºREF			1,2
θ3	12ºREF			1,2
Variations				
D	4.90	5.00	5.10	1,2,3,8
E1	4.30	4.40	4.50	1,2,4,8
E	6.4BSC			1,2
e	0.65BSC			1,2
N	16			1,2,6

11 Ordering Information

Part Number	Description	Package Type	Delivery Form
AS1152	Quad low-voltage differential signaling driver	16-pin TSSOP	Tube
AS1152-T	Quad low-voltage differential signaling driver	16-pin TSSOP	Tape and Reel

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