ARC3C0845/ARC3C0845W

Document Category: Product Specification

High-Efficiency LED Backlight Driver

General Description

The ARC3C0845/ARC3C0845W is an ultra-high efficiency DC-DC converter solution with integrated programmable current sinks that drive up to eight strings of LEDs. The ARC3C0845/ARC3C0845W integrates all MOSFETs and their control and driver circuitry. With its proprietary architecture, the ARC3C0845/ARC3C0845W provides the highest efficiency—up to 96%—possible in a compact 3.44 mm x 2.415 mm WLCSP 40-pin package (ARC3C0845W) or 4 mm x 4 mm 32-pin QFN package (ARC3C0845). The high switching frequency enables a small and low-profile solution size aligned to the needs of the latest mobile products.

Features

- Synchronous DC-DC converter with integrated FETs
- 2- and 3-cell Li-ion battery input voltage for LED boost: 4.5V to 15V
- Proprietary architecture for ultra-high LED efficiency, above 88% over the operating range
- Integrated output disconnect switch
- Up to 45V output for maximum flexibility in assignment of LEDs to strings and selection of LED forward voltage
- Up to 12-bit dimming resolution with an additional 3-bit dithering
- Linear/logarithmic analog and PWM dimming for maximum flexibility and resolution
- LED brightness ramp up/down control with programmable ramp rate and linear/logarithmic ramp profiles
- Phase-shifted PWM dimming among active strings to minimize audible noise
- 1 MHz I^2C 6.0-compatible serial interface to program the brightness, or an external resistor on ISET pin to set the maximum brightness
- Extensive programming capability with non-volatile memory for storing user register settings
- Eight independently enabled current sinks, up to 43 mA per current sink
- External PWM input for fine dimming resolution
- 0.5% current matching at 30 mA per current sink
- Wide range of input and output voltages with 2x charge pump ratio
- Selectable boost switching frequency from 320 kHz to 2.6 MHz
- Extensive fault protection, including boost over-current protection, output short circuit protection, output over-voltage protection, LED open and short protection, and thermal shutdown

Applications

Typical applications for 2- and 3-cell platforms include the following:

- 8”-17” FHD/UHD + LCD backlight panels
- Ultrabooks, ultraportables, and notebooks
- 2-in-1, convertible, and detachable notebooks
- Full-size tablet computers
- LCD panels
- Ultra-thin form factor mobile platforms

Efficiency

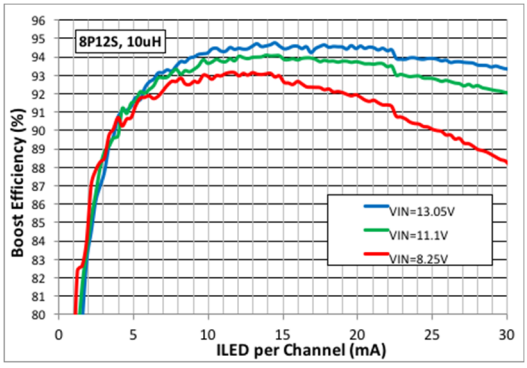

Figure 1. Typical Boost Efficiency – 8p12s

Application

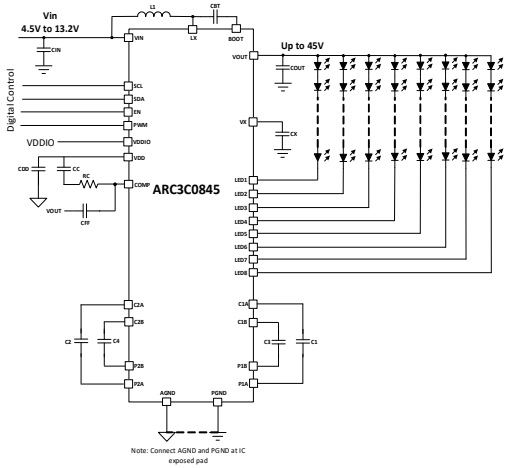

Figure 2. Typical Application Circuit

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Absolute Maximum Ratings

Exceeding the absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between operating range maximum and absolute maximum for extended periods could reduce reliability.

ESD Precautions

When handling this device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the ratings specified in Table 1.

Table 1. ARC3C0845/ARC3C0845W Absolute Maximum Ratings

Parameter	Min	Max(1)	Unit
VIN to AGND	-0.3	17.6	V
VDD, VDDIO, PWM, COMP, EN, ISET, SCL, SDA, ADDR to AGND	-0.3	6	V
VOUT, C1B, C2B to AGND	-0.3	47	V
LEDx to AGND	-0.3	40	V
AGND to PGND	-0.3	0.3	V
LX, VX, P1A, P2A, P1B, P2B to PGND	-0.3	22	V
VX to LX, P1A, P2A, P1B, P2B	-0.3	22	V
BOOT to VDD	-0.3	22	V
BOOT to LX	-0.3	6	V
C1A, C2A to VX	-0.3	22	V
C1B to C2A	-0.3	33	V
C2B to C1A	-0.3	33	V
Storage temperature	-65	150	°C
Junction temperature (J_T)	–	150	°C
Bump or lead temperature (soldering and reflow)	–	260	°C
ESD tolerance, PE23363 HBM(2)(4)	–	1000	V
ESD tolerance, PE23102 HBM(2)	–	1000	V
ESD tolerance, CDM(3)	–	1000	V

Notes:

1. These “Absolute Maximum Ratings” are stress ratings only; the notation of these conditions does not imply functional operation of the device at these or any other conditions that fall outside the range identified by the operational sections of this specification.
2. Human body model, per JEDEC standard JS-001-2017.
3. Field-induced charge device model, per JEDEC standard JESD22-C101.
4. With exception, contact pSemi for details. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. Pins listed as 1000V might have higher ESD performance

Recommended Operating Conditions

Table 2 lists the ARC3C0845/ARC3C0845W recommend operating conditions. Do not operate the device outside the operating conditions listed below.

Table 2. ARC3C0845/ARC3C0845W Recommended Operating Conditions

Parameter	Min	Max	Unit
V_{IN} input voltage range, relative to AGND or PGND(*)	4.5	15	V
V_{OUT} output voltage range, relative to AGND PGND(*)	18	45	V
VX boost output voltage range, relative to AGND or PGND	1.2*VIN	20	V
V_{DDIO} voltage range, relative to AGND	1.08	5.5	V
Junction temperature range (J_T)	-30	+125	°C
Note: * The V_{IN} and V_{OUT} ranges must meet the valid operating regions as shown in Figure 5.			

Package Thermal Characteristics

Table 3 lists the package thermal characteristics.

Table 3. Package Thermal Characteristics(1)(2))

Device	Parameter	Max	Unit
ARC3C0845	Junction-to-ambient thermal resistance (Θ_{JA}), soldered thermal pad, connected to plane	47	°C/W
	Junction-to-board thermal characterization (Ψ_{JB})	25	°C/W
	Junction-to-top case thermal characterization (Ψ_{JC})	5.8	°C/W
ARC3C0845W	Junction-to-ambient thermal resistance (Θ_{JA}), soldered thermal pad, connected to plane	46	°C/W
	Junction-to-board thermal characterization (Ψ_{JB})	11	°C/W
	Junction-to-top case thermal characterization (Ψ_{JC})	8	°C/W

Notes:

1. The package thermal characteristics and performance are measured and reported in a manner consistent with JEDEC standards JESD51-8 and JESD51-12.
2. The junction-to-ambient thermal resistance (Θ_{JA}) is a function not only of the IC, but it is also extremely sensitive to the environment which includes, but is not limited to, board thickness, planes, copper weight/routes, and air flow. To realize the expected thermal performance, pay close attention to the board layout.

Electrical Specifications

Table 4 lists the ARC3C0845/ARC3C0845W key electrical specifications at the following conditions, unless otherwise noted. Typical values are at $T_A = T_J = 25$ °C with 8p12s.

VIN = 7.4V, $V_{AGND} = V_{PGND} = 0V$, $V_{EN} = 1.8V$, $T_A = T_J = -30$ °C to +85 °C

The minimum and maximum specifications in Table 4 are 100% production tested at $T_A = T_J = 25$ °C, unless otherwise noted. Limits over the operating range are guaranteed by design.

Table 4. ARC3C0845/ARC3C0845W Electrical Specifications

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Input supply							
Input voltage range	V_{VIN}	For the operating ranges, see Figure 5.		4.5	–	15	V
Voltage regulator output voltage	V_{VDD}	–		–	4.4	5.0	V
Under-voltage lockout (UVLO) threshold high	V_{UVLO_H}	V_{VIN} rising		–	4.275	4.45	V
Under-voltage lockout (UVLO) hysteresis	V_{UVLO_HYST}	–		–	60	–	mV
Shutdown supply current	I_{VIN_SD}	I_{VIN} with $V_{EN} = 0V$		–	–	1	µA
Standby supply current	I_{VIN_STDBY}	$V_{EN} = 1.8V$, I^2C_STDBY=1		–	–	300	µA
Supply voltage for digital I/Os	V_{DDIO}	–		1.08	–	5.5	V
Supply current for digital I/Os	I_{VDDIO}	EN = 0V or 1.8V, SDA = SCL = 0V or V_{DDIO}, measure at $V_{DDIO} = 1.8V$		–	8	–	µA
Thermal shutdown threshold(1)	T_{TSD}	–		–	150	–	°C
Thermal shutdown hysteresis(1)	T_{TSD_HYST}	–		–	20	–	°C
Soft start timeout duration	–	–		–	10	–	ms
Step-up converter: boost							
Output voltage range(2)(3)	V_{OUT}	–		18	–	45	V
Maximum output power(4)	–	–		10	–	–	W
Boost switching frequency range	f_{SW_BOOST}	I^2C interface only FSW_BOOST [4:0]	10011	–	0.512	–	MHz
			01001	–	1.024	–	
			00101	–	1.707	–	
			00011	–	2.56	–	
		Non-I^2C interface only	SDA = VDD	–	1.138	–	
			SDA = open	–	0.731	–	
			SDA = AGND	–	0.51	–	
Boost switching frequency accuracy	–	–		-6	–	+6	%

Boost minimum off-time	$T_{OFF\_BOOST\_MIN}$	–		–	50	–	ns
Boost minimum on-time	$T_{ON\_BOOST\_MIN}$	–		–	50	–	ns
Boost low-side switch current limit, cycle-by-cycle	I_{BOOST_LIMIT}	I_{LX} rising	BOOST_ILIM [1:0]=00	–	2.0	–	A
			BOOST_ILIM [1:0]=01	–	1.0	–	
			BOOST_ILIM [1:0]=10	–	3.0	–	
			BOOST_ILIM[1:0]=11	–	4.0	–	
Step-up converter: charge pump							
Output over-current threshold	I_{OUT_OC}	I_{OUT} rising		375	–	–	mA
Output over-voltage threshold	V_{OUT_OVP}	$OVP_{TH[3:0]}$	0010	–	47.5	–	V
			0011	–	45.625	–	
			…	–	…	–	
			1111	–	19.375	–	
Output over-voltage hysteresis	$V_{OUT\_OVP\_HYST}$	–		–	0.35	–	V
Accuracy of output over-voltage protection threshold	V_{UVLO_HYST}	–		-5	–	5	%
LED current sinks (LED1 to LED8)							
ISET voltage	V_{ISET}	–		–	0.4	–	V
ISET pin voltage accuracy	–	–		-3	–	3	V
ISET recommended resistor range	R_{ISET}	Excluding resistor tolerance (E96, 1% tolerance)		13.3	–	133	kΩ
Current multiplier	K_{ISET}	I^2C register setting MAX_I[4:0]	MAX_I[4:0]=00000	–	400	–	A/A
			MAX_I[4:0]=00001	–	433	–	
			…	–	…	–	
			MAX_I [4:0]=11111	–	1433	–	
LED current full-scale output range	I_{LED_MAX}	I^2C register setting MAX_I[4:0]	MAX_I [4:0]=00000	–	12	–	mA
			MAX_I [4:0]=00001	–	13	–	
			…	–	…	–	
			MAX_I [4:0]=11111	–	43	–	
Minimum sink current LED1–8	I_{LEDx_MIN}	I_{MAX} programmed to 30 mA, linear mapping		–	7.3	–	µA
Leakage current	$I_{LED\_LEAKAGE}$	LED1…LED8 = 0, V_{OUT} = 36V		–	0.75	2	µA
LED current matching[5]	$I_{LED\_MATCHING}$	I_{LEDX} programmed to 30 mA		-1	–	1	%
LED current matching[5]	$I_{LED\_MATCHING}$	I_{LEDX} programmed to 0.5 mA		-2.5	–	2.5	%
LED current accuracy[6]	$I_{LED\_ACCURACY}$	I_{LEDX} programmed to 30 mA		-2	–	2	%
LED regulation voltage	$V_{LED\_REGULATION}$	I_{LEDX} programmed to 30 mA, T_A = 25 °C		–	500	–	mV

LED shorted string detection threshold	–	V_{LEDX} falling	LED_SHORT_VTH[1:0] = 00	–	4.35	–	V
			LED_SHORT_VTH[1:0] = 01	–	4.85	–	
			LED_SHORT_VTH[1:0] = 10	–	5.25	–	
			LED_SHORT_VTH[1:0] = 11	–	5.75	–	
Current ripple	–	I_{LED} programmed to 20 mA, T_A = 25 °C, DC LED current output		–	–	1	%
Internal PWM dimming							
Transition point between internal PWM and analog dimming[6]	–	DIM_MODE=0		–	0	–	%
		DIM_ MODE=1	PWM_IX[1:0] = 00	–	12.5	–	%
			PWM_IX[1:0] = 01	–	25 (default)	–	
			PWM_IX[1:0] = 10	–	50	–	
			PWM_IX[1:0] = 00	–	100	–	
		Non-I²C interface[6]		–	25	–	
LED PWM output frequency	f_{LEDX}	I²C interface, PWM_DIM_FREQ[2:0]		2..5	–	40	kHz
		Non-I²C interface		–	2.5	–	
LED current sink minimum output pulse width	–	–		–	200	–	ns
Direct PWM dimming							
Direct PWM input to output timing skew	–	–		–	100	–	ns
Logic interface							
EN logic input high voltage	V_{IH_EN}	–		1.2	–	–	V
EN logic input low voltage	V_{IL_EN}	–		–	–	0.4	V
PWM logic input high voltage	V_{IH_PWM}	–		0.9	–	–	V
PWM logic input low voltage	V_{IL_PWM}	–		–	–	0.5	V
Logic input current	I_{PWM}, I_{EN}	–		-1.0	–	1.0	µA
ADDR input resistance	I_{ADDR_R}	I²C interface only		–	100	–	kΩ
ADDR input low voltage	V_{IL_ADDR}	I²C interface only		–	–	0.4	V
ADDR input high voltage	V_{IH_ADDR}	I²C interface only		V_{DD}-0.4	–	–	V
SDA, SCL pin input resistance	I_{SDA/SCL_R}	Non-I²C interface only		–	100	–	kΩ
SDA, SCL pin input low voltage	$V_{IL\_SDA/SCL}$	Non-I²C interface only		–	–	0.4	V
SDA, SCL pin input high voltage	$V_{IH\_SDA/SCL}$	Non-I²C interface only		V_{DD}-0.4	–	–	V
PWM pin input frequency for internal PWM mode	F_{IPWM}	–		0.2	–	40	kHz
PWM pin input frequency for direct PWM mode	F_{DPWM}	–		0.2	–	20	kHz
PWM pin minimum input high pulse	–	–		100	–	–	ns

PWM pin minimum input low pulse	–	–	100	–	–	ns
PC serial interface (SCL, SDA, and VDDIO)						
VDDIO supply voltage range	V_{DDIO}	–	1.08	–	5.5	V
SDA, SCL input high voltage	V_{IH}	–	0.7 x V_{VDDIO}	–	–	V
SDA, SCL input low voltage	V_{IL}	–	–	–	0.3 x V_{VDDIO}	V
SDA, SCL input hysteresis	V_{HYS}	–	0.05 x V_{VDDIO}	–	–	V
SDA, SCL input current	I_{SCL}, I_{SDA}	–	-1	–	1	µA
SDA output low level	V_{OL}	I_{SDA} = 20 mA	–	–	0.4	V
I^2C interface initial wait time	–	Initial wait time from EN logic high to the first accepted I^2C command	1	–	–	ms
MTP non-volatile memory write cycle time	–	–	–	34	50	ms
SDA, SCL pin capacitance	$C_{I/O}$	–	–	–	10	pF
I^2C interface timing characteristics for standard, fast mode, and fast mode plus						
Serial clock frequency	F_{SCL}	Standard mode	–	–	100	kHz
		Fast mode	–	–	400	
		Fast mode plus	–	–	1000	
Clock low period	t_{LOW}	Standard mode	4.7	–	–	µs
		Fast mode	1.3	–	–	
		Fast mode plus	0.5	–	–	
Clock high period	t_{HIGH}	Standard mode	4	–	–	µs
		Fast mode	0.6	–	–	
		Fast mode plus	0.26	–	–	
BUS free time between a STOP and a START condition	t_{BUF}	Standard mode	4.7	–	–	µs
		Fast mode	1.3	–	–	
		Fast mode plus	0.5	–	–	
Setup time for a repeated START condition	$t_{SU:STA}$	Standard mode	4.7	–	–	µs
		Fast mode	0.6	–	–	
		Fast mode plus	0.26	–	–	
Hold time for a repeated START condition	$t_{HD:STA}$	Standard mode	4	–	–	µs
		Fast mode	0.6	–	–	
		Fast mode plus	0.26	–	–	
Setup time of STOP condition	$t_{SU:STO}$	Standard mode	4	–	–	µs
		Fast mode	0.6	–	–	
		Fast mode plus	0.26	–	–	

Data setup time	$t_{SU:DAT}$	Standard mode	0.25	–	–	µs
		Fast mode	0.1	–	–	
		Fast mode plus	0.05	–	–	
Data hold time	t_{HD_DAT}	Standard mode	0	–	–	µs
		Fast mode	0	–	–	
		Fast mode plus	0	–	–	
Rise time of SCL signal	t_{RCL}	Standard mode	–	–	1	µs
		Fast mode	0.02	–	0.3	
		Fast mode plus	–	–	0.12	
Fall time of SCL signal	t_{FCL}	Standard mode	–	–	0.3	µs
		Fast mode	–	–	0.3	
		Fast mode plus	–	–	0.12	
Rise time of SDA signal	t_{RDA}	Standard mode	–	–	1	µs
		Fast mode	0.02	–	0.3	
		Fast mode plus	–	–	0.12	
Fall time of SDA signal	t_{FDA}	Standard mode	–	–	0.3	µs
		Fast mode	20 x V_{DDIO}/ 5.5V	–	0.3	
		Fast mode plus	20 x V_{DDIO}/ 5.5V	–	0.12	
Data valid time	t_{VD}	Standard mode	–	–	3.45	µs
		Fast mode	–	–	0.9	
		Fast mode plus	–	–	0.45	
Data valid acknowledge time	t_{VDA}	Standard mode	–	–	3.45	µs
		Fast mode	–	–	0.9	
		Fast mode plus	–	–	0.45	
Capacitive load for SDA and SCL	C_{BUS}	Standard mode	–	–	400	pf
		Fast mode	–	–	400	
		Fast mode plus	–	–	550	

Notes:

1. Thermal shutdown is not production tested.
2. The V_{IN} and V_{OUT} ranges must meet the valid operating regions as shown in Figure 5.
3. At light loads while in DCM mode, V_{OUT} could be higher than expected, but the LED current regulation is not adversely affected.
4. Higher output power is possible under certain operating conditions. For details, contact pSemi.
5. The LED current accuracy is defined/tested as: 100 * (I_{LED_AVG} - I_{LED_Target}) / I_{LED_AVG}. The sink current matching is defined and tested as (I_{LED_MAX} - I_{LED_MIN}) / I_{LED_AVG}.
6. The default is 25%, but can be trimmed to 0, 12.5%, 50% or 100% if needed for non-I^2C mode.

Pin Configuration

This section includes the ARC3C0845/ARC3C0845W configuration information. Figure 3 shows the pin map of the ARC3C0845 in the 4 mm x 4 mm 32-pin LGA package, and Figure 4 shows the pin map of the ARC3C0845W in the 3.44 mm x 2.415 mm WLCSP40 package. Table 5 lists the descriptions for each pin.

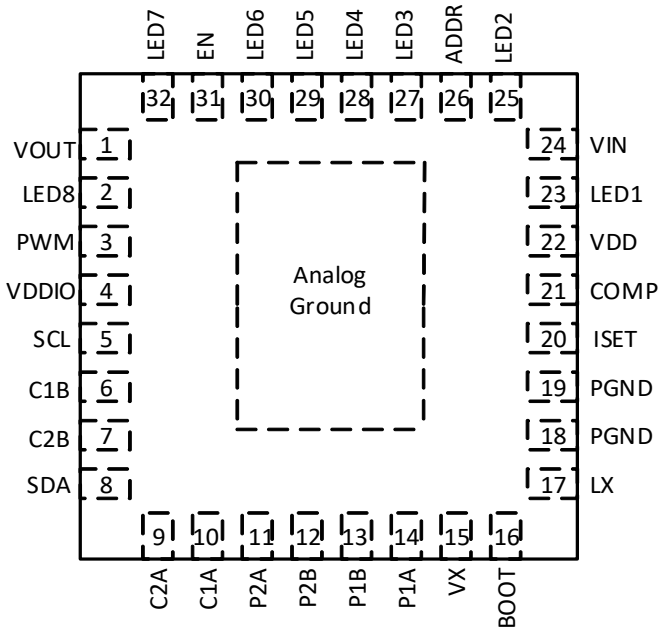


Figure 3. ARC3C0845 32-Pin LGA Top View

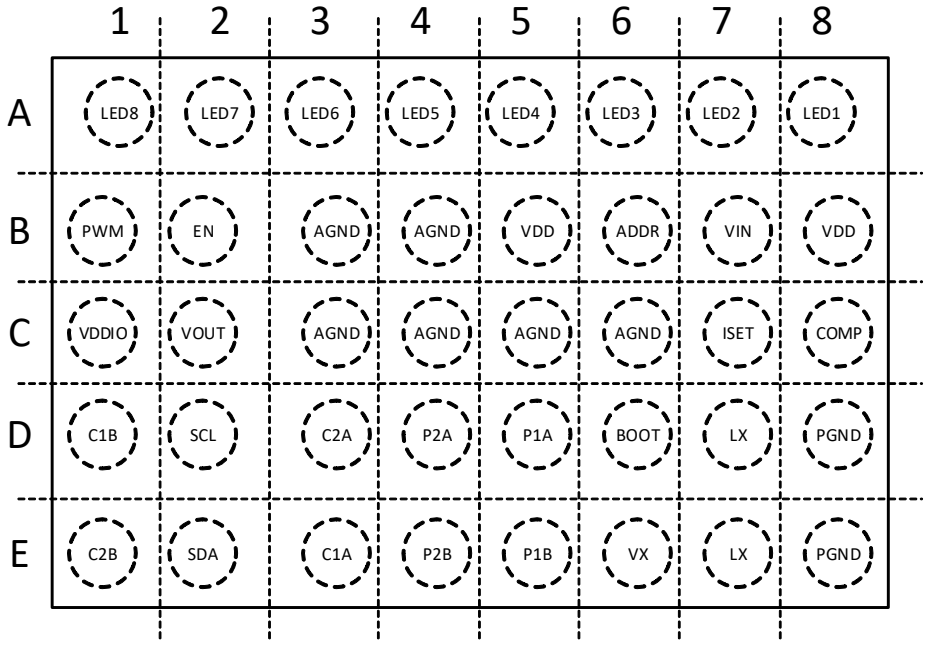


Figure 4. ARC3C0845W WLCSP40 Top View

Pin Descriptions

Table 5 lists the ARC3C0845/ARC3C0845W pin descriptions. For the capacitor and inductor selection guidelines, see Component Selection on page 64.

Table 5. ARC3C0845/ARC3C0845W Pin Descriptions

ARC3C0845 32P QFN Pin No.	ARC3C0845W WLCSP40 Pin No.	Pin Name	Description
EP Pad	B3, B4, C3, C4, C5, C6	AGND	Analog and LED current sink ground. Tie externally to the ground plane and the PGND pins.
1	C2	VOUT	Power converter output voltage. Connect to the high side of all LED strings. Connect externally to the C_{OUT} capacitor.
2	A1	LED8	Individual LED current sink. Connect to the low side of the individual LED strings.
3	B1	PWM	PWM dimming input for brightness control. If not used, connect to the VDD pin.
4	C1	VDDIO	Digital IO supply voltage for the I^2C interface, used as the I^2C VIH and VIL reference. Can be tied to the VDD pin. To use the non-I^2C interface, connect to AGND.
5	D2	SCL	Serial clock for the I^2C bus. Also used in non-I^2C mode to select between the three dimming modes.
6	D1	C1B	Charge pump fly capacitor positive node. Connect the capacitor from C1B to P1B.
7	E1	C2B	Charge pump fly capacitor positive node. Connect the capacitor from C2B to P2B.
8	E2	SDA	Serial data for the I^2C bus. Also used in non-I^2C mode to select between the three switching frequencies.
9	D3	C2A	Charge pump fly capacitor positive node. Connect the capacitor from C2A to P2A.
10	E3	C1A	Charge pump fly capacitor positive node. Connect the capacitor from C1A to P1A.
11	D4	P2A	Charge pump fly capacitor phase node. Connect the capacitor from P2A to C2A..
12	E4	P2B	Charge pump fly capacitor phase node. Connect the capacitor from P2B to C2B.
13	E5	P1B	Charge pump fly capacitor phase node. Connect the capacitor from P1B to C1B.
14	D5	P1A	Charge pump fly capacitor phase node. Connect the capacitor from P1A to C1A.
15	E6	VX	Charge pump input node, internally driven by the output of the boost converter. Connect capacitor Cx between this pin and PGND.
16	D6	BOOT	Bootstrap capacitor for the boost stage high-side FET. Connect a 22 nF, 10V, or higher capacitor from BOOT to LX.
17	D7, E7	LX	Fully synchronous switching node for the boost power inductor, which connects between LX and input voltage V_{IN}.
18,19	D8, E8	PGND	Power ground, which must tie externally to the ground plane and the AGND EP pad. High current path.
20	C7	ISET	LED current setting pin. Connect a resistor from this pin to AGND to set the full-scale LED current in non-I^2C mode or when the ISET_EXT bit is set to 1 in I^2C mode.

21	C8	COMP	External compensation pin. For details, see Switching Converter Compensation on page 35.
22	B5, B8	VDD	Internal LDO output pin. Connect capacitor CVDD between this pin and PGND.
23	A8	LED1	Individual LED current sink. Connect to the low side of individual LED strings.
24	B7	VIN	Input voltage, battery power supply pin
25	A7	LED2	Individual LED current sink. Connect to the low side of individual LED strings.
26	B6	ADDR	Sets the lower three bits of the I^2C slave address: ▪ 000: Tie to the AGND pin. ▪ 010: Leave floating. ▪ 101: Tie to the VDD pin.
27	A6	LED3	Individual LED current sink. Connect to the low side of the individual LED strings.
28	A5	LED4	Individual LED current sink. Connect to the low side of the individual LED strings.
29	A4	LED5	Individual LED current sink. Connect to the low side of the individual LED strings.
30	A3	LED6	Individual LED current sink. Connect to the low side of the individual LED strings.
31	B2	EN	Enable input
32	A2	LED7	Individual LED current sink. Connect to the low side of the individual LED strings.

Operating Voltage Range and Charge Pump Ratio

To improve efficiency, the ARC3C0845/ARC3C0845W uses a 2x/3x charge-pump. The charge pump architecture requires the battery input voltage to be less than the output voltage divided by 2.15x in 2x mode and by 3.2x in 3x mode:

$$\text{For 2x Charge Pump Mode: } Vin \leq \frac{Vout}{2.15}$$

$$\text{For 3x Charge Pump Mode: } Vin \leq \frac{Vout}{3.2}$$

Figure 5 shows a graph of the output voltage versus input voltage. In addition to maintaining the minimum V_{OUT}/V_{IN} requirement for the 2x/3x charge pump modes, the graph shows a region called “Out of Regulation Zone for 2x/3x Charge Pump Mode” not supported for normal operation. Failure to maintain the minimum V_{OUT}/V_{IN} requirement or attempting to operate in the “Out of Regulation Zone for 2x/3x Charge Pump Mode” could result in the ARC3C0845/ARC3C0845W having lower efficiency, faulting off, or requiring a restart. To prevent the VX over voltage condition, operate the charge pump in 3x charge pump mode for V_{OUT} > 40V.

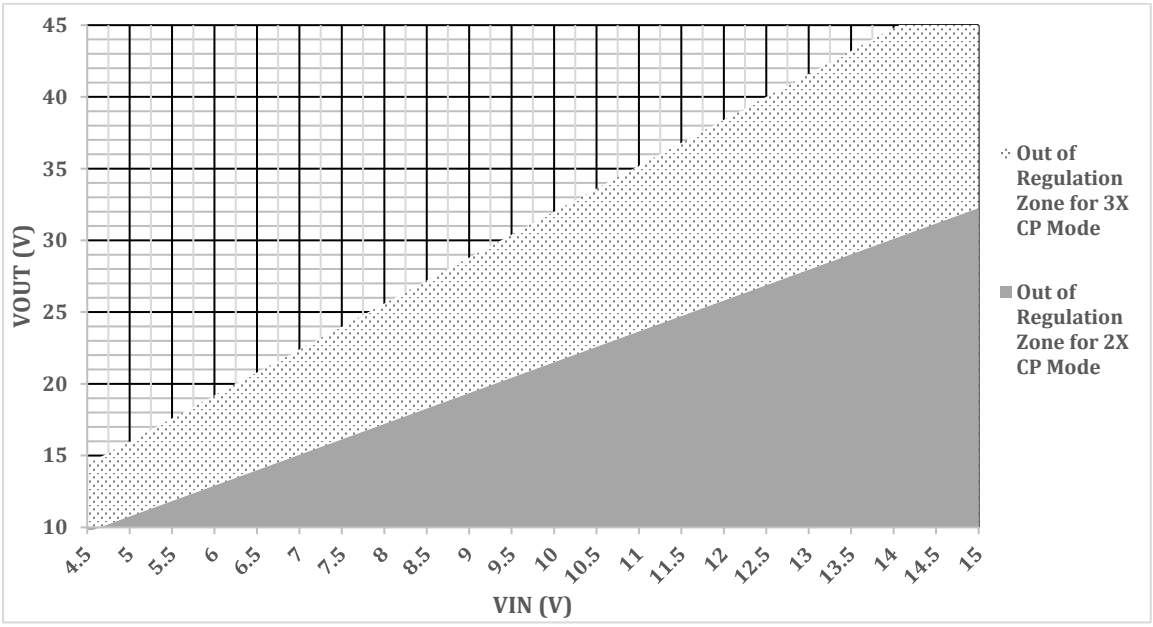


Figure 5. V_{OUT} vs V_{IN} Requirement

To optimize efficiency, the ARC3C0845/ARC3C0845W has an automatic feature (AUTOCP) to switch between the 2x or 3x charge pump modes, depending on the V_{IN} and V_{OUT} conditions. This feature is enabled by setting the AUTO_CP_RATIO register bit to 0. The charge pump ratio can also be set to a fixed 2x or 3x ratio by setting the AUTO_CP_RATIO bit to 1 to and use the SEL_CP_RATIO to select the 2x or 3x charge pump mode.

When using the AUTOCP feature, the 2X to 3X charge pump switchover must not cause an out-of-regulation issue for the application operating range. For example, a V_{IN} = 12V and the LED current is increasing to push the V_{OUT} from 37V into 38V. The charge pump would transition from 2x into 3x mode. In 2x mode, the minimum V_{OUT} requirement to prevent out of regulation is 25.8V, which is below the 37V operation condition. But in 3X mode, the minimum V_{OUT} requirement to prevent out of regulation is 38.4V, which is over the 38V operation condition and causes an out-of-regulation issue. For this example, pSemi recommend operating the charge pump in a fixed 2x mode to prevent out of regulation issues.

Table 6 shows the charge pump ratio in AUTOCP mode for different V_{IN} and V_{OUT} conditions. The charge pump automatically switches from 2x to 3x mode or 3x to 2x mode when the V_{IN} or V_{OUT} conditions cross over the threshold. The gray area indicates out-of-regulation operation for 3x mode and in this case pSemi recommends setting the charge pump operation to fixed 2x mode. The black area indicates out-of-regulation operation for 2x mode. When V_{OUT} is 40V or higher, set the charge pump to fixed 3x mode to avoid an overvoltage condition on the VX pin.

Table 6. AUTOCP Charge Pump Ratio at Different V_{OUT} and V_{IN} Conditions

VOUT\VIN	4.5	5	5.5	6	6.5	7	7.5	8	8.5	9	9.5	10	11	12	13
20	3X	3X	3X	2X	2X	2X	2X	2X	2X	2X					
21	3X	3X	3X	3X	2X	2X	2X	2X	2X	2X	2X				
22	3X	3X	3X	3X	2X	2X	2X	2X	2X	2X	2X	2X			
23	3X	3X	3X	3X	3X	2X	2X	2X	2X	2X	2X	2X			
24	3X	3X	3X	3X	3X	2X	2X	2X	2X	2X	2X	2X	2X		
25	3X	3X	3X	3X	3X	3X	2X	2X	2X	2X	2X	2X	2X		
26	3X	3X	3X	3X	3X	3X	2X	2X	2X	2X	2X	2X	2X	2X	
27	3X	3X	3X	3X	3X	3X	3X	2X	2X	2X	2X	2X	2X	2X	
28	3X	3X	3X	3X	3X	3X	3X	2X	2X	2X	2X	2X	2X	2X	2X
29	3X	3X	3X	3X	3X	3X	3X	3X	2X	2X	2X	2X	2X	2X	2X
30	3X	3X	3X	3X	3X	3X	3X	3X	3X	2X	2X	2X	2X	2X	2X
31	3X	3X	3X	3X	3X	3X	3X	3X	3X	2X	2X	2X	2X	2X	2X
32	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	2X	2X	2X	2X	2X
33	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	2X	2X	2X	2X	2X
34	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	2X	2X	2X	2X
35	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	2X	2X	2X	2X
36	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	2X	2X	2X
37	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	2X	2X	2X
38	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X
39	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X
40	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X
41	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X
42	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X
43	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X
44	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X
45	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X

Functional Block Diagram

Figure 6 shows the ARC3C0845/ARC3C0845W functional block diagram.

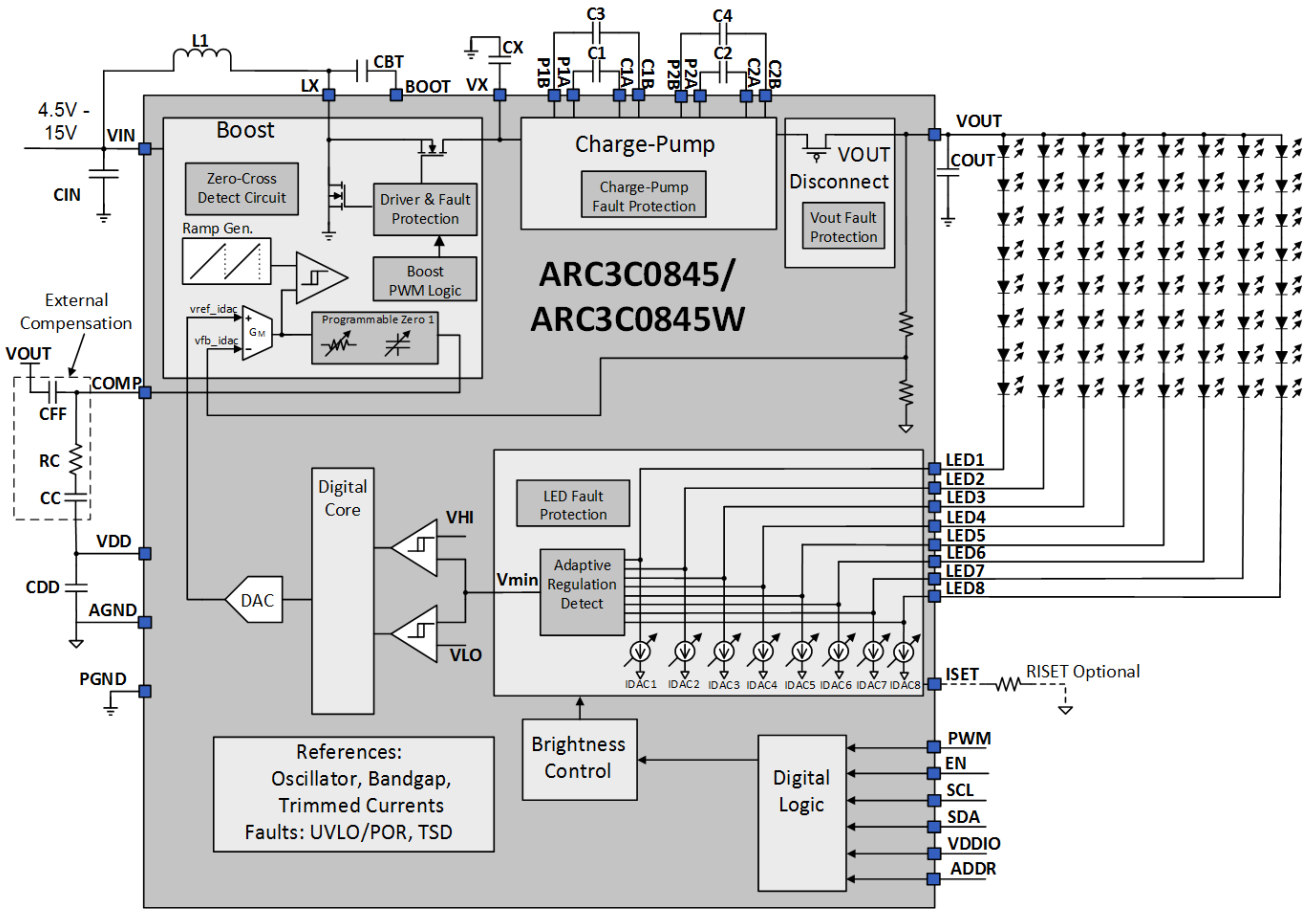


Figure 6. ARC3C0845/ARC3C0845W Functional Block Diagram

Application Circuit

For the application circuit:

- ARC3C0845: Connect PGND and AGND at the ICs exposed pad (EP).
- ARC3C0845W: Connect PGND and AGND at the ICs AGND bumps.

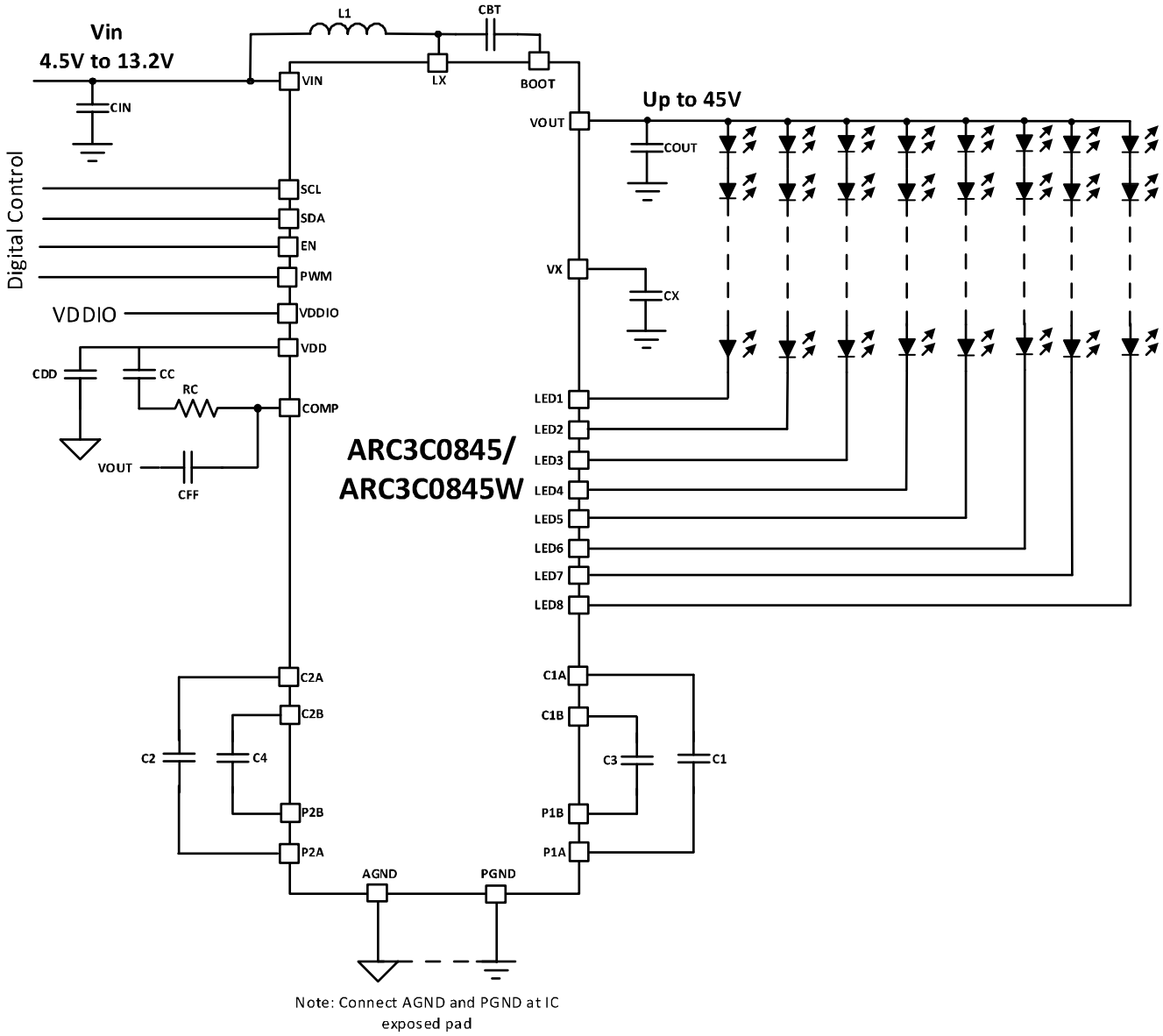


Figure 7. I²C Interface Application Schematic

Typical Performance Data

Figure 8–Figure 13 show the ARC3C0845/ARC3C0845W typical performance data with C_{OUT} = 4.7 µF, LED VF = 3V at 20 mA (typical), and analog dimming, unless otherwise specified.

LED efficiency: 931-kHz boost frequency, 2-cell only input voltage with 2.2 µH, 1.2-mm high chip inductor (part number DFE322512F-2R2M).

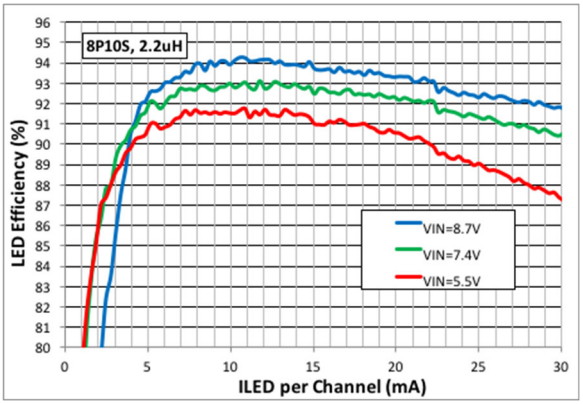


Figure 8. 8P10S LED Efficiency, 2.2 µH Inductor

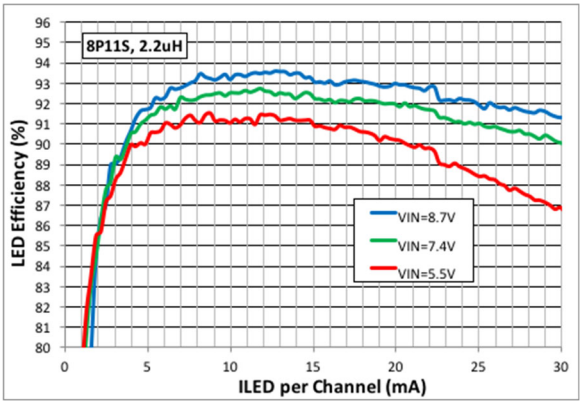


Figure 9. 8P11S LED Efficiency, 2.2 µH Inductor

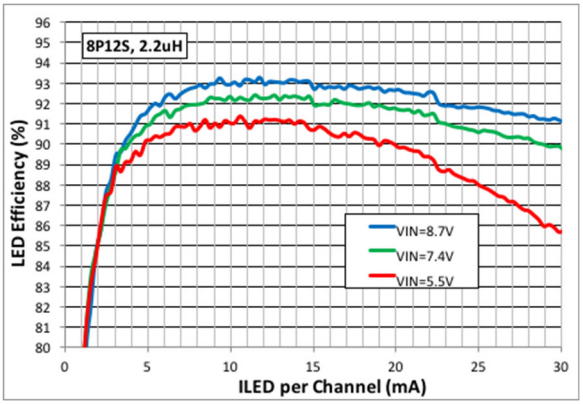


Figure 10. 8P12S LED Efficiency, 2.2 µH Inductor

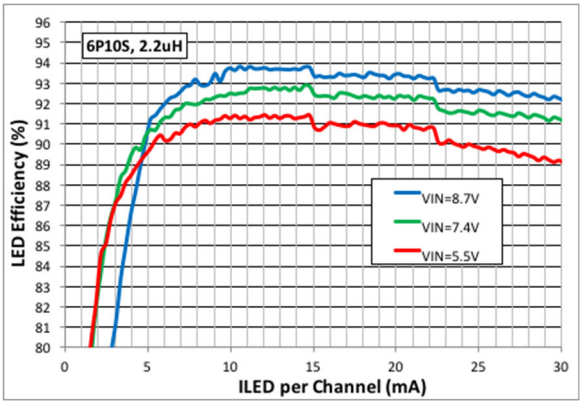


Figure 11. 6P10S LED Efficiency, 2.2 µH Inductor

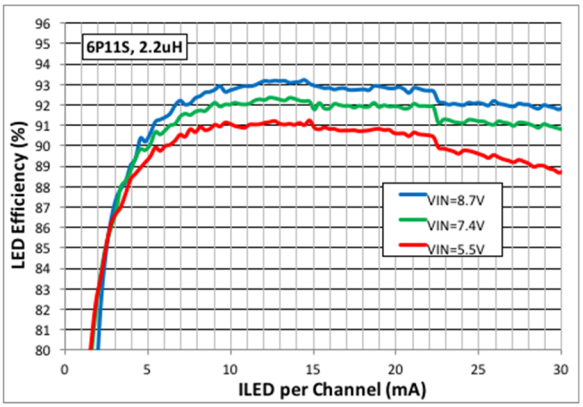


Figure 12. 6P11S LED Efficiency, 2.2 µH Inductor

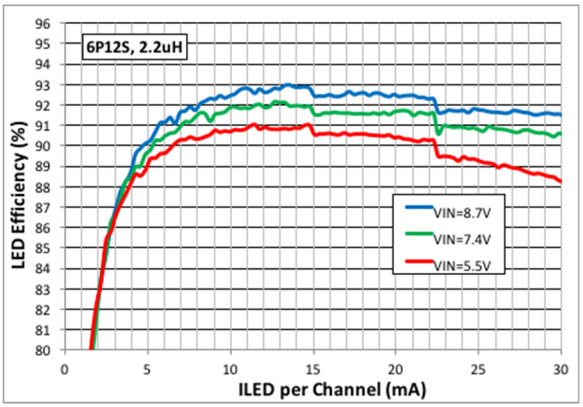


Figure 13. 6P12S LED Efficiency, 2.2 µH Inductor

Figure 14–Figure 17 show the ARC3C0845/ARC3C0845W typical performance data with C_{OUT} = 4.7 µF, LED VF = 3V at 20 mA (typical), and analog dimming, unless otherwise specified.

LED efficiency: 787-kHz boost frequency, 2-cell only input voltage with 4.7 µH, 1.2-mm high chip inductor (part number DFE322512F-4R7M).

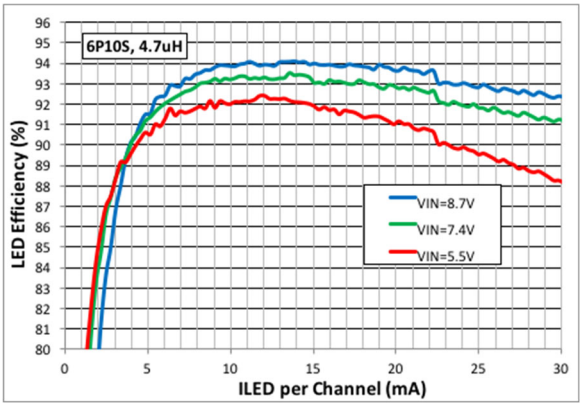


Figure 14. 6P10S LED Efficiency, 4.7 µH Inductor

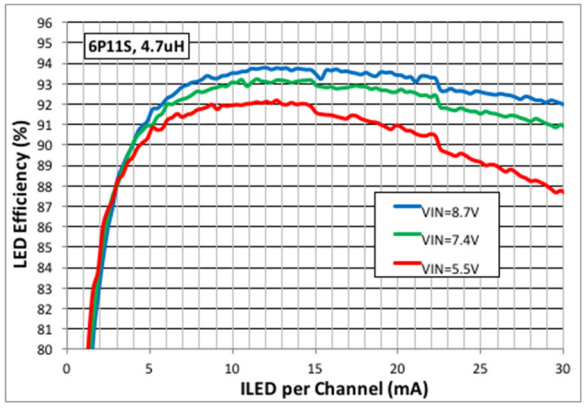


Figure 15. 6P11S LED Efficiency, 4.7 µH Inductor

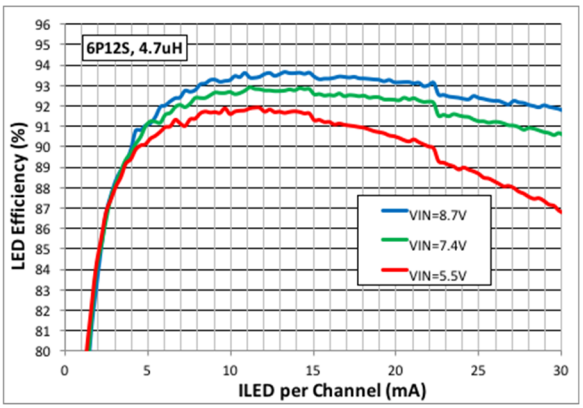


Figure 16. 6P12S LED Efficiency, 4.7 µH Inductor

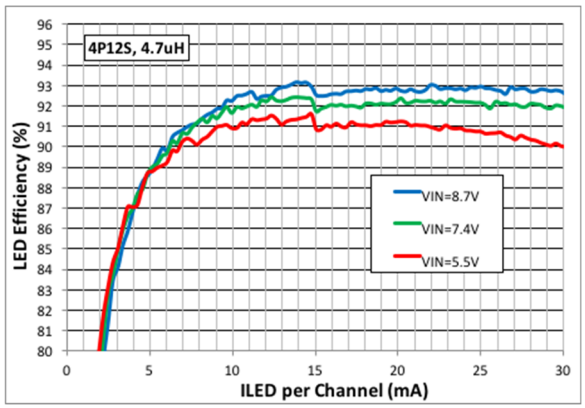


Figure 17. 4P12S LED Efficiency, 4.7 µH Inductor

Figure 18–Figure 23 show the ARC3C0845/ARC3C0845W typical performance data with C_{OUT} = 4.7 µF, LED VF = 3V at 20 mA (typical), and analog dimming, unless otherwise specified.

LED efficiency: 731-kHz boost frequency, 3-cell only input voltage with 6.8 µH, 1.2-mm high chip inductor (part number DFE322512F-6R8M).

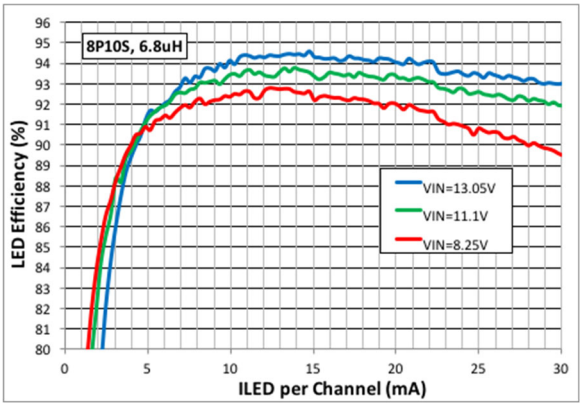


Figure 18. 8P10S LED Efficiency, 6.8 µH Inductor

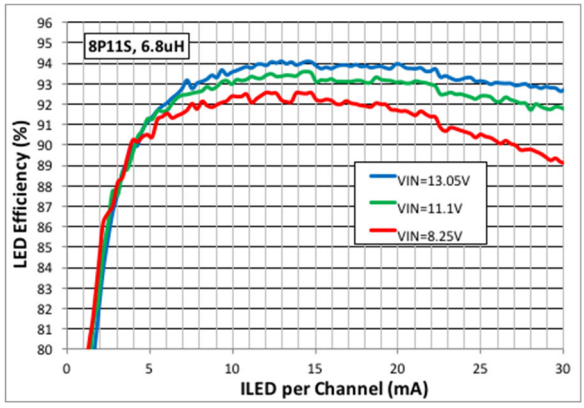


Figure 19. 8P11S LED Efficiency, 6.8 µH Inductor

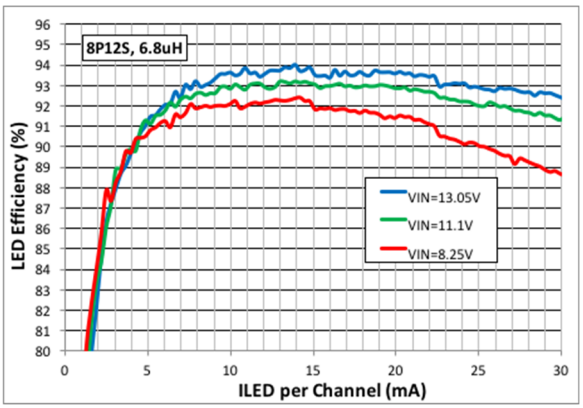


Figure 20. 8P12S LED Efficiency, 6.8 µH Inductor

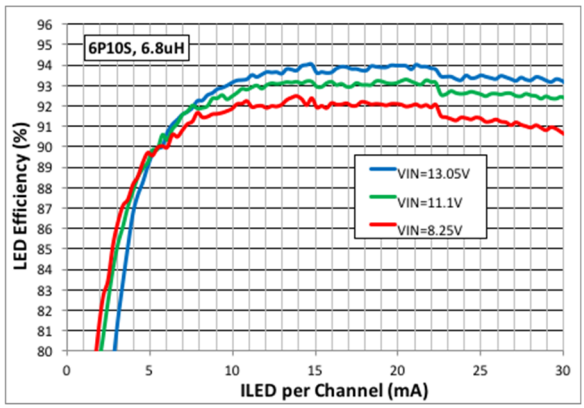


Figure 21. 6P10S LED Efficiency, 6.8 µH Inductor

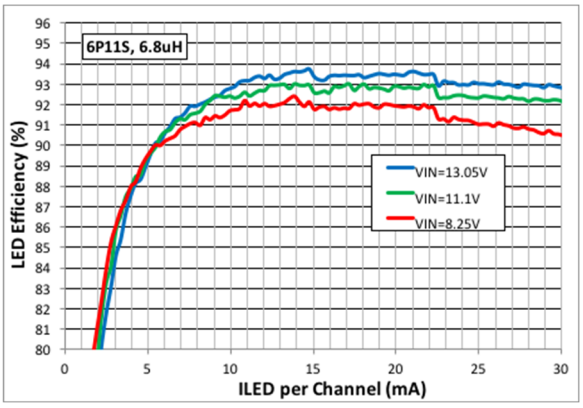


Figure 22. 6P11S LED Efficiency, 6.8 µH Inductor

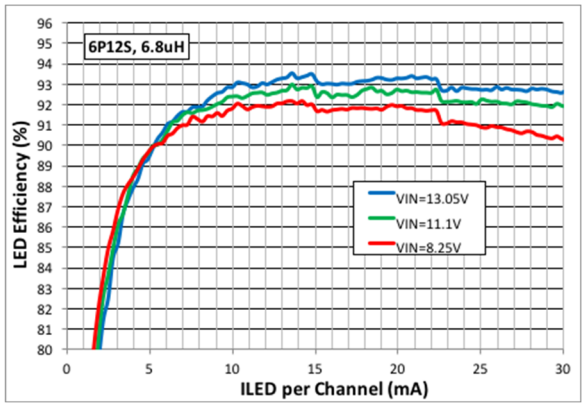


Figure 23. 6P12S LED Efficiency, 6.8 µH Inductor

Figure 24–Figure 25 show the ARC3C0845/ARC3C0845W typical performance data with C_{OUT} = 4.7 µF, LED VF = 3V at 20 mA (typical), and analog dimming, unless otherwise specified.

LED efficiency: 731-kHz boost frequency, 3-cell only input voltage with 6.8 µH inductor (part number DFE322512F-6R8M) and 10 µH (part number DFE322512F-100M) 1.2-mm high chip inductors.

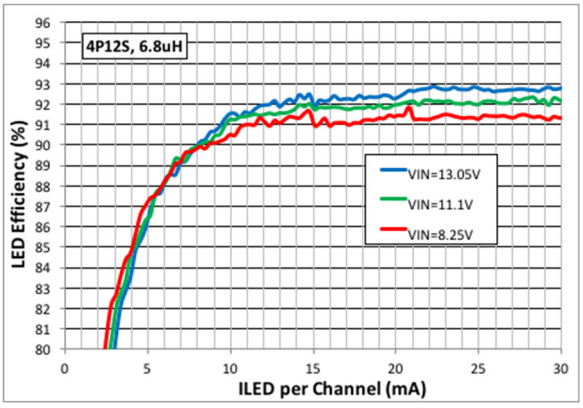


Figure 24. 4P12S LED Efficiency, 6.8 µH Inductor

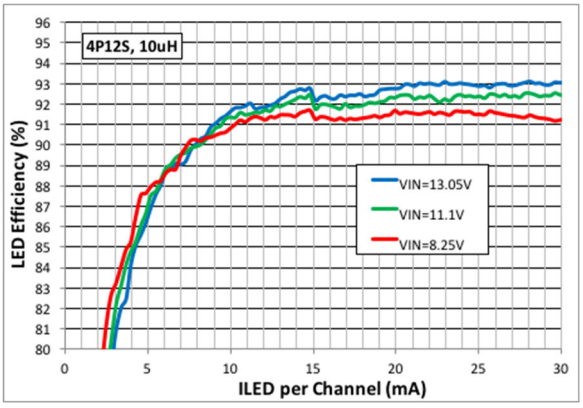


Figure 25. 4P12S LED Efficiency, 10 µH Inductor

Figure 26–Figure 31 show the ARC3C0845/ARC3C0845W typical performance data with C_{OUT} = 4.7 µF, LED VF = 3V at 20 mA (typical), and analog dimming, unless otherwise specified.

LED efficiency: 853-kHz boost frequency, 2-cell and 3-cell NVDC input voltage with 3.3 µH, 1.2-mm high chip inductor (part number DFE322512F-3R3M).

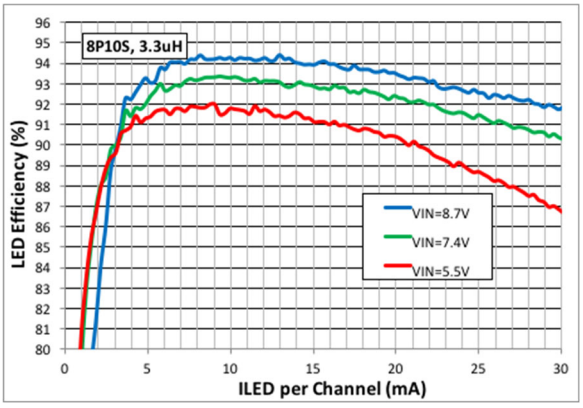


Figure 26. 2S, 8P10S LED Efficiency, 3.3 µH Inductor

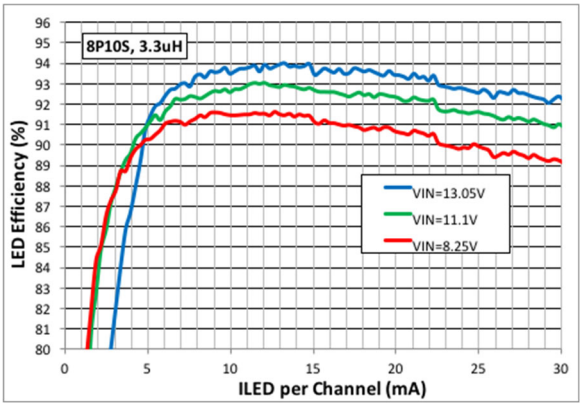


Figure 27. 3S,8P10S LED Efficiency, 3.3 µH Inductor

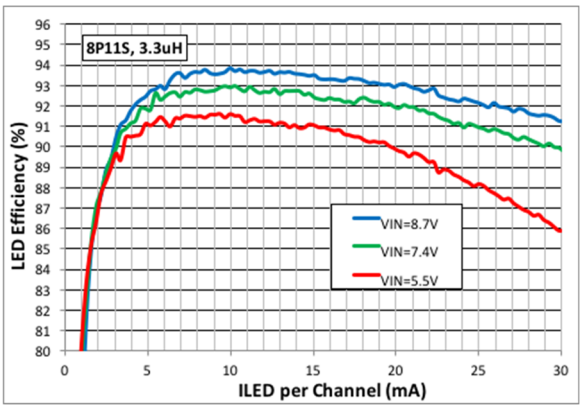


Figure 28. 2S, 8P11S LED Efficiency, 3.3 µH Inductor

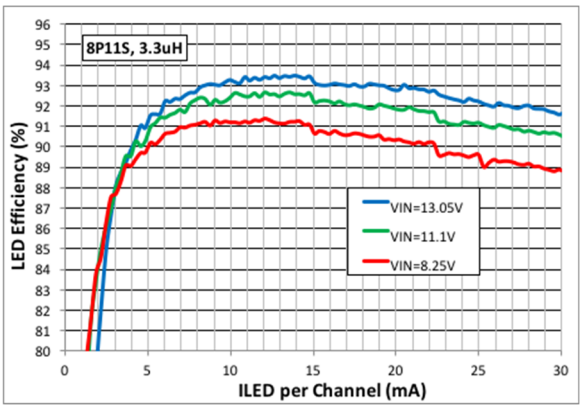


Figure 29. 3S, 8P11S LED Efficiency, 3.3 µH Inductor

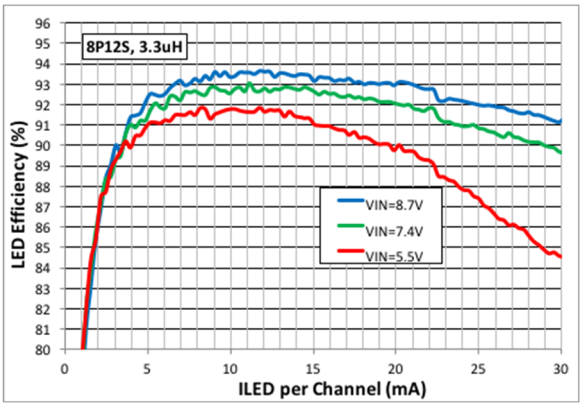


Figure 30. 2S, 8P12S LED Efficiency, 3.3 µH Inductor

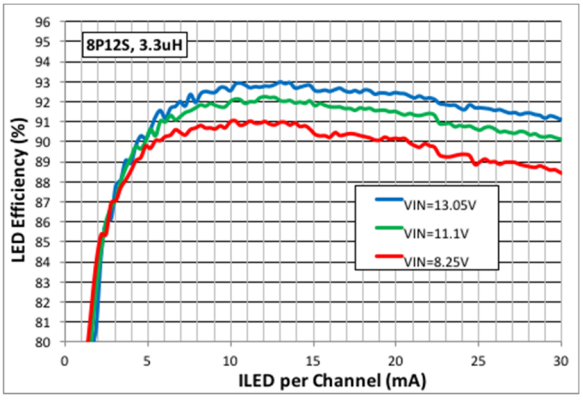


Figure 31. 3S, 8P12S LED Efficiency, 3.3 µH Inductor

Figure 32–Figure 37 show the ARC3C0845/ARC3C0845W typical performance data with C_{OUT} = 4.7 µF, LED VF = 3V at 20 mA (typical), and analog dimming, unless otherwise specified.

LED efficiency: 853-kHz boost frequency, 2-cell and 3-cell NVDCy input voltage with 3.3 µH, 1.2-mm high chip inductor (part number DFE322512F-3R3M).

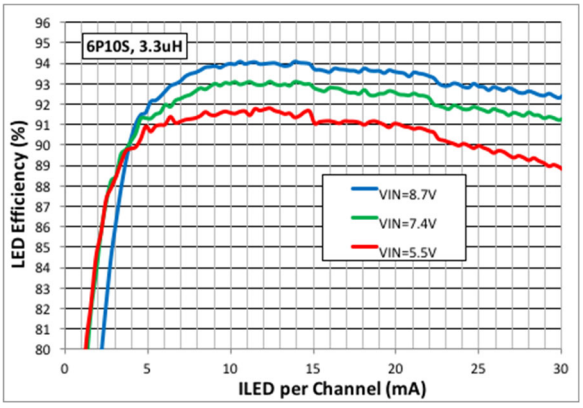


Figure 32. 2S, 6P10S LED Efficiency, 3.3 µH Inductor

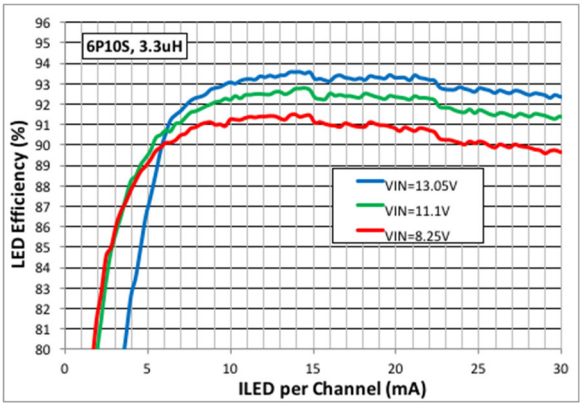


Figure 33. 3S, 6P10S LED Efficiency, 3.3 µH Inductor

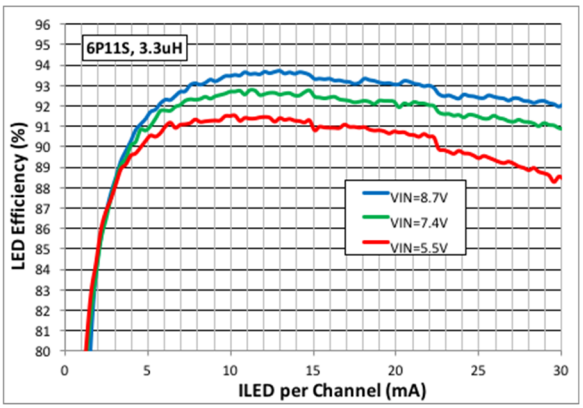


Figure 34. 2S, 6P11S LED Efficiency, 3.3 µH Inductor

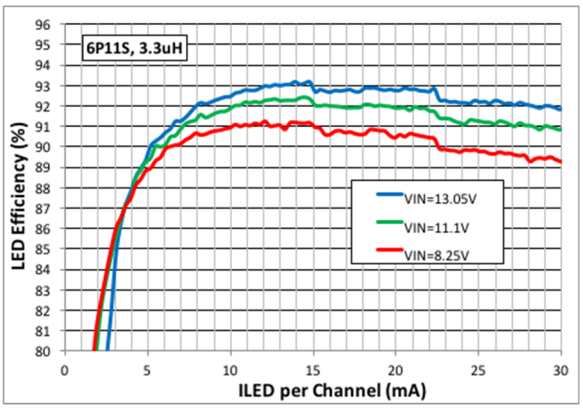


Figure 35. 3S, 6P11S LED Efficiency, 3.3 µH Inductor

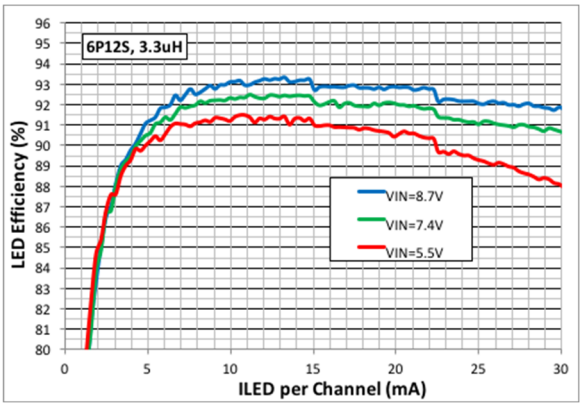


Figure 36. 2S, 6P12S LED Efficiency, 3.3 µH Inductor

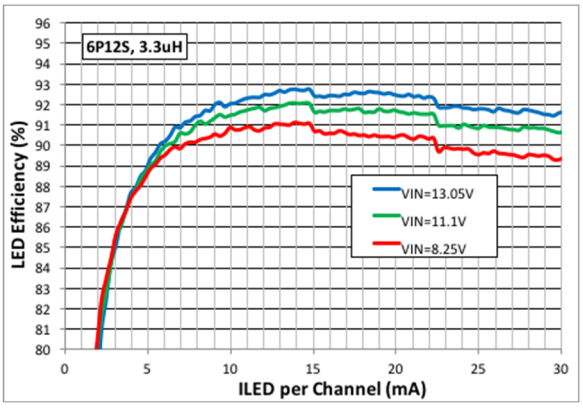


Figure 37. 3S, 6P12S LED Efficiency, 3.3 µH Inductor

Figure 38–Figure 39 show the ARC3C0845/ARC3C0845W typical performance data with C_{OUT} = 4.7 µF, LED VF = 3V at 20 mA (typical), and analog dimming, unless otherwise specified.

LED efficiency: 853-kHz boost frequency, 2-cell and 3-cell NVDC input voltage with 3.3 µH, 1.2-mm high chip inductor (part number DFE322512F-3R3M).

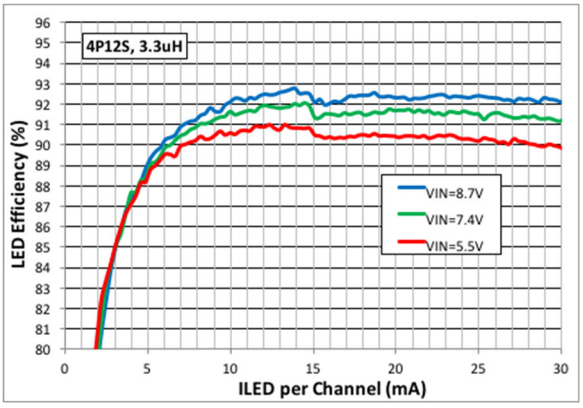


Figure 38. 2S, 4P12S LED Efficiency, 3.3 µH Inductor

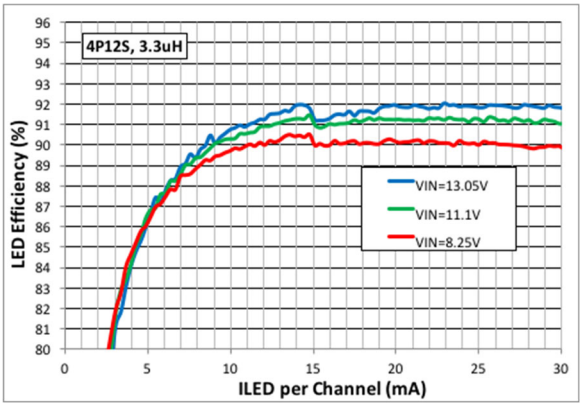


Figure 39. 3S, 4P12S LED Efficiency, 3.3 µH Inductor

LED Current Sinks

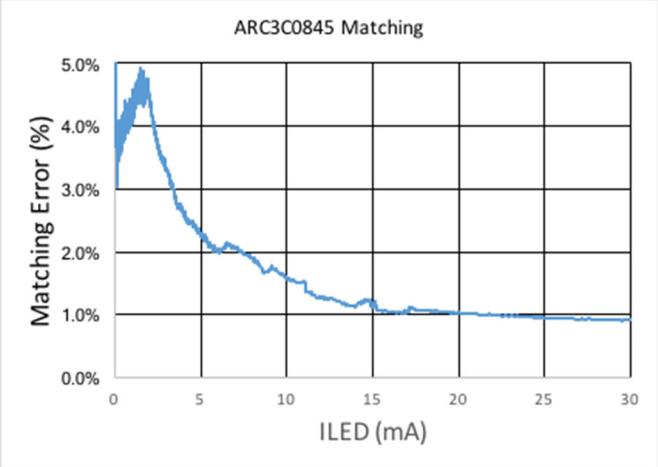


Figure 40. LED Mismatch in Linear Mode

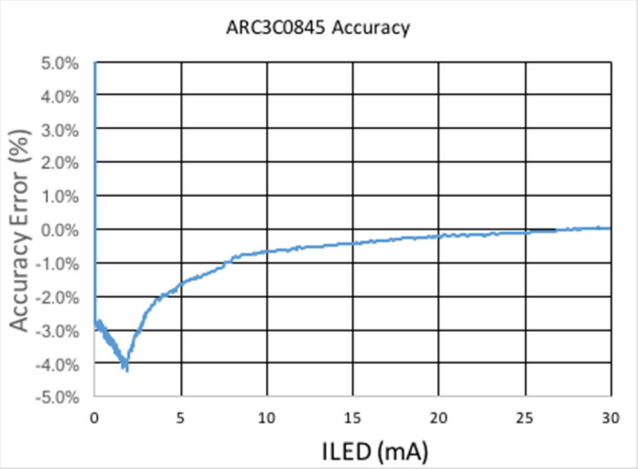


Figure 41. LED Accuracy in Linear Mode

Startup Characteristics

Figure 42–Figure 44 show the ARC3C0845/ARC3C0845W typical performance data with C_{OUT} = 4.7 µF, LED VF = 3V at 20 mA (typical), and analog dimming, unless otherwise specified.

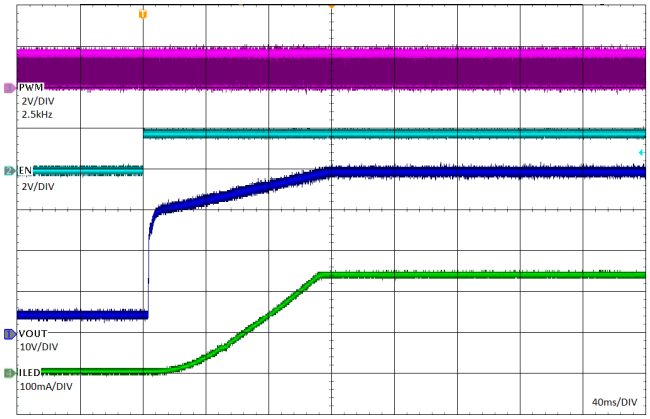


Figure 42. Startup Under 99% PWM Condition. 8P12S Configuration. V_{IN} = 7.4V, 3x Charge Pump Ratio.

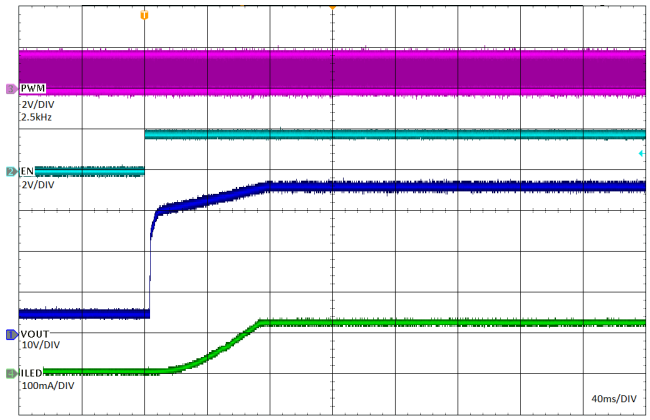


Figure 43. Startup under 50% PWM condition. 8P12S configuration. V_{IN} = 7.4V, 3x Charge Pump Ratio.

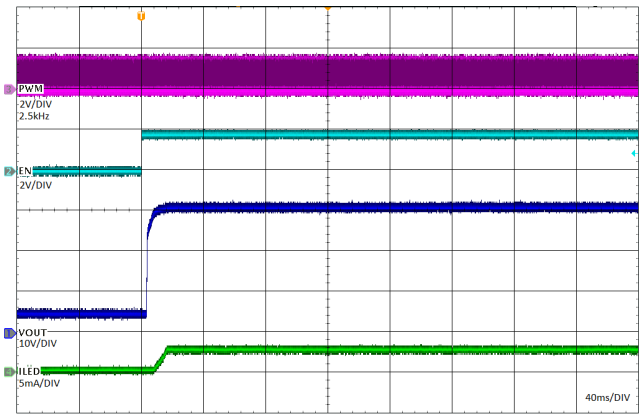


Figure 44. Startup under 1% PWM condition. 8P12S configuration. V_{IN} = 7.4V, 3x Charge Pump Ratio.

Thermal Performance

Figure 45–Figure 46 show the ARC3C0845/ARC3C0845W thermal performance data with C_{OUT} = 4.7 µF, LED VF = 3V at 20 mA (typical), and analog dimming, unless otherwise specified.

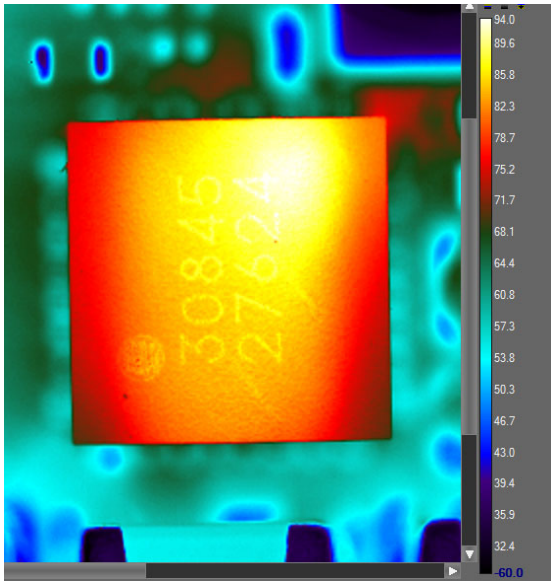


Figure 45. ARC3C0845 Thermal Performance

Conditions

- 8p12s configuration
- 38.5V V_{OUT}
- 240 mA
- 5.5V V_{IN}
- 1.5W power dissipation
- 1.2 mm 4.7-µH Inductor (DFE322512F-4R7M)
- Ambient temperature (T_A) is 23.7 °C
- Maximum temperature (T_{MAX}) is 94 °C close to the package LX and PGND pins

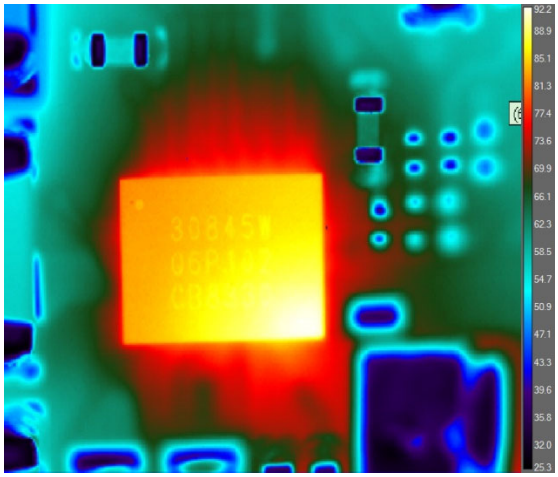


Figure 46. ARC3C0845W Thermal Performance

Conditions

- 8p12s configuration
- 37.5V V_{OUT}
- 240 mA
- 5.5V V_{IN}
- 1.45W power dissipation
- 1.2 mm 4.7-µH Inductor (DFE322512F-4R7M)
- Ambient temperature (T_A) is 23.5 °C
- Maximum temperature (T_{MAX}) is 92.2 °C close to the package LX and PGND bumps

Detailed Description

The ARC3C0845/ARC3C0845W uses a proprietary architecture with a charge pump driven by a synchronous boost converter to achieve high peak efficiencies and superior efficiency over the two-cell/three-cell lithium battery input voltage range. This architecture further realizes excellent performance across a range of LED forward voltages, allowing freedom in the LED selection.

The ARC3C0845/ARC3C0845W supports 1–8 LED strings. Tie unused LEDx pins to ground. This provides maximum design flexibility for wide variety of LCD screens.

The ARC3C0845/ARC3C0845W supports both I²C and non-I²C operation. It can be configured through the I²C interface or external settings and allows combined I²C command settings with the PWM signal to adjust the LED brightness.

The ARC3C0845/ARC3C0845W provides a full set of protection features to ensure robust system operation:

- Input voltage under-voltage lockout (UVLO)
- Thermal shutdown (TSD)
- Boost and charge pump over-current protection (OCP)
- Boost and charge pump output over-voltage and under-voltage protection (OVP and UVP)
- LED open and short detection

Input Sequencing Requirements

V_{DDIO} determines if the device starts up in I²C or non-I²C mode. This input must be taken high—for I²C mode—or low—for non-I²C mode—before both V_{IN} and EN are asserted. Do not leave V_{DDIO} floating. With V_{DDIO} already established, then both V_{IN} and EN can be asserted high to enable the internal VDD LDO. When V_{DD} is above the VDD UVLO threshold—3V typical—for ~100us, the ARC3C0845/ARC3C0845W detects the V_{DDIO} level to determine device is in I²C or non-I2C mode. Then the ARC3C0845/ARC3C0845W becomes operational. In I²C mode the first command can be given 1 ms after both V^{IN} and EN are asserted.

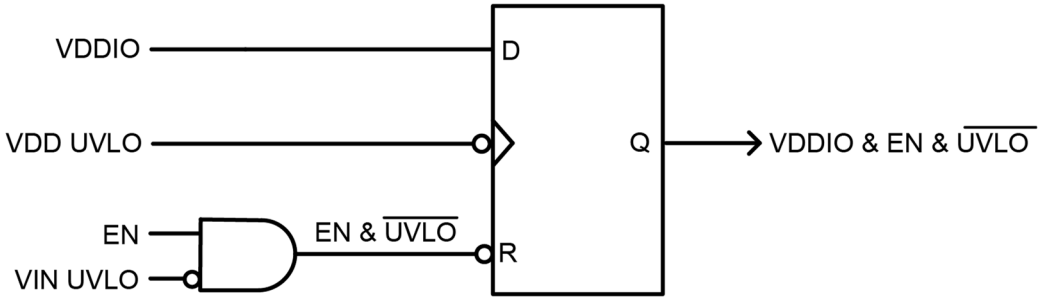


Figure 47. Input Sequencing Logic Diagram

If the part is enabled in non-I²C mode, connect V_{DDIO} to the GND plane with a low inductance trace. In I²C mode, connect V_{DDIO} to the same pull-up voltage used by the SDA and SCL signals because the SDA and SCL VIH and VIL are referenced to V_{DDIO}. If this voltage drops too low, I²C communication stops, but the device retains all its register values. I²C communication can resume 5 µs after V_{DDIO} becomes stable within its allowable voltage range.

In I²C mode, SCL and SDA serve as clock and data lines. In non-I²C mode, SCL can be used to select three different dimming modes and SDA can be used to select three different boost switching frequencies depending on whether the pins are logic low, logic high or floating.

The sequence for the PWM pin does not matter. It can be switched according to the application requirements while all other signals are being turned on and off. Table 7 lists the various ARC3C0845/ARC3C0845W input conditions.

Table 7. Input Conditions

V_{IN}	EN	V_{DDIO}	SCL	SDA	PWM	Device Status
Low	–	–	–	–	Switching	Non-operational
High	Low	–	–	–	Switching	Non-operational
High	High	High	Clock	Data	Switching	Non-operational

Note: A dash (–) indicates that the level can be high or low and does not affect operation.

Under-voltage Lockout (UVLO)

The ARC3C0845/ARC3C0845W continuously monitors the V_{IN} input. If the V_{IN} voltage drops below approximately 4.3V, the ARC3C0845/ARC3C0845W immediately shuts down.

Output Over-voltage and Under-voltage Protection

The ARC3C0845/ARC3C0845W protects against excessive output voltage by initiating over-voltage protection (VOUT_OVP) when VOUT rises above the over-voltage threshold V_{OUT_OVP}. When a VOUT OVP occurs, the VOUT_OVP bit of the STATUS1 register is updated to 1, and the ARC3C0845/ARC3C0845W turns off the boost converter. The boost converter automatically restarts after an OVP event when V_{OUT} decreases below the threshold plus 0.5V typical hysteresis.

The over-voltage threshold can be configured through the OVP_TH[3:0] bits in COMMAND register. The accuracy of each over-voltage threshold is ±5%.

Table 8. Over-voltage Threshold

VOUT_OVP_SEL[3:0]	V_{OUT} Over-voltage Threshold (V)
0000	47.5
0001	45.625
0010	43.75
0011	41.875
0100	40.0
0101	38.125
0110	36.25
0111	34.375
1000	32.5
1001	30.625
1010	28.75
1011	26.875
1100	25.0
1101	23.125
1110	21.25
1111	19.375

In non-I^2C mode, the OVP threshold is fixed at 47.5V—the factory default—but can be programmed to a different level in the non-volatile memory.

Select the output over-voltage threshold with enough voltage margin above the highest expected operating VOUT voltage in the application to ensure proper LED open or grounded string fault detection. The highest expected operating VOUT voltage is a function of the number of series LEDs used, the highest LED forward voltage expected, and the regulation voltage at the LED pins during the maximum LED current used in the application per channel.

Reset and Standby Functions

Table 9 lists the RESET and Standby states when the part uses the I²C interface. For all modes: UVLO high = POR IC (entire chip shutdown).

Table 9. I²C Interface RESET and Standby States

EN Pin Logic Level	I2C_STANDBY	LEDEN[8:1]	Reset	Status	Internal Block ON	Register
0	–	–	–	OFF	None	Cleared
1	0	0	0	Ready	References ON, Boost/CP off, LED drivers on standby	I²C accessible
1	0	>0	0	ON	All ON	I²C accessible
1	1	–	–	Standby	All off except UVLO + critical reference circuits	I²C accessible
1	0	–	1 (self-clearing)	Reset -> Ready (self-clearing)	Ready state after self-clearing reset	Cleared
Note: A dash (–) indicates that the level can be high or low and does not affect operation.						

The STATUS1 and STATUS2 register bits are all cleared upon read, so the repeated read-back of a logic-high fault bit indicates that the fault event remains persistent.

Boost Output Over-voltage and Under-voltage Protection

The ARC3C0845/ARC3C0845W monitors the boost output (VX) voltage by initiating over-voltage protection (VX_OV) when VX rises above a typical over-voltage threshold of 17V (3x charge pump ratio) or 22.25V (2x charge pump ratio). When a VX OVP occurs, the VX_OVP bit of the STATUS1 register is updated to a 1, and the ARC3C0845/ARC3C0845W turns off the boost converter. The boost converter automatically restarts after a VX_OV event when VX decreases below the VX_OV threshold plus a 0.5V typical hysteresis.

If the boost output voltage (VX) falls below the V_{IN} voltage plus a V_{IN} proportional offset after the LED current sinks have turned on, the ARC3C0845/ARC3C0845W shuts down the switching converter and the LED current sinks immediately and the VX_UV register bit in the STATUS1 register is set to 1. The switching converter and the LED current sinks remain latched off and do not start unless the part is shutdown or reset as listed in Table 9.

The ARC3C0845/ARC3C0845W can detect a missing or unconnected inductor upon startup by monitoring the boost output before enabling the switching converter and LED strings. When an inductor open is detected, the switching converter and LED strings remain off and the SS_TIMEOUT and VX_UV bits in the STATUS1 register are set and are cleared upon read.

Soft-Start Timeout

The ARC3C0845/ARC3C0845W implements a soft-start timeout fault. If the output voltage does not rise above 2x/3x of the input voltage within 10 ms, the switching converter and the LED current sinks are disabled. The SS_TIMEOUT bit in the STATUS1 register is set to 1. This is a latched fault. The ARC3C0845/ARC3C0845W does not start up until a reset event occurs, such as by toggling EN low or setting the RESET bit in the CONFIG4 register (which clears itself).

LED Short Protection

The ARC3C0845/ARC3C0845W includes a fault comparator on each LEDx pin to detect a shorted LED condition. This comparator enables when at least one LED pin is in regulation and the shorted LED fault is triggered when an LEDx voltage rises above the shorted LED voltage threshold. The shorted LED voltage threshold can be programmed to 4.35V, 4.85V, 5.25V, and 5.75V by using the CONFIG3 register LED_SHORT_VTH[1:0] bits. This fault condition can occur when some LEDs in a string are electrically bypassed, making that LED string shorter than the other LED strings.

The reduced forward voltage causes the current sink attached to that string to have a higher voltage than other current sinks, which could cause overheating of that current sink. When this fault is detected, the faulty current sink is disabled, and an LED short fault is recorded in the STATUS1 register. The faulty current sink can only be re-enabled by turning off all LED current sinks first, or if a reset event occurs.

LED Open Circuit Protection

When one of the LED strings is open, the output rises until it crosses the VOUT OVP threshold. Any string under-regulation at that moment is blocked from controlling V_{OUT}, resulting in the output decreasing to a level needed to regulate the remaining non-open LED strings. An LED open fault is recorded in the STATUS2 register.

If the open LED string is reconnected, the LED current sink re-establishes the current to the level based on the output voltage, but it is not allowed to control the V_{OUT} voltage. To re-enable the output control for any faulted strings, turn off all LEDs or reset the part.

Over-current and Short Circuit Protection

The boost converter has a cycle-by-cycle over-current limit. It starts up initially with a derated over-current limit of 1.0A typically for soft start. The cycle-by-cycle over-current limit can be programmed to 1A, 2A, 3A, or 4A by using the CONFIG1 register BOOST_ILIM[1:0] bits. The boost low-side switch turns off when the inductor current reaches the current limit threshold and remains off until the beginning of the next switching cycle. This fault is not reported in the STATUS1 or STATUS2 registers.

For more severe over-current faults in which the cycle-by-cycle over-current limit cannot prevent the inductor current from continuing to ratchet up, a secondary over-current protection is implemented. When the inductor current through the boost low-side switch exceeds the secondary current limit—which is 2A above the programmed BOOST_ILIM[1:0] setting—the converter and the LED current sinks are disabled immediately. The STATUS1 register BST_ILIM_SEC bit is set and is cleared upon read. The switching converter and the LED current sinks remain latched off and do not restart unless the part is shutdown or reset.

A separate short-circuit detection is implemented if the output voltage drops suddenly, forcing a large current out of the charge pump. The output is disconnected from the charge pump and the LED current sinks are temporarily disabled. The boost and charge pump remain switching, regulating at the last-known voltage level. The STATUS1 register DISC_OCP bit is set. The LED current sinks are enabled again when the fault at the VOUT pin is removed.

Current Setting

In I²C mode, the LED output maximum currents are set by the CONFIG2 register MAX_I[4:0] bits. The default maximum current is 43 mA per LED string with 31 further settings available: 12 mA to 43 mA in 1 mA increment per step.

Fine-tuning of the maximum current of the LED outputs can be set by the VREG_IMAXTUNE register IMAXTUNE[3:0] bits. This allows incremental increases in the maximum output current from the MAX_I[4:0] setting mentioned above, in 4-bit resolution (16 steps) ranging from 0% to 7.66% with an average of 0.51% per step. Using IMAXTUNE[3:0] to increase the maximum output current from these default values can result in some loss of accuracy.

Table 10. Current Settings

MAX_I[4:0]	Full-scale ILED Current (ISET_EXT = 0)	KISET Current Multiplier	MAX_I[4:0]	Full-scale ILED Current	KISET Current Multiplier (ISET_EXT = 1)
00000	12 mA	400.00	10000	28 mA	933.33
00001	13 mA	433.33	10001	29 mA	966.66
00010	14 mA	466.67	10010	30 mA	999.99
00011	15 mA	500.00	10011	31 mA	1033.33
00100	16 mA	533.33	10100	32 mA	1066.66
00101	17 mA	566.67	10101	33 mA	1099.99
00110	18 mA	600.00	10110	34 mA	1133.33
00111	19 mA	633.33	10111	35 mA	1166.66
01000	20 mA	666.66	11000	36 mA	1199.99
01001	21 mA	700.00	11001	37 mA	1233.33
01010	22 mA	733.33	11010	38 mA	1266.66
01011	23 mA	766.66	11011	39 mA	1299.99
01100	24 mA	800.00	11100	40 mA	1333.32
01101	25 mA	833.33	11101	41 mA	1366.66
01110	26 mA	866.66	11110	42 mA	1399.99
01111	27 mA	900.00	11111	43 mA	1433.32

In addition, the maximum current can be adjusted by an external resistor, R_{ISET}, connected between ISET pin and ground, when the CONFIG3 register ISET_EXT bit is set to 1. R_{ISET} controls the full-scale LED current in conjunction with the current determined by the MAX_I register bits as follows:

$$I_{LED\_FULL} = \frac{0.4}{R_{ISET}} * K_{ISET}$$

The R_{ISET} range is 13.3 KΩ to 133 KΩ. In PWM mode, the output current of the LED can be calculated from the duty cycle of the PWM input as follows:

$$I_{LED} = \frac{0.4}{R_{ISET}} * K_{ISET} * PWM\ Duty\ Cycle$$

In non-I²C mode, the above formula applies with KISET = 999.99 by default. KISET can be changed by re-programming MTP[

Boost Converter Switching Frequency

The ARC3C0845/ARC3C0845W boost converter provides wide frequency selection to meet different application requirements. Four bits set the boost switching frequency(f_{SW_BOOST}), which are the CONFIG1 register FSW_BOOST[4:0] bits, as listed in Table 11.

In non-I^2C mode, the boost switching frequency is set by the SDA pin, which is sampled once at startup. Changing the SDA pin bias after boost switching has started does not change the boost switching frequency. Table 12 lists the boost switching frequency settings through the I^2C register value and SDA pin in both I^2C and non-I^2C modes.

The choice of inductor, charge pump fly capacitors, and compensation components depend on the selected boost switching frequency for proper part operation. For the recommended component types and values, contact pSemi.

Table 11. Boost Switching Frequency Settings

Freq (kHz)	FSW_BOOST[4:0] Binary Code	Non-I2C SDA Pin	Freq (kHz)	FSW_BOOST[4:0] Binary Code	Non-I2C SDA Pin
3413	00010	–	569	10001	–
2560	00011	–	539	10010	–
2048	00100	–	512	10011	Tie to AGND
1707	00101	–	488	10100	–
1463	00110	–	465	10101	–
1280	00111	–	445	10110	–
1138	01000	Tie to VDD	427	10111	–
1024	01001	–	410	11000	–
931	01010	–	394	11001	–
853	01011	–	379	11010	–
788	01100	–	366	11011	–
731	01101	Floating	353	11100	–
683	01110	–	341	11101	–
640	01111	–	330	11110	–
602	10000	–	320	11111	–

Table 12. Non-I^2C Mode Boost Switching Frequency Settings

SDA Configuration	Frequency (kHz)
SDA shorted to VDD pin	1138
SDA open	731
SDA shorted to AGND pin(*)	512
Note: * Depends on the FSW_BOOST[4:0] bits default setting.	

Charge Pump Switching Frequency

Table 13 lists the default relationship between the LED brightness setting and the charge-pump frequency ratio from the boost switching frequency. The charge-pump frequency ratio and relationship to the LED brightness setting are programmable using the CONFIG_CP register CP_FREQ_TRAN, SEL_CP_FREQ, and CP_FREQ_DIV[1:0] bits, as described on page 58.

Table 13. Charge-Pump Frequency Ratio

CP_FREQ_TRAN	SEL_CP_FREQ	CP_FREQ_DIV[1]	CP_FREQ_DIV[0]	CP Frequency Ratio
0	0	X	X	1/8 at <50% LED brightness 1/4 between ≥50% and <75% LED brightness 1/2 at ≥75% LED brightness
0	1	0	0	1/2 across entire LED brightness range
0	1	0	1	1/4 across entire LED brightness range
0	1	1	0	1/8 across entire LED brightness range
0	1	1	1	1/8 across entire LED brightness range
1	X	X	0	1/4 at <50% LED brightness 1/2 at ≥50% LED brightness
1	X	X	1	1/8 at <50% LED brightness 1/4 at ≥50% LED brightness

Switching Converter Compensation

The switching converter operates in voltage-mode control and uses Type-III compensation, which requires three external components, as shown in Figure 48.

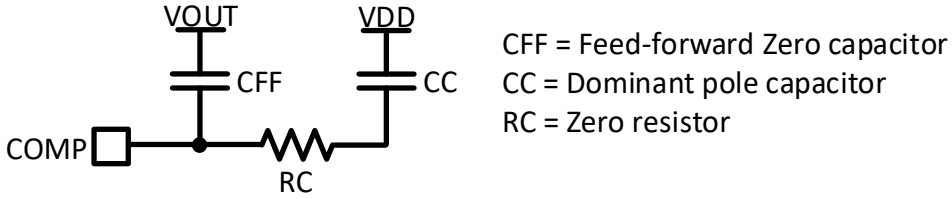


Figure 48. Compensation Components

Table 14 lists the recommended compensation component selection for different inductor values. The SEL_VR[2:0] bits set the control loop DC gain.

For a more specific set of compensation components to optimize the bandwidth and phase margin for your application, contact pSemi.

Table 14. Compensation Components

Inductor Value	RC Value	CC Value	CFF Value	SEL_VR[2:0] Setting
2.2 µH	680Ω	10 nF	220 pF	111
3.3 µH	820Ω	10 nF	220 pF	111
4.7 µH	1kΩ	10 nF	220 pF	111
6.8 µH	1.2kΩ	10 nF	220 pF	111
10 µH	1.5kΩ	10 nF	220 pF	111

LED Current Output Dimming

The ARC3C0845/ARC3C0845W supports four LED current output dimming options for maximum application flexibility in choosing among low noise, converter efficiency, optical efficiency, and minimal WLED color shift at low brightness levels. These options are analog, phase-shift PWM, hybrid PWM (mixed-mode), and direct PWM (DPWM) dimming.

Analog Dimming

In I^2C mode, when the CONFIG2 register DIM_MODE bit is set to 0, dimming is set to analog only. In analog dimming, the LED current sink output is always a DC current across the entire brightness range. As the brightness is reduced, the LED current sink output DC level decreases, which also decreases the LED forward voltage. The adaptive output voltage regulation loop decreases the V_{OUT} voltage at the top of the LED strings, which can also reduce power dissipation in the switching converter. Operating the LEDs with a DC current output also minimizes noise in the system.

When using a non-I^2C interface, the analog dimming mode is selected by floating the SCL pin. The full-scale output current per channel can be scaled using an external resistor, R_{ISET}, connected between the ISET pin and analog ground. The tolerance of the external resistor R_{ISET} directly affects the accuracy of the LED current sink output, so using a precision resistor is recommended. The recommended R_{ISET} resistor range is 13.3kΩ to 133kΩ, with 13.3kΩ corresponding to 43 mA full-scale current output per channel with the MAX_I[4:0] bits set to 11111.

Phase-shift PWM Dimming

In I^2C mode, when the CONFIG2 register DIM_MODE bit is set to 1, PWM dimming is enabled. In this mode, the mixed dimming block generates phase-shifted PWM signals to dim the active LED strings when the required LED current is below the threshold set by the PWM_IX[1:0] register bits. The phase difference between the active strings is automatically adjusted to 360 degrees divided by the number of active strings. This phase shifting reduces noise in the audio band.

When the LED current outputs are PWM dimming, their switching frequency can be selected from one of five frequency settings between 2.5 kHz and 40 kHz using the PWM_DIM_FREQ[2:0] register bits. When using a non-I^2C interface, the PWM dimming frequency of the LED current outputs is 2.5kHz—the factory default—with the SCL pin grounded. For alternate frequency options or to reprogram the MTP, contact pSemi.

Hybrid PWM (Mixed-mode) Dimming

The ARC3C0845/ARC3C0845W allows a mixed dimming output scheme for better optical efficiency. The switch point from analog to PWM dimming is set by register bits DIM_MODE=1 and PWM_IX[1:0], and can be 12.5%, 25%, 50%, or 100% of the brightness range. 100% means that PWM dimming is used across the whole brightness range. In the brightness range above the switch point, analog dimming is adopted, and below the switch point, PWM dimming is adopted. With this arrangement, good optical efficiency at low brightness levels is achieved while minimizing system noise at higher brightness levels.

- PWM_IX[1:0] = 11 results in a DC output current only when the LED brightness setting is at 100%, otherwise the LED current sink switches off and on to 100% of its full-scale output level.
- PWM_IX[1:0] = 10 results in a DC output current only when the LED brightness setting is at 50% or greater, otherwise the LED current sink switches off and on to 50% of its full-scale output level.
- PWM_IX[1:0] = 01 results in a DC output current only when the LED brightness setting is at 25% or greater, otherwise the LED current sink switches off and on to 25% of its full-scale output level.
- PWM_IX[1:0] = 00 results in a DC output current only when the LED brightness setting is at 12.5% or greater, otherwise the LED current sink switches off and on to 12.5% of its full-scale output level.

Figure 49 shows an example of the LED current output for any one channel at the PWM_IX[1:0] = 01 setting.

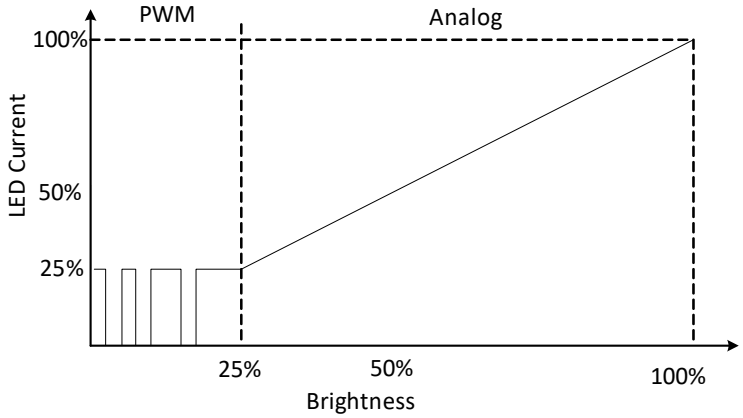


Figure 49. Mixed-mode Dimming

The choice of four brightness transition points between analog dimming and PWM dimming at the LED current sink output provides flexibility in optimizing between good optical efficiency and good matching of the LED brightness and color shift. Because the LED current output peak during PWM dimming scales proportionally with the brightness transition point, the LED current pulse width also must scale inversely for a given brightness setting. For example, at a 10% LED brightness setting, the LED current pulse width at PWM_IX[1:0] = 01 (25% transition point) is four times longer than at PWM_IX[1:0] = 11 (PWM-only dimming) to get an equivalent output brightness. The minimum controllable LED current on pulse or off pulse is typically 200 ns.

In non-I^2C mode, when the SCL pin is grounded, the mixed dimming control scheme is enabled and the brightness transition point between analog dimming and PWM dimming is 25% (factory default).

In non-I²C mode, the SCL pin selects the LED output dimming options, and is sampled once at startup. Changing the SCL pin bias after boost switching has started does not change the LED dimming scheme. Table 15 lists the SCL pin setting and dimming scheme in non-I²C mode.

Table 15. SCL Pin Setting and Dimming Scheme

SCL Pin(1)	Dimming Scheme
Tied to the AGND pin(2)	Mixed dimming with 25% transition point
Floating	Analog dimming
Tied to the VDD pin	Direct PWM dimming

Notes:
1. Do not set DIMCODE[1:0] to 11 as the default setting.
2. Depends on the DIM_MODE bit default setting.

Direct PWM (DPWM) Dimming

The brightness is directly proportional to the duty cycle applied at the PWM pin. The LED current outputs are no longer phase-shifted but are synchronized with the timing edges at the PWM pin.

In I²C mode, when the DIMCODE[1:0] register bits are set to 11, the direct PWM dimming mode is selected. In non-I²C mode, tying the SCL pin to the VDD pin selects direct PWM dimming.

In direct PWM dimming mode, the input PWM signal switches the LED strings on and off directly, with the LED current on when PWM is high. The mixed dimming block is bypassed, and there is no phase shift among the LED strings. The minimum PWM pulse width allowed under direct PWM dimming is 200 ns. In this mode, the PWM input frequency range is 200 Hz to 20 KHz.

LED Current Full-scale or 100% Brightness

The maximum LED Current full-scale can be programmed using either I²C or an external resistor, both of which provide for fine tuning. For details, see Current Setting on page 33.

LED Brightness Control

In I²C mode, the LED brightness is controlled by the duty cycle of the PWM input signal, the WLED_ISET_MSB and WLED_ISET_LSB registers written through the I²C interface, or both. The DIMCODE[1:0] register bits select the four different brightness control options described in this section.

DIMCODE = 00

When DIMCODE = 00, the LED current is controlled only by the PWM input duty cycle. The PWM detector block extracts the duty cycle of the PWM input signal. The duty cycle goes through a mapping to generate a DC current level or phase-shifted PWM currents at the LED strings.

When the I²C interface is not used, LED dimming is controlled by the PWM input only, with the full-scale current set by the resistor on the ISET pin.

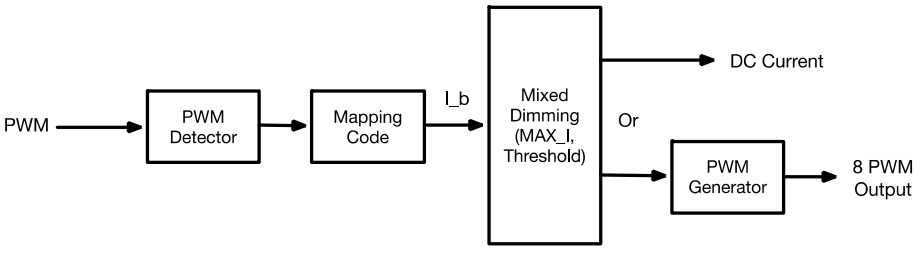


Figure 50. DIMCODE = 00

DIMCODE = 01

When DIMCODE = 01, the LED current is controlled by the WLED_ISET_MSB and WLED_ISET_LSB registers through the I²C interface. The register codes go through a mapping first, then through the mixed dimming block to generate a DC current level or eight phase-shifted PWM currents at the LED strings. To update the 12-bit dimming value, write to the WLED_ISET_LSB register, then write to the WLED_ISET_MSB register.

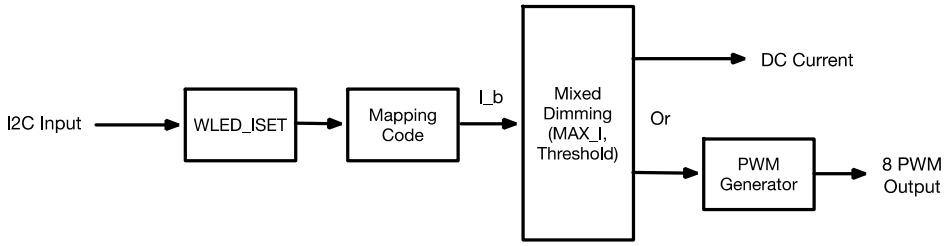


Figure 51. DIMCODE = 01

DIMCODE = 10

When DIMCODE = 10, the LED current is controlled by the PWM input duty cycle and the WLED_ISET_MSB and WLED_ISET_LSB register values through the I²C interface. The register codes go through a mapping first and are then multiplied by the PWM-based brightness code. After multiplication, the resulting code goes into the dimming block to generate a DC current level or eight phase-shifted PWM currents.

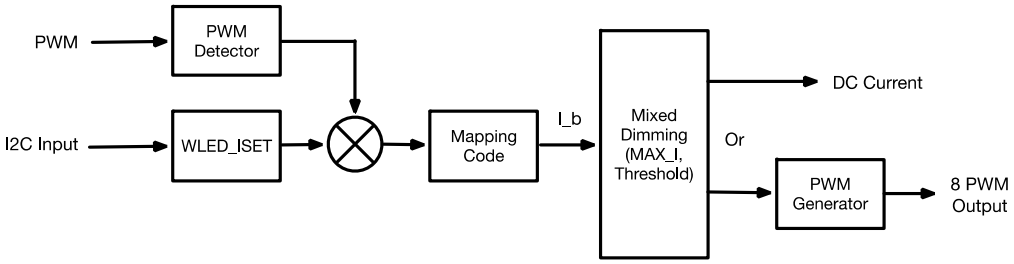


Figure 52. DIMCODE = 10

DIMCODE = 11

When DIMCODE=11, direct PWM dimming is enabled. Under this setting, the input PWM signal turns the active LED strings on and off directly while the internal decoding circuitry and mixed dimming block are bypassed. The minimum input PWM pulse width is limited to 200 ns under direct PWM dimming. The LED current at each string switches from zero current to the full-scale current level set by the MAX_I[4:0] bits and, if used, the external ISET resistor.

Linear and Logarithmic Mapping

In linear mapping mode, the dimming settings presented either through the PWM input or WLED_ISET_MSB and WLED_ISET_LSB registers are translated linearly into the LED current. This is the factory default setting. There are 4095 possible brightness states in this mode with the dither function disabled (DITHER_ENABLE bit = 0), and 32767 possible brightness states with the dither function enabled (DITHER_ENABLE bit = 1).

For a better visual experience, the ARC3C0845/ARC3C0845W can also translate the dimming settings using a logarithmic mapping to produce the LED current. To enable this feature, set the CONFIG2 register LOG_MODE bit to 1. There are 1023 possible brightness states in this mode with the dither function disabled (DITHER_ENABLE bit = 0), and 8191 possible brightness states with the dither function enabled (DITHER_ENABLE bit = 1).

With the dither function enabled, the ARC3C0845/ARC3C0845W uses the DITHER_LSB[2:0] bits combined with WLED_ISET_MSB[11:4] and WLED_ISET_LSB[3:0] to form a 15-bit LED output current setting, where the DITHER_LSB[2:0] bits become the lower LSBs. You can then write to the eight MSBs in register 0x06 first, then the 7 LSBs in register 0x05, for a 15-bit resolution LED dimming adjustment.

Operation with DIMCODE = 00 or 10

In these modes, the ARC3C0845/ARC3C0845W PWM input frequency range is 200 Hz to 40 KHz. The input frequency is independent of the PWM output frequency, which is the 8-phase LED current switching frequency. In I^2C mode, the PWM output frequency is set by the PWM_DIM_FREQ[2:0] register bits. In non-I^2C mode, the PWM output frequency defaults to 2.5 kHz with the SCL pin grounded.

Because the on-chip clock is 10.24 MHz, a full 12-bit PWM input resolution can obtained with a ≤2.5 kHz PWM input signal (10.24 MHz/2^{12} = 2.5 kHz). Higher PWM input frequencies reduce thePWM input resolution, with eight bits of PWM input resolution available at 40 kHz.

The same resolution limitation occurs with the PWM output frequency. This effect is most pronounced with 100% PWM dimming (PWM_IX[1:0] = 11) with eight bits of dimming resolution. When using 25% PWM dimming, a 40-kHz PWM output frequency provides ten bits of dimming resolution relative to the full-scale LED output current.

For 12-bit brightness control, the PWM generator uses register 0x06 as the MSB portion mapped as bits [11:4] and the upper nibble of register 0x05 as the LSB [3:0] in the 12-bit value. The LED intensity is updated at the start of every LED output PWM cycle with the frequency set by the PWM_DIM_FREQ[2:0] bits.

In general, the dimming resolution at the LED current output is related to the PWM dimming frequency and the hybrid transition point, with a higher resolution achieved with a lower PWM dimming frequency and lower transition point. For example, for a 25% transition point, a 12-bit resolution is possible at the 10 kHz PWM_DIM_FREQ[2:0]=010 setting or lower, an 11-bit resolution is possible at the 20 kHz PWM_DIM_FREQ[2:0]=011 setting, and so on. This example is based on I^2C control when the PWM input frequency is ≤2.5 kHz.

The ARC3C0845/ARC3C0845W provides a dithering function by increasing the dimming resolution above 12 bits. With the DITHER_ENABLE bit set to 1, the dimming resolution increases by 15 bits by using the DITHER_LSB[2:0] bits as the lower three LSB. These three LSB bits combine with the WLED_ISET[11:0] bits to provide 15 bits of dimming resolution. Figure 53 and Figure 54 show how the register bits are used.

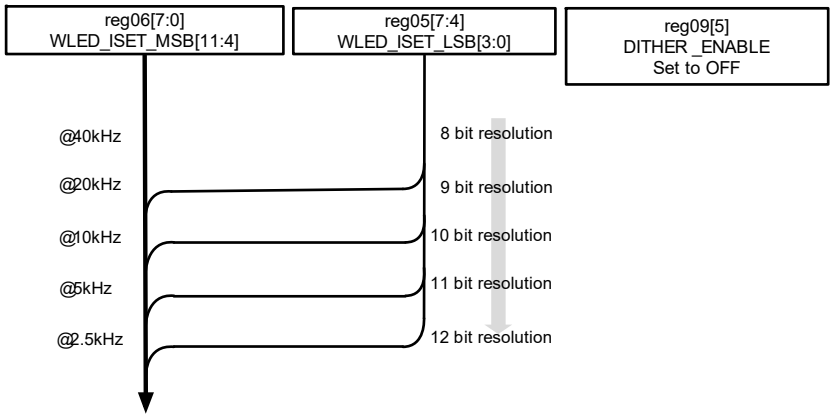


Figure 53. Relationship Between Frequency and Resolution in Phase Shift PWM Dimming with Dither OFF

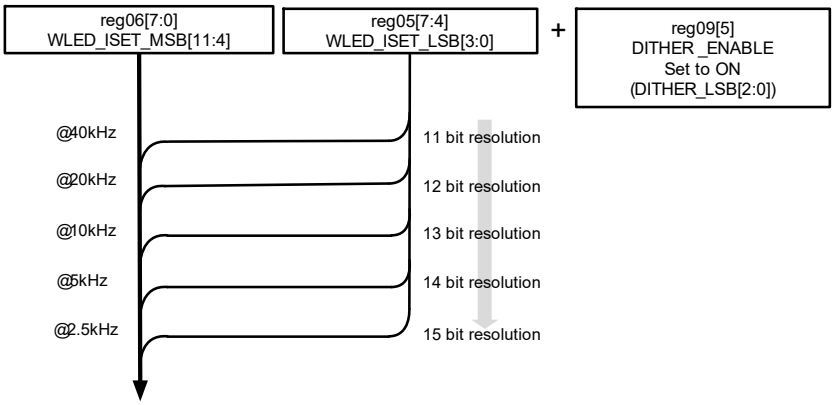


Figure 54. Relationship Between Frequency and Resolution in Phase Shift PWM Dimming with Dither ON

Fade In/Out Control

The fade in/out control makes a smooth transition from one brightness value to another for a better human eye experience. The ARC3C0845/ARC3C0845W provides extensive selection of the time for brightness changes from one level to another. The fading speed is selected by the FADING_SPEED register FADING_SPEED[7:0] bits. This register can set the speed from 50 µs/step (0x01) to 12.75 ms/step (0xFF) or disabled (0x00), based on your preference. For details, see the FADING_SPEED register on page 49.

In non-I^{2}C mode, FADING_SPEED defaults to 0x00.

Digital R-C Filter Mode Brightness Change

Due to the variability in the rate of consecutive discrete input brightness changes, it is not possible to select a single fading speed and still produce a visibly smooth output brightness change for all use cases. To resolve this issue, an RC-filter is used to filter the output brightness change response to each input brightness change.

The FILTER_SETTING register RCFILTER[1:0] bits control the coefficient of this RC time constant—as shown in Table 16—for a specific case of brightness changes between 1% and 99%. The RC filter coefficient is independent of the PWM_DIM_FREQ[2:0] frequency settings. The RCFILTER[1:0] bits are available in I^{2}C mode through the FILTER_SETTINGS register.

Table 16. RC Filter Settings

RCFILTER[1:0]	RC Time Constant (T)
00	Disabled
01	417 ms
10	207 ms
11	103 ms

Input PWM Filter for Non-DPWM Mode

When a duty cycle is applied at the PWM pin to control brightness, the on-time and period are sampled by the internal 10.24 MHz master clock to translate time-domain information into binary values. As inherent with any sampling of an asynchronous signal, the sampled binary values can jitter by ±1 LSB at steady-state, which translates into jitter on the final brightness result, and this can be visible as flicker. Adding some basic filtering to this sampled system can help to eliminate this flicker at steady-state.

The FILTER_SETTING register PWMFILTER[2:0] bits enable or disable this filter and control the amount of filtering. Furthermore, the filtering depends on the direction of the sampled PWM time-step, as follows:

- If the PWM time-step has been decreasing, the sampled binary value is allowed to decrement regardless of the delta time-step size but prevented from incrementing unless the delta time-step size is greater than or equal to the programmed filter threshold.
- If the PWM time-step has been increasing, the sampled binary value is allowed to increment regardless of the delta time-step size but prevented from decrementing unless the delta time-step size is greater than or equal to the programmed filter threshold.

The time-step size is 700 ns.

Table 17. PWM Filter Settings

PWMFILTER[2:0]	Minimum PWM Time-step Size
000	Off
001	2 steps
010	4 steps
011	6 steps
100	8 steps
101	10 steps
110	12 steps
111	14 steps

I²C Interface Bus Overview

The I²C bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both the SDA and SCL lines are pulled high. All the I²C-compatible devices connect to the I²C bus through the open drain I/O pins, SDA, and SCL. A master device such as a microcontroller or a digital signal processor controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives or transmits data on the bus under control of the master device.

The ARC3C0845/ARC3C0845W operates as a slave and supports the following data transfer modes, as defined in the I²C-Bus specification:

- Standard mode (100 kbps)
- Fast mode (400 kbps)
- Fast mode plus (1 Mbps)

The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as the V_{IN} voltage remains above UVLO and the EN pin remains asserted.

The data transfer protocol for standard and fast modes is the same, so they are referred to as F/S-mode in this document. The ARC3C0845/ARC3C0845W supports 7-bit addressing; 10-bit addressing and general call address are not supported. The device 7-bit address is defined as ‘0110XXX‘.

Programming the I²C Slave Address - Multiple Parts on One I²C Bus

To enable multiple ARC3C0845/ARC3C0845W parts to be addressed on one I²C bus, the lower three bits of the I²C slave address are programmable by using the ADDR pin. Table 18 lists the ADDR pin configuration to the device 7-bit address.

Table 18. ADDR Pin Configuration

ADDR Pin	Device 7-Bit Address
Tied to AGND	0110000 (0x30)
Floating	0110010 (0x32)
Tied to VDD	0110101 (0x35)

Standard-, Fast-, and Fast-Mode Plus Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 55. All I²C-compatible devices must recognize a start condition.

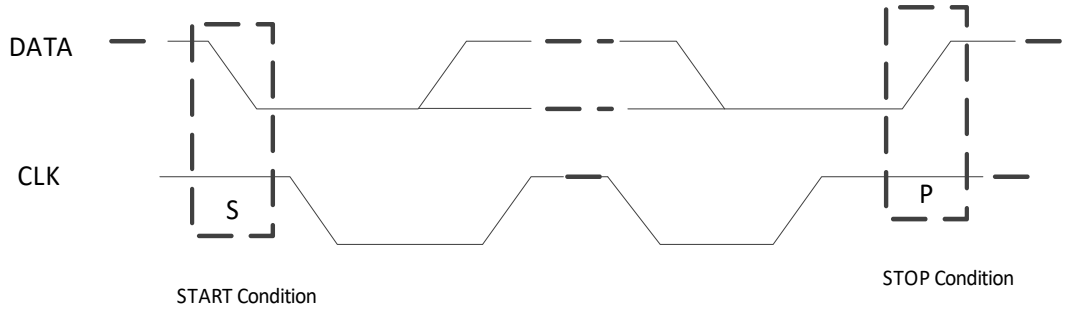


Figure 55. START and STOP Conditions

The master then generates the SCL pulses and transmits the 7-bit address and the read/write direction bit $R/\overline{w}$ on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 56). Only the slave device with a matching address generates an acknowledge (see Figure 57) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that a communication link with a slave has been established.

The master generates further SCL cycles to either transmit data to the slave ($R/\overline{w}$ bit 0) or receive data from the slave ($R/\overline{w}$ bit 1). In either case, the receiver must acknowledge the data sent by the transmitter. So, an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. Nine-bit valid data sequences consisting of 8-bit data and a 1-bit acknowledge can continue as long as needed.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 55). This releases the bus and stops the communication link with the addressed slave. All I²C-compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.

Attempting to read data from register addresses not listed in this section result in FFh being read out.

ARC3C0845/ARC3C0845W I²C Update Sequence

The ARC3C0845/ARC3C0845W requires a start condition, a valid I²C address, a register address byte, and a data byte for a single update. After the receipt of each byte, the ARC3C0845/ARC3C0845W acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the ARC3C0845/ARC3C0845W. The ARC3C0845/ARC3C0845W performs an update on the falling edge of the acknowledge signal that follows the LSB.

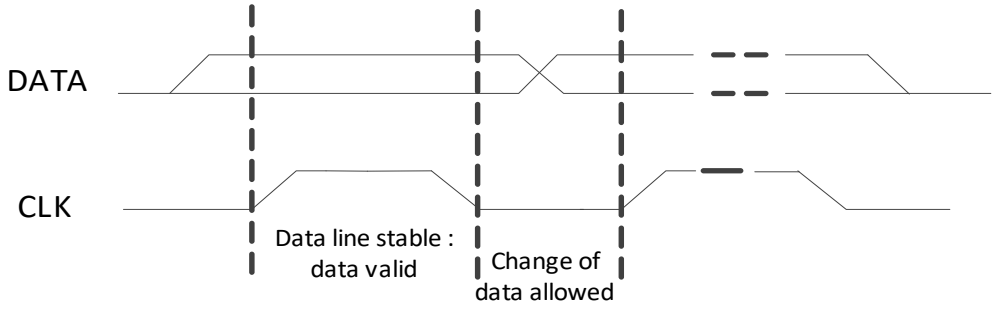


Figure 56. Bit Transfer on the Serial Interface

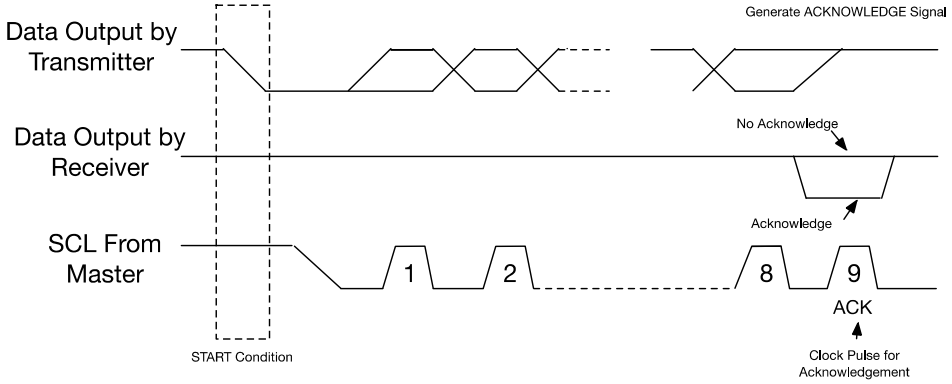


Figure 57. Acknowledge on the I²C Bus

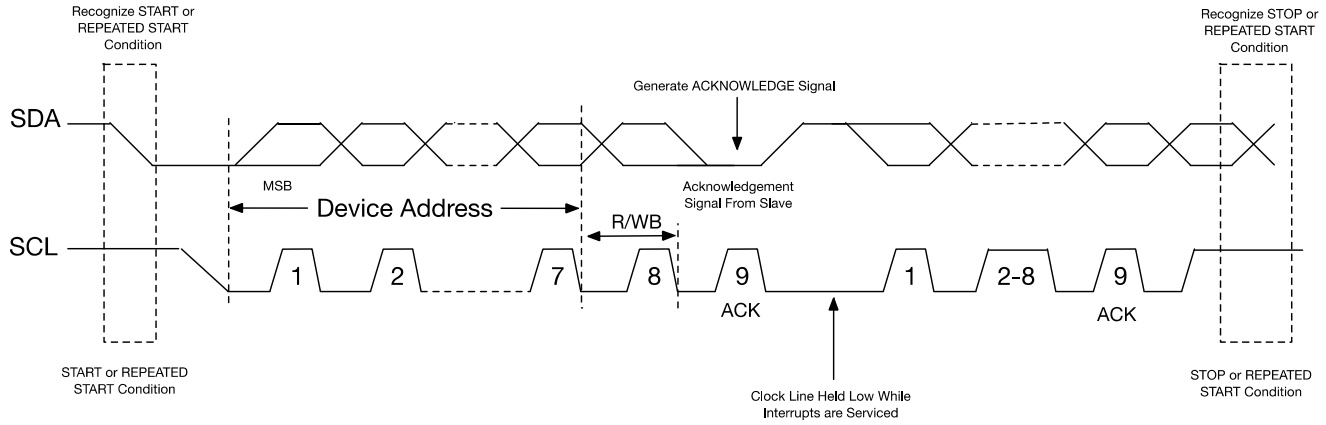


Figure 58. Bus Protocol

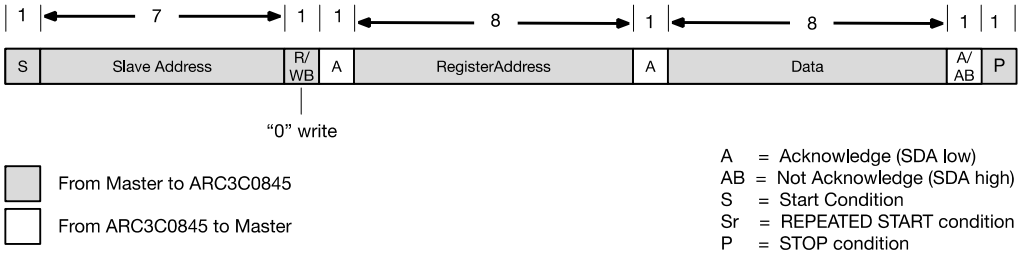


Figure 59. “Write” Data Transfer Format in Standard, Fast, Fast-Plus Modes

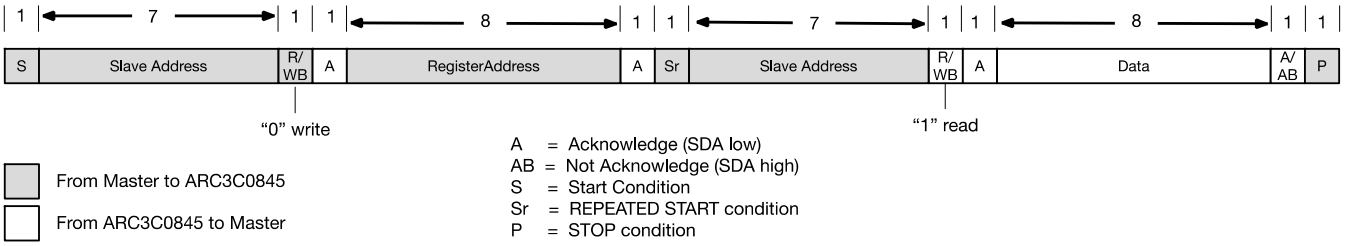


Figure 60. "Read” Data Transfer Format in Standard, Fast, Fast-Plus Modes

ARC3C0845/ARC3C0845W MTP Non-volatile Memory Description

The ARC3C0845/ARC3C0845W contains non-volatile memory (NVM) to store the default values for registers 0x00–0x0B. The NVM data is recalled to the registers at the device POR event. This function saves system initialization time by allowing you to program the device default setting in the production line instead of programming these settings after every POR event. To perform the MTP programming cycle, first write the preferred values for registers 0x00–0x0B. Then set the MTP_WRITE_CMD[4:0] bits to 10010 to initialize the MTP programming. During the MTP programming cycle, the MTP_WRITE_CMD[4:0] bits remain at 10010 and the MTP_WRITE_DNE bit is at 0. When the MTP programming cycle completes, the MTP_WRITE_CMD[4:0] bits automatically reset back to 00000 and the MTP_WRITE_DNE bit is set to 1. The MTP programming cycle takes 50 ms maximum to complete. To avoid data corruption, do not write to registers 0x00–0x0B during the MTP programming cycle.

Register Maps

Slave Address: 0110000 (0x30)

Register Configuration Parameters*

Register	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
COMMAND	0x00	SEL_VR[2:0]			BOOST_ MODE	OVP_TH[3:0]			
CONFIG1	0x01	Reserved	BOOST_ILIM[1:0]		FSW_BOOST[4:0]				
FADING_ SPEED	0x02	FADING_SPEED[7:0]							
CONFIG2	0x03	Reserved	LOG_MODE	DIM_MODE	MAX_I[4:0]				
LEDEN	0x04	LEDEN_8	LEDEN_7	LEDEN_6	LEDEN_5	LEDEN_4	LEDEN_3	LEDEN_2	LEDEN_1
WLED_ISET_ LSB	0x05	WLED_ISET_LSB[3:0]				DITHER_LSB[2:0]			Reserved
WLED_IST_ MSB	0x06	WLED_IST_MSB[11:4]							
CONFIG3	0x07	ISET_EXT	LED_SHORT_VTH[1:0]		PWM_IX[1:0]		PWM_DIM_FREQ[2:0]		
CONFIG4	0x08	I2C_ STANDBY	Reset	Reserved					
FILTER_ SETTINGS	0x09	DIMCODE[1:0]		DITHER_ ENABLE	RCFILTER[1:0]		PWMFILTER[2:0]		
VREG_ IMAXTUNE	0x0A	LED_VREG_CNT_INIT[3:0]				IMAXTUNE[3:0]			
CONFIGCP	0x0B	AUTO_CP_ RATIO	SEL_CP_ RATIO	Reserved	Reserved	CP_FREQ_ TRAN	SEL_CP_ FREQ	CP_FREQ_DIV[1:0]	
CKSUM0	0x0C	CHKSUM0[7:0]							
CKSUM1	0x0D	CHKSUM1[7:0]							
STATUS1	0x0E	BST_ILIM_ SEC	VOUT_OVP	VX_OV	VX_UV	DISC_OCP	TSD	SS_ TIMEOUT	LED_ SHORT
STATUS2	0x0F	MTP_WRITE_CMD[4:0]					MTP_WRITE _DNE	CRC_OK	LED_OPEN

Note: * ADDR pin tied to GND. Excluding read/write bit. 01100000 (0x60) if including the read/write bit.)

Detailed Register Description

Register COMMAND

Address	Name	POR Value(*)
0x00	COMMAND	0xE0

Bit Assignment

7	6	5	4	3	2	1	0
SEL_VR[2:0]			BOOST_MODE	OVP_TH[3:0]			

Bit Description

Field Name	Bits	Type	POR(*)	Description
SEL_VR[2:0]	[7:5]	$R/\overline{w}$	111	3-bit selection of control loop DC GAIN: From the highest (000) to the lowest (111) in 2-dB increments. For the recommended setting, see Switching Converter Compensation on page 35.
BOOST_MODE	[4]	$R/\overline{w}$	0	0 = DCM fixed-frequency boost switching (no negative inductor current) 1 = Forced CCM fixed-frequency boost switching (negative inductor current allowed)
OVP_TH[3:0]	[3:0]	$R/\overline{w}$	0000	4-bit selection of the VOUT OVP thresholds: From 47.5V (0000) to 19.375V (1111) in 1.875V decrements per step.

Note: * The POR value listed for each register is the factory programmed default value. These POR values could change after performing MTP programming.

Register CONFIG1

Address	Name	POR Value(*)
0x01	CONFIG1	0x53

Bit Assignment

7	6	5	4	3	2	1	0
Reserved	BOOST_ILIM[1:0]		FSW_BOOST[4:0]				

Bit Description

Field Name	Bits	Type	POR(*)	Description
Reserved	[7]	$R/\overline{w}$	0	Reserved
BOOST_ILIM[1:0]	[6:5]	$R/\overline{w}$	10	Boost cycle-by-cycle ILIM threshold: 00 = 2.0A 01 = 1.0A 10 = 3.0A (default) 11 = 4.0A
FSW_BOOST[4:0]	[4:0]	$R/\overline{w}$	10011	Boost switching frequency. For the full frequency chart, see Boost Converter Switching Frequency on page 34. ≤02h = 3.41 MHz 04h = 2.048 MHz 09h = 1.024 MHz 13h = 512 kHz (default)

Note: * The POR value listed for each register is the factory programmed default value. These POR values could change after performing MTP programming.

Register FADING_SPEED

Address	Name	POR Value(*)
0x02	FADING_SPEED	0x00

Bit Assignment

7	6	5	4	3	2	1	0
FADING_SPEED[7:0]							

Bit Description

Field Name	Bits	Type	POR(*)	Description
FADING_SPEED[7:0]	[8]	$R/\overline{W}$	00000000	Sets the fading counter from 50 µs to 12.75 ms in 50 µs steps. This is the period between each intensity step. 0x00 = No fading 0x01 = 50 µs per step 0xFF = 12.75 ms per step

Note: * The POR value listed for each register is the factory programmed default value. These POR values could change after performing MTP programming.

Register CONFIG2

Address	Name	POR Value(*)
0x03	CONFIG2	0x32

Bit Assignment

7	6	5	4	3	2	1	0
Reserved	LOG_MODE	DIM_MODE	MAX_I [4:0]				

Bit Description

Field Name	Bits	Type	POR(*)	Description
Reserved	[7]	$R/\overline{W}$	0	Reserved
LOG_MODE	[6]	$R/\overline{W}$	0	Dimming mode selector: 0 = Linear mode (default) 1 = Logarithmic mode. The log table uses 1023 codes with the dither function disabled and up to 8191 codes with the dither function enabled.
DIM_MODE	[5]	$R/\overline{W}$	1	Dimming mode selector: 0 = Analog dimming only 1 = Mixed-mode dimming (default)
MAX_I [4:0]	[4:0]	$R/\overline{W}$	10010	Program maximum current per string in 1 mA steps: 00000 = 12 mA 00001 = 13 mA 00010 = 14 mA 10010 = 30 mA (default) 11111 = 43 mA

Note: * The POR value listed for each register is the factory programmed default value. These POR values could change after performing MTP programming.

Register LEDEN

Address	Name	POR Value(*)
0x04	LEDEN	0x00

Bit Assignment

7	6	5	4	3	2	1	0
LEDEN_8	LEDEN_7	LEDEN_6	LEDEN_5	LEDEN_4	LEDEN_3	LEDEN_2	LEDEN_1

Bit Description

Field Name	Bits	Type	POR(*)	Description
LEDEN_8…LEDEN_1	[7:0]	$R/\overline{w}$	0	LED string enabled: 0 = string is disabled 1 = string is enabled (default)
Note: * The POR value listed for each register is the factory programmed default value. These POR values could change after performing MTP programming.				

Register WLED_ISET_LSB

Address	Name	POR Value(*)
0x05	WLED_ISET_LSB	0x00

Bit Assignment

7	6	5	4	3	2	1	0
WLED_ISET[3:0]				DITHER_LSB[2:0]			Reserved

Bit Description

Field Name	Bits	Type	POR(*)	Description
WLED_ISET[3:0]	[7:4]	$R/\overline{W}$	0000	LED output current setting bits 3-0. For details, see LED Brightness Control on page 38. If changing the LSB bits, these must be written before the MSB bits. Changes to these bits are only implemented when the next register is written, which is typically the MSBs but could be any register.
DITHER_LSB[2:0]	[3:1]	$R/\overline{W}$	000	With DITHER_ENABLE=1, these three bits combine with WLED_ISET[11:0] as the lower LSBs to form a 15-bit ILED dimming control. For 15-bit dimming adjustment, write to these bits along with WLED_ISET[11:0].
Reserved	[0]	$R/\overline{W}$	0	Reserved

Note: * The POR value listed for each register is the factory programmed default value. These POR values could change after performing MTP programming.

Register WLED_ISET_MSB

Address	Name	POR Value(*)
0x06	WLED_ISET_MSB	0x00

Bit Assignment

7	6	5	4	3	2	1	0
WLED_ISET[11:4]							

Bit Description

Field Name	Bits	Type	POR(*)	Description
WLED_ISET[11:4]	[7:0]	$R/\overline{w}$	00000000	The MSB bits of the WLED_ISET[11:0] brightness code. For details, see LED Brightness Control on page 38.
Note: * The POR value listed for each register is the factory programmed default value. These POR values could change after performing MTP programming.				

Register CONFIG3

Address	Name	POR Value(*)
0x07	CONFIG3	0x08

Bit Assignment

7	6	5	4	3	2	1	0
ISET_EXT	LED_SHORT_VTH [1:0]		PWM_IX [1:0]		PWM_DIM_FREQ[2:0]		

Bit Description

Field Name	Bits	Type	POR(*)	Description
ISET_EXT	[7]	$R/\overline{W}$	0	0 = LED full-scale current set by MAX_I[4:0] (default) 1 = LED full-scale current set by ISET external resistor and MAX_I[4:0]
LED_SHORT_VTH [1:0]	[6:5]	$R/\overline{W}$	00	LED short detect threshold: 00 = 4.35V (default) 01 = 4.85V 10 = 5.25V 11 = 5.75V
PWM_IX [1:0]	[4:3]	$R/\overline{W}$	01	PWM_IX[1:0] transition point between analog dimming and PWM dimming during mode change: 00 = 12.5% 01 = 25% (default) 10 = 50% 11 = 100% (also 100% PWM dimming)
PWM_DIM_FREQ[2:0]	[2:0]	$R/\overline{W}$	000	PWM_DIM_FREQ in kHz: 000 = 2.5 kHz (default) 001 = 5 kHz 010 = 10 kHz 011 = 20 kHz 100 = 40 kHz 101…111 = Reserved

Note: * The POR value listed for each register is the factory programmed default value. These POR values could change after performing MTP programming.

Register CONFIG4

Address	Name	POR Value(*)
0x08	CONFIG4	0x00

Bit Assignment

7	6	5	4	3	2	1	0
I2C_STANDBY	RESET	Reserved					

Bit Description

Field Name	Bits	Type	POR(*)	Description
I2C_STANDBY	[7]	$R/\overline{W}$	0	Quasi-low current mode with references and digital blocks disabled, but register contents retained (MTP not reloaded): 0 = Not in standby 1 = Standby mode
RESET	[6]	$R/\overline{W}$	0	Power on reset bit – clears all register contents and MTP is reloaded.
Reserved	[5:0]	–	–	Reserved

Note: * The POR value listed for each register is the factory programmed default value. These POR values could change after performing MTP programming.

Register FILTER_SETTINGS

Address	Name	POR Value(*)
0x09	FILTER_SETTINGS	0x24

Bit Assignment

7	6	5	4	3	2	1	0
DIMCODE[1:0]		DITHER_ENABLE	RCFILTER[1:0]		PWMFILTER[2:0]		

Bit Description

Field Name	Bits	Type	POR(*)	Description
DIMCODE[1:0]	[7:6]	$R/\overline{W}$	00	Brightness control method: 00 = PWM control only (default) 01 = I²C control only 10 = Input PWM x I²C control 11 = Reserved
DITHER_ENABLE	[5]	$R/\overline{W}$	1	0 = Dithering disabled 1 = Enable dithering for up to 15-bit effective resolution for linear dimming mode, up to 13-bit effective resolution for logarithmic dimming mode (default).
RCFILTER[1:0]	[4:3]	$R/\overline{W}$	00	RC filter time constant: 00 = RC filter OFF (default) 01 = 417 ms 10 = 207 ms 11 = 103 ms
PWMFILTER[2:0]	[2:0]	$R/\overline{W}$	100	Enables or disables the PWM filter and sets the step size: 000 = OFF 001 = 2 steps 010 = 4 steps 011 = 6 steps 100 = 8 steps (default) 101 = 10 steps 110 = 12 steps 111 = 14 steps

Note: * The POR value listed for each register is the factory programmed default value. These POR values could change after performing MTP programming.

Register VREG_IMAXTUNE

Address	Name	POR Value(*)
0x0A	VREG_IMAXTUNE	0x70

Bit Assignment

7	6	5	4	3	2	1	0
LED_VREG_CNT_INIT[3:0]				IMAXTUNE[3:0]			

Bit Description

Field Name	Bits	Type	POR(*)	Description
LED_VREG_CNT_INIT[3:0]	[7:4]	$R/\overline{W}$	0111	Initial starting target voltage, 2.27V increments per step: 0000 = 13.75V 0001 = 16.02V 0010 = 18.28V … 0111 = 29.61V (default) 1000 = 31.88 … 1110 = 45.47V 1111 = 47.73V
IMAXTUNE[3:0]	[3:0]	$R/\overline{W}$	0000	Sets percentage increase of LED full-scale current in approximately 0.51% increments starting from code 1h: 0000 = 0.00% increase 0001 = 0.47% increase … 1101 = 7.12% increase 1111 = 7.66% increase

Note: * The POR value listed for each register is the factory programmed default value. These POR values could change after performing MTP programming.

Register CONFIG_CP

Address	Name	POR Value(*)
0x0B	CONFIG_CP	0x00

Bit Assignment

7	6	5	4	3	2	1	0
AUTO_CP_RATIO	SEL_CP_RATIO	Reserved		CP_FREQ_TRAN	SEL_CP_FREQ	CP_FREQ_DIV[1:0]	

Bit Description

Field Name	Bits	Type	POR(*)	Description
AUTO_CP_RATIO	[7]	$R/\overline{W}$	0	Sets the charge pump ratio: 0 = Device automatically selects 2x or 3x charge pump ratio based operating condition 1 = Charge pump ratio is fixed by the SEL_CP_RATIO bit
SEL_CP_RATIO	[6]	$R/\overline{W}$	0	Active only if AUTO_CP_RATIO=1: 0 = Device operates in 2x charge pump ratio only 1 = Device operates in 3x charge pump ratio only
Reserved	[5:4]	$R/\overline{W}$	00	Reserved
CP_FREQ_TRAN	[3]	$R/\overline{W}$	0	0 = Charge pump frequency changes at 75% and 50% LED brightness automatically. 1 = Charge pump frequency changes at 50% LED brightness only, and as a function of CP_FREQ_DIV[0].
SEL_CP_FREQ	[2]	$R/\overline{W}$	0	When CP_FREQ_TRAN=0: 0 = Charge pump frequency changes at 75% and 50% LED brightness automatically 1 = Charge pump is independent of LED brightness and selected by CP_FREQ_DIV[0] When CP_FREQ_TRAN=1: SEL_CP_FREQ bit is don't care.
CP_FREQ_DIV[1:0]	[1:0]	$R/\overline{W}$	00	When CP_FREQ_TRAN=0, SEL_CP_FREQ=1: 00 = 1/2 01 = 1/4 10 = 1/8 11 = 1/8 When CP_FREQ_TRAN=1: CP_FREQ_DIV[0] = 0 the charge pump frequency changes between 1/2 (≥50% LED brightness) and 1/4 (<50% LED brightness). CP_FREQ_DIV[0] = 1 the charge pump frequency changes between 1/4 (≥50% LED brightness) and 1/8 (<50% LED brightness).

Note: * The POR value listed for each register is the factory programmed default value. These POR values could change after performing MTP programming.

Register CHKSUM0

Address	Name
0x0C	CHKSUM0

Bit Assignment

7	6	5	4	3	2	1	0
CHKSUM0[7:0]							

Bit Description

Field Name	Bits	Type	Description
CHKSUM0[7:0]	[7:0]	R	Lower eight bits of the 16-bit register checksum for registers 0x00–0x0B. If incorrect, the MTP values are still loaded if the internal factory checksum is correct. After each MTP write, the CHKSUM0 register value is updated after toggling the EN pin or cycling VIN.

Register CHKSUM1

Address	Name
0x0D	CHKSUM1

Bit Assignment

7	6	5	4	3	2	1	0
CHKSUM1[7:0]							

Bit Description

Field Name	Bits	Type	Description
CHKSUM1[7:0]	[7:0]	R	Upper eight bits of the 16-bit register checksum for registers 0x00 to 0x0B. If incorrect, the MTP values are still loaded if the internal factory checksum is correct. After each MTP write, the CHKSUM1 register value is updated after toggling the EN pin or cycling VIN.

Register STATUS1

Address	Name	POR Value(*)
0x0E	STATUS1	0x00

Bit Assignment

7	6	5	4	3	2	1	0
BST_ILIM_SEC	VOUT_OVP	VX_OV	VX_UV	DISC_OCP	TSD	SS_TIMEOUT	LED_SHORT

Bit Description

Field Name	Bits	Type	POR(*)	Description
BST_ILIM_SEC	[7]	R	0	Status bit to flag a secondary current limit: 0 = No error 1 = Boost current exceeded secondary current limit
VOUT_OVP	[6]	R	0	Status bit to flag an output over-voltage condition: 0 = No error 1 = Output over-voltage
VX_OV	[5]	R	0	Status bit to flag a VX over-voltage condition: 0 = No error 1 = VX voltage is above over-voltage threshold
VX_UV	[4]	R	0	Status bit to flag a VX under-voltage condition: 0 = No error 1 = VX voltage is below under-voltage threshold
DISC_OCP	[3]	R	0	Status bit to flag a disconnect switch over-current event: 0 = No error 1 = Disconnect switch exceeded over-current threshold, or VOUT is shorted to ground
TSD	[2]	R	0	Status bit to flag a thermal shutdown condition: 0 = No error 1 = Part has exceeded thermal shutdown threshold
SS_TIMEOUT	[1]	R	0	Status bit to flag a soft start timeout condition: 0 = No error 1 = Soft start has not completed before the timeout event
LED_SHORT	[0]	R	0	Status bit to flag an LED shorted-string fault: 0 = No error 1 = An LED shorted-string event occurred on one or more enabled strings

Note: * The POR value listed for each register is the factory programmed default value. These POR values could change after performing MTP programming.

Register STATUS2

Address	Name	POR Value(*)
0x0F	STATUS2	0x00

Bit Assignment

7	6	5	4	3	2	1	0
MTP_WRITE_CMD[4:0]					MTP_WRITE_DNE	CRCOK	LED_OPEN

Bit Description

Field Name	Bits	Type	POR(*)	Description
MTP_WRITE_CMD[4:0]	[7:3]	$R/\overline{W}$	00000	Writing 10010 to these register bits automatically initiates an MTP programming cycle to register 0x00–0x0B. At the end of programming, this register is automatically cleared, and the MTP_WRITE_DNE read-only status bit shows '1'.
MTP_WRITE_DNE	[2]	R	0	Status bit indicating the completion of MTP programming for registers 0x00–0x0B. Clears upon read.
CRCOK	[1]	R	0	Status bit indicating that the CHECKSUM for registers 0x00–0x0B is good.
LED_OPEN	[0]	R	0	Status bit to flag an open or grounded condition on any LED pin: 0 = No error 1 = One or more LED strings is grounded open

Note: * The POR value listed for each register is the factory programmed default value. These POR values could change after performing MTP programming.

Application Schematic

Figure 61 shows the ARC3C0845/ARC3C0845W detailed application schematic. For compensation details, contact pSemi.

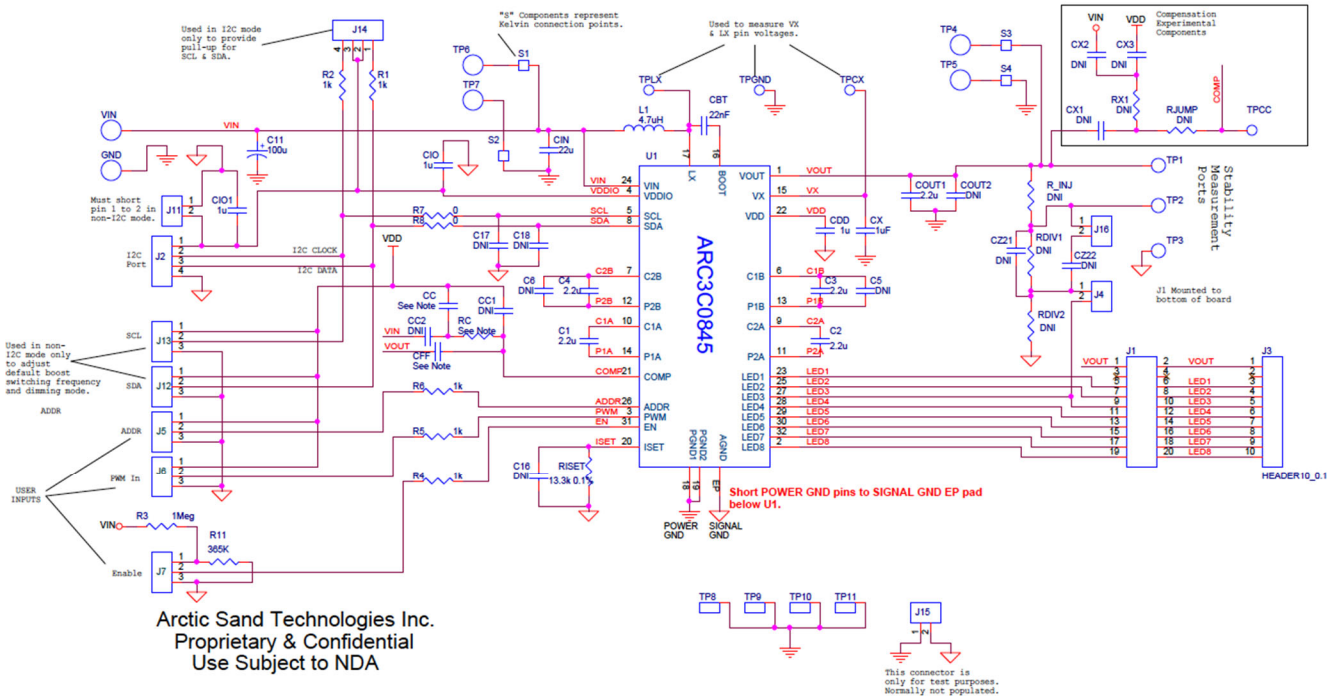


Figure 61. ARC3C0845/ARC3C0845W Detailed Application Schematic

Application Circuit Part List

Table 19 lists the recommended part numbers.

Table 19. Recommended Parts[1]

Component	Value	Part Size	Mfg. Part Number
CBT	22 nF 50V X7R	0402	GRM155R71H223KA12D
CX	1 µF 35V X5R	0402	GRM155R6YA105KE11
C3, C4	2.2 µF 50V X5R	1206	GJ8319R61H225KA12
C1, C2	2.2 µF 25V X5R	0805	C2012X5R1E225K085AC
CIN [2]	1.0 µF 16V X5R	0603	GRM188R61C105KA12D
CC [3]	–	0201	–
CFF [3]	–	0201	–
COUT	2.2 µF 50V X5R	1206	GJ8319R61H225KA12
CDD, CIO	1 µF 10V X5R	0402	GRM155R61A105KE15D
L1 [4]	4.7 µH	3.2 mm x 2.5 mm x 1.2 mm	DFE322512F-4R7M
RISET	13.3 kΩ	0402	Use tighter than 1% tolerance
RC [3]	–	0201	–

Notes:

1. Components in this part list are optimized for 8P12S or higher applications. For an optimized selection based on your application, contact pSemi.
2. Value might require an adjustment based on proximity of the input source to eliminate input voltage ringing.
3. For the general selection, see Switching Converter Compensation on page 35. For an optimized selection based on your application, contact pSemi.
4. See also recommended inductor values below for varying operating conditions.

Component Selection

pSemi recommends that ARC3C0845/ARC3C0845W customers adhere closely to the parts selected for the Application Circuit Part List in Table 19. Component selection is a complex process and several of the parameters of importance to the design are not typically specified for passive components. If you want to deviate from these recommended components, contact pSemi for guidance.

Efficiency Optimization

The ARC3C0845/ARC3C0845W is designed specifically to address 2-cell and 3-cell narrow-voltage DC (NVDC) platforms, and for a wide range of LED configurations. The two-stage architecture relies less on the inductor for power and voltage conversion; therefore, reduction in the physical size of the inductor has less impact on the overall conversion efficiency compared with traditional single-stage architectures. This enables the use of low profile, small footprint and low-cost chip inductors versus wire-wound inductors used by traditional LED boost drivers.

Table 20 lists inductors optimized for platforms with an input voltage that is 2-cell NVDC only; 3-cell NVDC only; or 2-cell AND 3-cell NVDC. The latter solution trades off a small amount of efficiency in exchange for a single bill-of-materials for platforms where cell count may vary. Refer to the typical performance data for measured efficiency using for these different inductor and LED configurations for max ILED=30 mA.

Table 20. Inductors Optimized for Platforms

LED Configuration	2-Cell Only	3-Cell Only	2-Cell and 3-Cell
8P12S	2.2 µH	6.8 µH	3.3 µH
8P11S	2.2 µH	6.8 µH	3.3 µH
8P10S	2.2 µH	6.8 µH	3.3 µH
6P12S	2.2 µH, 4.7 µH	6.8 µH	3.3 µH
6P11S	2.2 µH, 4.7 µH	6.8 µH, 10 µH	3.3 µH
6P10S	4.7 µH	6.8 µH, 10 µH	3.3 µH
4P12S	4.7 µH	6.8 µH, 10 µH	3.3 µH

Capacitor Selection

If, due to component availability, size, second-source requirement, or other reasons that the Application Circuit Part List in Table 19 cannot be followed, use the following guidelines to select the proper ARC3C0845/ARC3C0845W capacitors.

Charge Pump Capacitors

The effective capacitance of the capacitors used for C1A, C2A, C1B and C2B must have a minimum value of 0.7 µF, and the ideal value is 1 µF. The effective capacitance must match closely between charge pump capacitors; therefore, the same capacitor cannot be used for both the first and second charge pump stages. For example, with V_{OUT} at 45V, 15V is applied across the charge pump capacitors C1A and C2A, and 30V is applied across the second-stage charge pump capacitors C1B and C2B. Following the Application Circuit Part List in Table 19, the C2012X5R1E225K085AC capacitor selected for C1A and C2A has a 1-µF effective capacitance at 15V and the GJ8319R61H225KA12 capacitor selected for C1B and C2B has 1.05 µF at 30V, which matches closely with the C1A and C2A capacitors. If the same GJ8319R61H225KA12 capacitor is used for C1A and C2A, then the effective capacitance at 15V would be 1.8 µF, which is much higher than 1.05 µF. This wide capacitance difference can lower efficiency.

If a single capacitor cannot meet the effective capacitor requirement, use two or more capacitors in parallel together to meet the effective capacitor requirement.

VX Capacitor

The VX boost convertor output capacitor must have an effective capacitance between 0.1 µF and 0.2 µF. The VX voltage can easily be calculated:

- In 3x CP ratio, the VX is approximately VOUT/3.
- In 2x CP ratio, the VX is approximately VOUT/2.

VDD Capacitor

The VDD internal LDO capacitor must have a minimum effective capacitance of 0.5 µF. The VDD pin typical output voltage is 4.4V with a maximum output of 5V.

VOUT Capacitor

The VOUT LED output voltage capacitor must have an effective capacitance of 1 µF.

Layout Example

Figure 62 shows an example of a compact eight WLED string converter layout. The solution size is 95 mm^2.

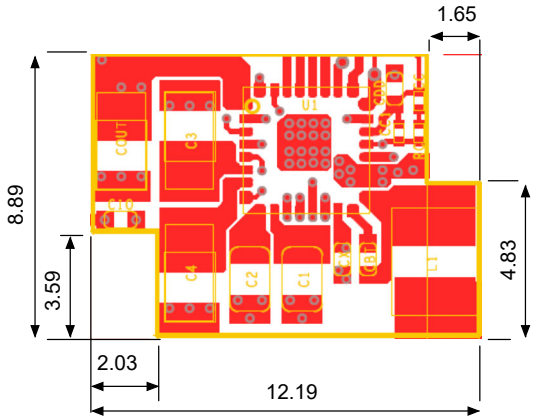


Figure 62. Layout Example

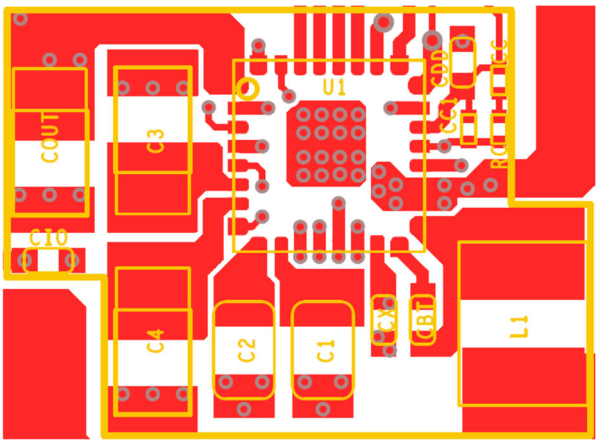


Figure 63. Top Layer

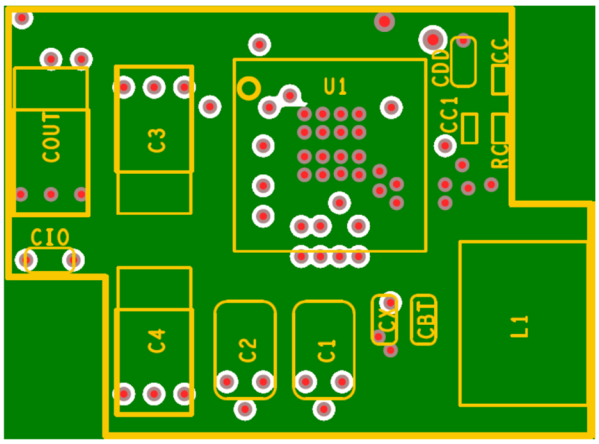


Figure 64. Layer 2

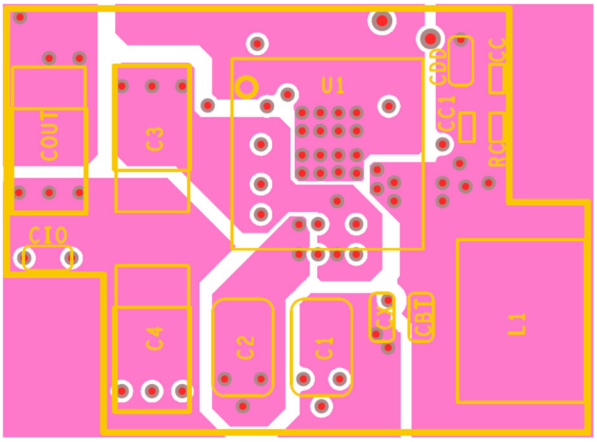


Figure 65. Layer 3

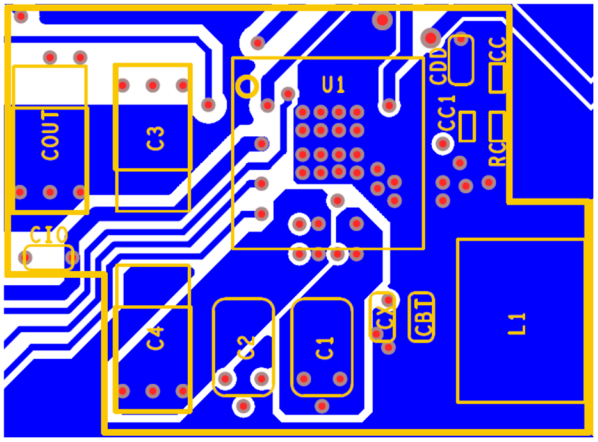


Figure 66. Bottom Layer

Packaging Information

This section includes the following packaging data:

- Package drawings
- PCB Land Design Guidelines
- Package marking
- Tape-and-reel information

ARC3C0845 Package Drawing

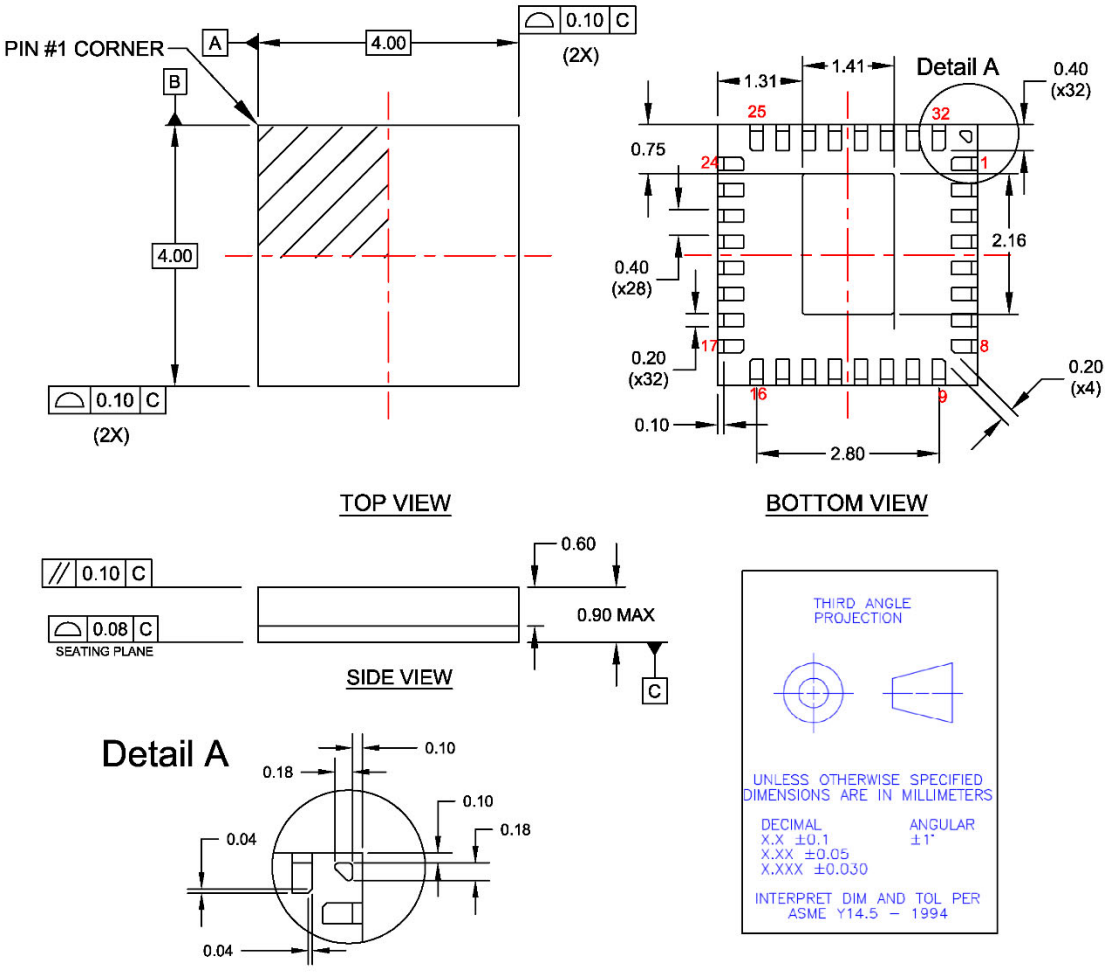
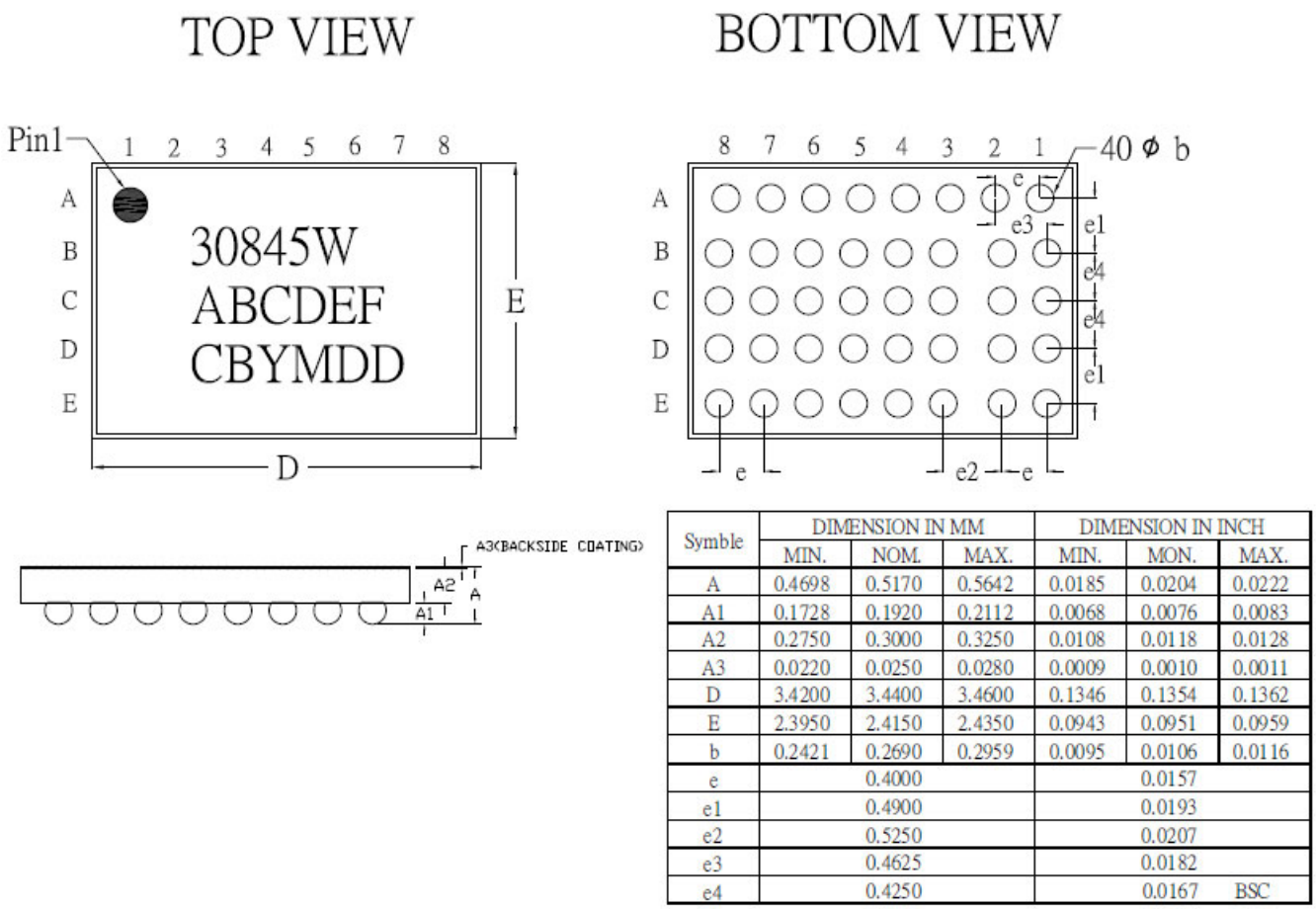


Figure 67. ARC3C0845 Package Mechanical Drawing

ARC3C0845W Package Drawing



Symble	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	MON.	MAX.
A	0.4698	0.5170	0.5642	0.0185	0.0204	0.0222
A1	0.1728	0.1920	0.2112	0.0068	0.0076	0.0083
A2	0.2750	0.3000	0.3250	0.0108	0.0118	0.0128
A3	0.0220	0.0250	0.0280	0.0009	0.0010	0.0011
D	3.4200	3.4400	3.4600	0.1346	0.1354	0.1362
E	2.3950	2.4150	2.4350	0.0943	0.0951	0.0959
b	0.2421	0.2690	0.2959	0.0095	0.0106	0.0116
e	0.4000			0.0157		
e1	0.4900			0.0193		
e2	0.5250			0.0207		
e3	0.4625			0.0182		
e4	0.4250			0.0167		BSC

ARC3C0845W Package Mechanical Drawing

PCB Land Design Guidelines

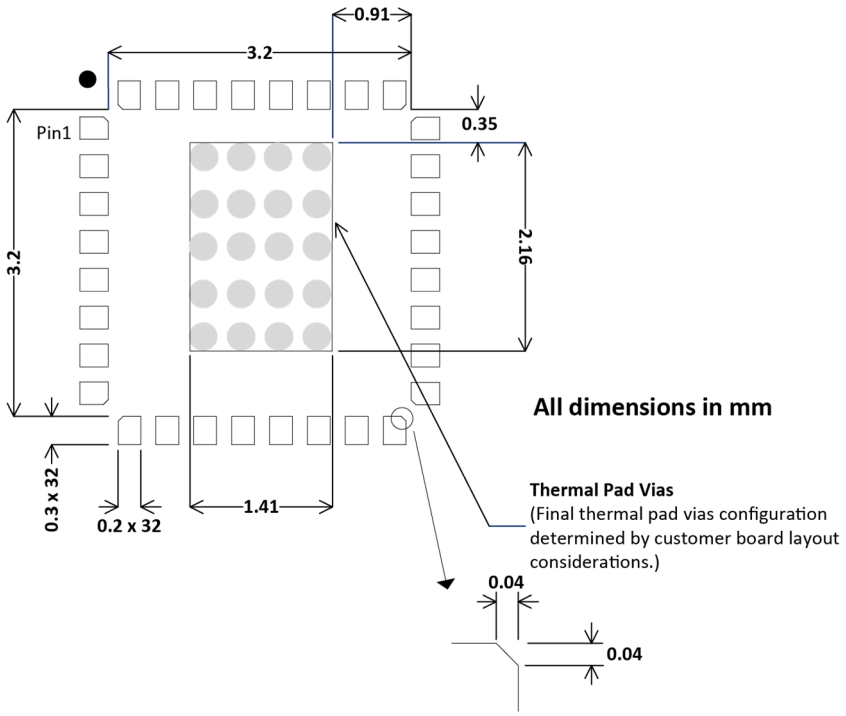


Figure 68. ARC3C0845 32P QFN Recommended PCB Footprint

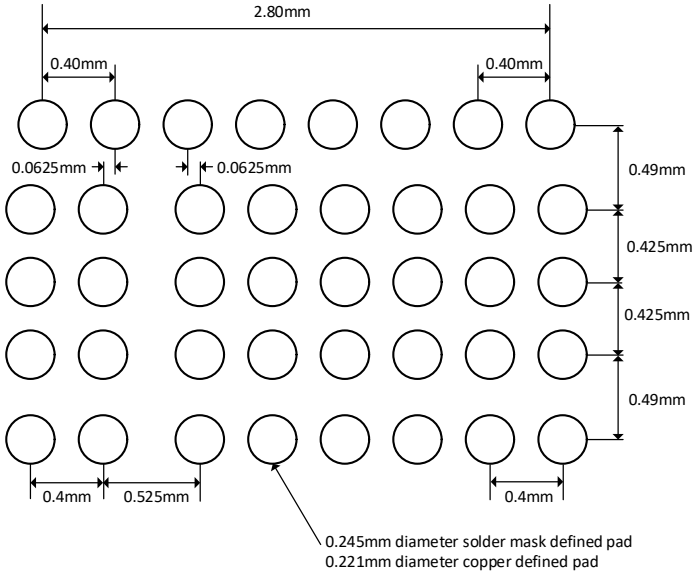


Figure 69. ARC3C0845W 40P WLCSP Recommended PCB Footprint

The solder mask openings must be larger with a typical 0.05-mm ring all around each of the perimeter pads. The center pad is solder mask defined, with the dimensions as shown above. The copper for the center pad can be extended beyond the solder mask defined pad as needed to optimize the thermal performance. Put as many thermal vias as possible in this copper. There must be no PCB Layer 1 copper under any package exposed metal, except for the center pad. All the exposed metal is dimensioned in the package mechanical details.

Top-Marking Specifications

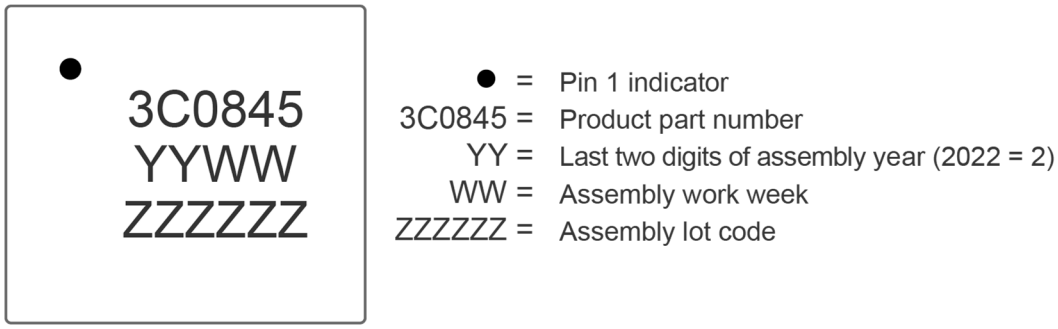


Figure 70. ARC3C0845 Package Marking Specification

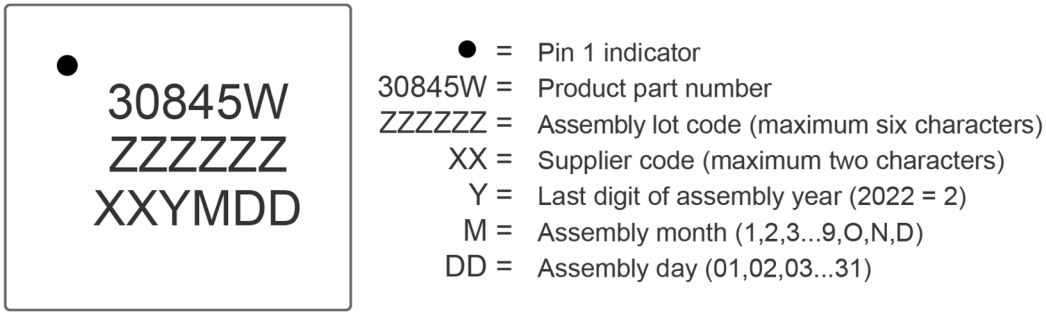
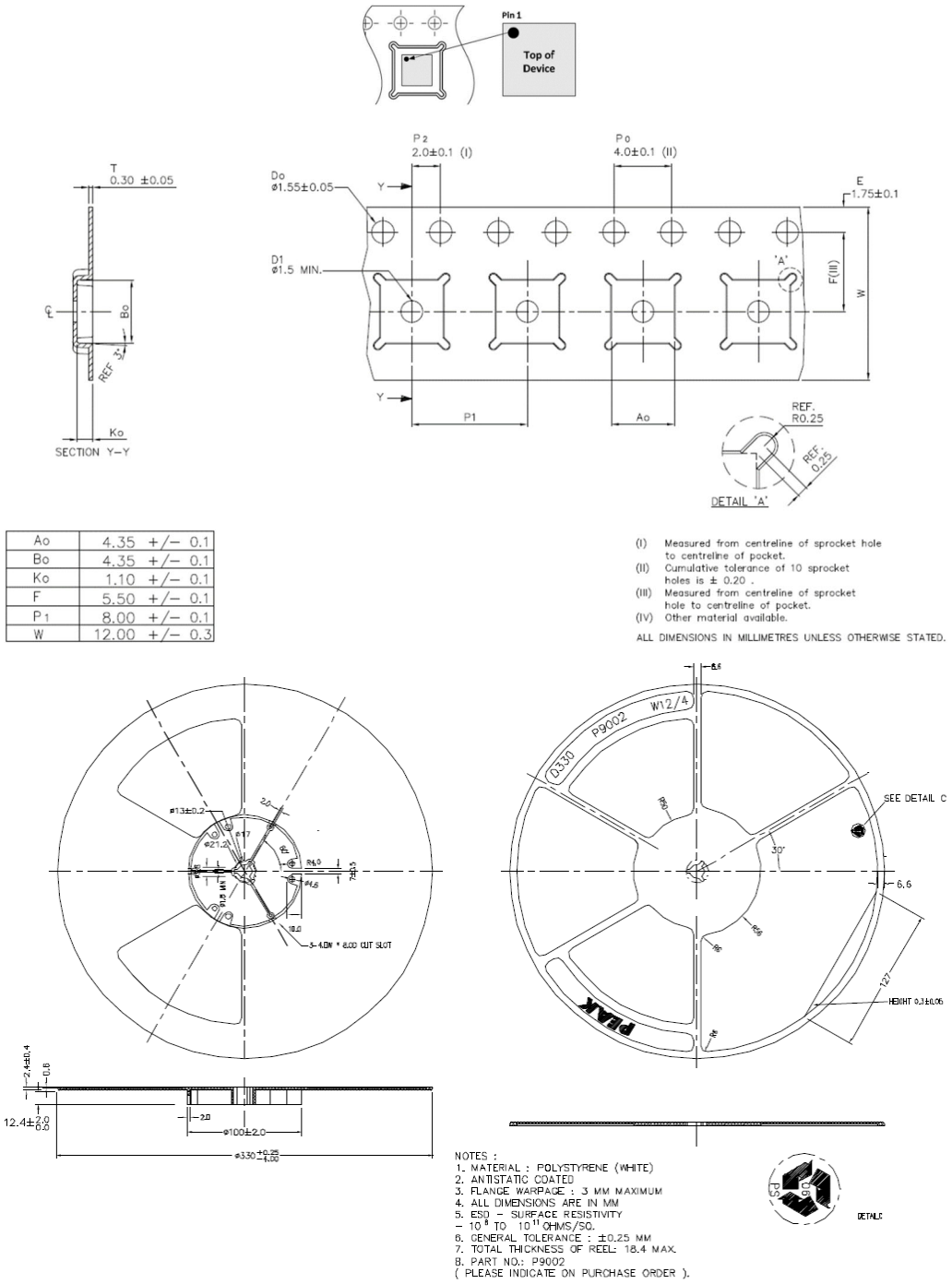


Figure 71. ARC3C0845W Package Marking Specification

Tape and Reel Specification



Ao	4.35 +/– 0.1
Bo	4.35 +/– 0.1
Ko	1.10 +/– 0.1
F	5.50 +/– 0.1
P1	8.00 +/– 0.1
W	12.00 +/– 0.3

Figure 72. ARC3C0845 Tape and Reel Specifications

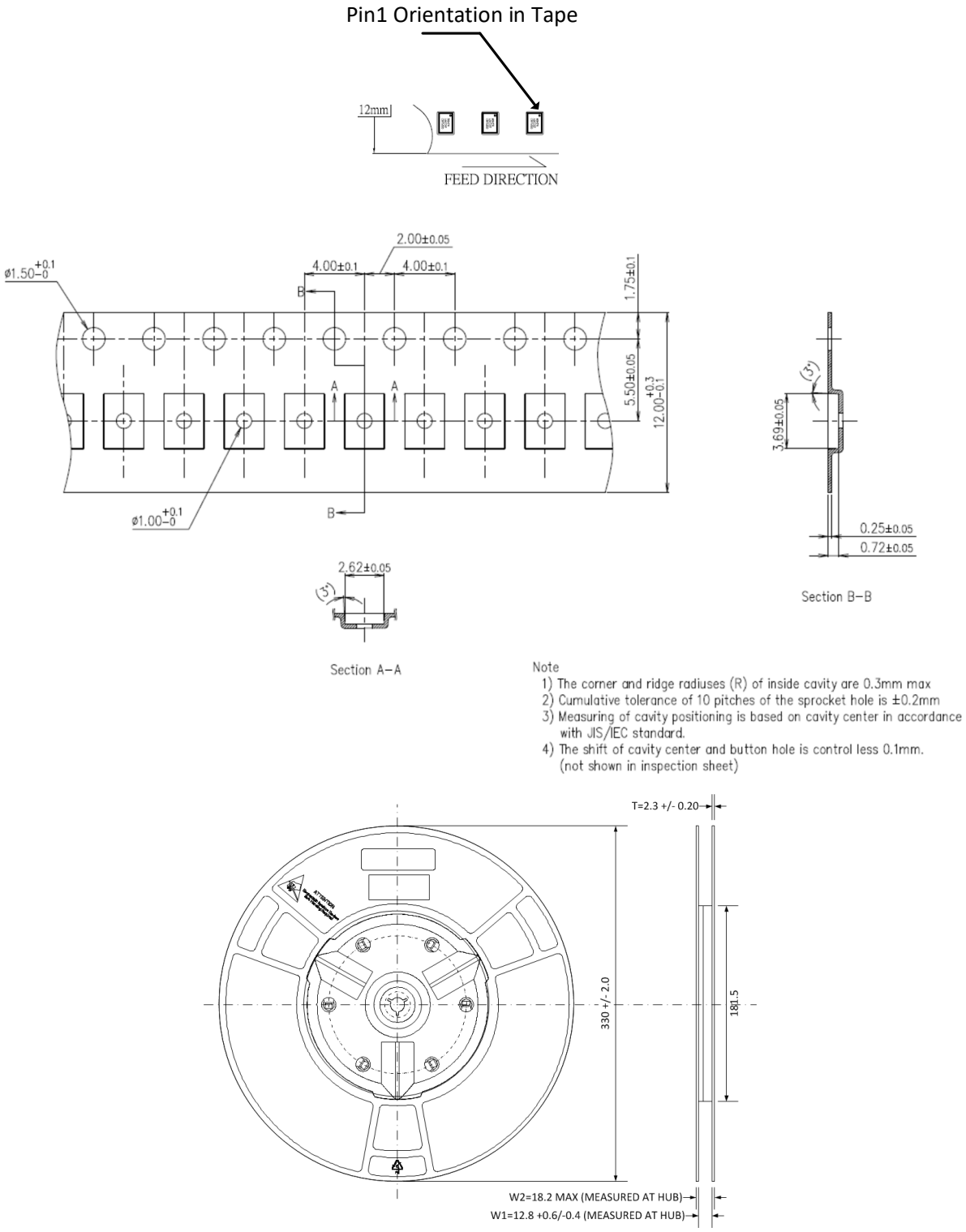


Figure 73. ARC3C0845W Tape and Reel Specifications

Ordering Information

Table 21 lists the ARC3C0845/ARC3C0845W order codes and shipping methods.

Table 21. ARC3C0845/ARC3C0845W Order Codes and Shipping Methods

Order Codes	Description	Packaging	Shipping Method
ARC3C0845-R	High-Efficiency LED Backlight Driver	4 mm x 4 mm QFN, 32-pin	5000 units/large tape and reel
ARC3C0845-V			250 units/small tape and reel
ARC3C0845-G			10 units/sample waffle tray
ARC3C0845W-R	High-Efficiency LED Backlight Driver	3.44 mm x 2.415 mm WLCSP, 40-pin	5000 units/large tape and reel
ARC3C0845W-V			250 units/small tape and reel
ARC3C0845W-G			10 units/sample waffle tray

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The datasheet contains final data. In the event pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a Customer Notification Form (CNF).

Product Brief

This document contains a shortened version of the datasheet. For the full datasheet, contact sales@psemi.com.

Sales Contact

For additional information, contact Sales at sales@psemi.com.

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