Description

The **ARC3C0845/ARC3C0845W** is an ultra-high efficiency DC/DC converter solution with integrated programmable current sinks that drive up to eight strings of LEDs. The ARC3C0845/ARC3C0845W integrates all MOSFETs and their control & driver circuitry. With the proprietary architecture, the ARC3C0845/ARC3C0845W provides the highest efficiency (>94%) possible in a compact 3.44 mm x 2.415 mm WLCSP40 (ARC3C0845W) or 4 mm x 4 mm 32-pin LGA package (ARC3C0845). The high switching frequency enables a small and low profile solution size aligned to the needs of the latest mobile products.

Features

- Synchronous DC/DC converter with integrated FETs
- 2- and 3-cell Li-Ion battery input voltage: 4.5V to 15V
- Proprietary architecture for ultra-high LED efficiency, above 88% over the entire operating range
- Integrated output disconnect switch
- Up to 45V output for maximum flexibility in assignment of LEDs to strings and selection of LED forward voltage
- Up to 12-bit dimming resolution with an additional 3-bit dithering
- Supports linear/logarithmic analog and PWM dimming, or direct PWM dimming, for maximum flexibility and resolution
- LED brightness ramp up/down control with programmable ramp rate and linear/logarithmic ramp profiles
- Phase-shifted PWM dimming among active strings to minimize audible noise
- 1 MHz I^{2}C 6.0-compatible serial interface to program the brightness, or an external resistor on ISET pin to set the maximum brightness
- Extensive programming capability with non-volatile memory for storing user register settings
- Eight independently enabled current sinks, up to 43 mA per current sink
- External PWM input for fine dimming resolution
- 0.5% current matching at 30 mA per current sink
- Wide range of input and output voltages with 2x and 3x charge pump ratio
- Select table boost switching frequency from 320 KHz to 2.6 MHz
- Extensive fault protection including boost overcurrent protection, output short circuit protection, output over-voltage protection, LED open and short protection, and thermal shutdown

Typical Applications

- 2-cell and 3-cell platforms including:
- 8”-17” FHD/UHD+ LCD backlight panels
- Ultrabooks / ultraportables / notebooks
- 2-in-1 / convertible / detachable notebooks
- Full-size tablet computers
- LCD panels
- Ultra-thin form factor mobile platforms

Efficiency

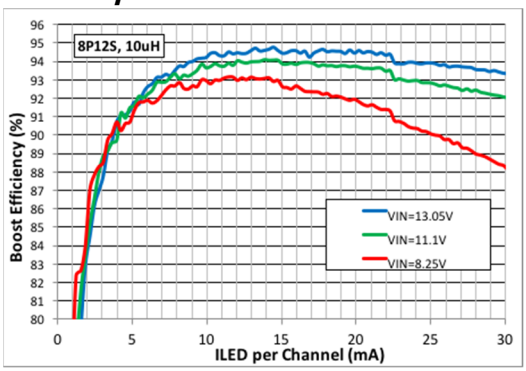

Figure 1: Typical Boost Efficiency – 8p12s

Simplified Application

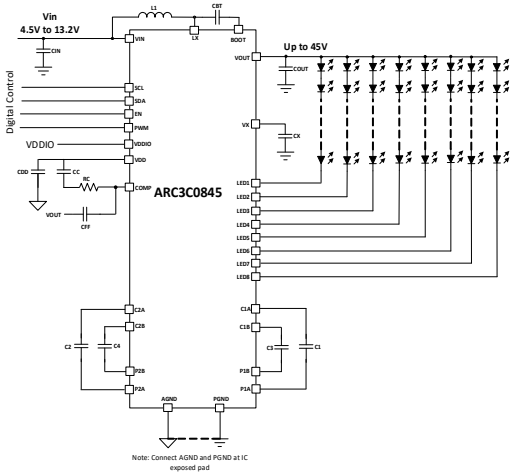

Figure 2: Typical Application Circuit

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Absolute Maximum Ratings[1,2]

PARAMETER	MIN	MAX	UNITS
VIN to AGND	-0.3	17.6	V
VDD, VDDIO, PWM, COMP, EN, ISET, SCL, SDA, ADDR to AGND	-0.3	6	V
VOUT, C1B, C2B to AGND	-0.3	47	V
LEDx to AGND	-0.3	40	V
AGND to PGND	-0.3	0.3	V
LX, VX, P1A, P2A, P1B, P2B to PGND	-0.3	22	V
VX to LX, P1A, P2A, P1B, P2B	-0.3	22	V
BOOT to VDD	-0.3	22	V
BOOT to LX	-0.3	6	V
C1A, C2A to VX	-0.3	22	V
C1B to C2A	-0.3	33	V
C2B to C1A	-0.3	33	V
Storage Temperature	-65	150	°C
PARAMETER	**VALUE**		
Junction Temperature	150°C		
Bump or Lead Temperature (soldering, reflow)	+260°C		
ESD Tolerance, ARC3C0845 HBM[3,5]	1kV		
ESD Tolerance, ARC3C0845W HBM[3]	1kV		
ESD Tolerance, CDM[4]	1kV		

Notes:

1. *The application of any stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device, and exposure at any of these ratings for extended periods may reduce the reliability of the device.*
2. *The above "Absolute Maximum Ratings" are stress ratings only; the notation of these conditions does not imply functional operation of the device at these or any other conditions that fall outside the range identified by the operational sections of this specification.*
3. *Human body model, per the JEDEC standard JS-001-2017.*
4. *Field induced charge device model, per the JEDEC standard JESD22-C101.*
5. *With exception, contact factory for detail. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. Pins listed as 1kV may have higher ESD performance.*

Table 1: Absolute Maximum Ratings

Recommended Operating Conditions

PARAMETER	MIN	MAX	UNITS
VIN Input Voltage Range, relative to AGND or PGND[1]	4.5	15	V
VOUT Output Voltage Range, relative to AGND PGND[1]	18	45	V
VX Boost Output Voltage Range, relative to AGND or PGND	1.2*VIN	20	V
VDDIO Voltage Range, relative to AGND	1.08	5.5	V
Junction Temperature Range, T_J	-30	125	°C

Table: Recommended Operating Conditions

Package Thermal Characteristics[2,3]

DEVICE	PARAMETER	MAX	UNITS
ARC3C0845	Junction-to-ambient thermal resistance (Θ_{JA}), soldered thermal pad, connected to plane	47	°C/W
	Junction-to-board thermal characterization (Ψ_{JB})	25	°C/W
	Junction-to-top case thermal characterization (Ψ_{JC})	5.8	°C/W
ARC3C0845W	Junction-to-ambient thermal resistance (Θ_{JA}), soldered thermal pad, connected to plane	46	°C/W
	Junction-to-board thermal characterization (Ψ_{JB})	11	°C/W
	Junction-to-top case thermal characterization (Ψ_{JC})	8	°C/W

Notes:

1. *Vin and Vout ranges must meet valid operating regions as shown on graph (see page 11).*
2. *Package thermal characteristics and performance are measured and reported in a manner consistent with the JEDEC standards JESD51-8 and JESD51-12.*
3. *Junction-to-Ambient Thermal Resistance (Θ_{JA}) is a function not only of the IC, but it is also extremely sensitive to the environment which includes, but is not limited to, board thickness, planes, copper weight / routes, and air flow. Attention to the board layout is necessary to realize expected thermal performance.*

Table 2: Package Thermal Characteristics

Electrical Characteristics[1]

V_{IN} = 7.4V, V_{AGND} = V_{PGND} = 0V, V_{EN} = 1.8V, T_A = T_J = -30°C to +85°C, unless otherwise noted. Typical values are at T_A = T_J = 25°C with 8p12s.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY						
Input Voltage Range	V_{VIN}	See Figure 5 for valid operating ranges	4.5		15	V
Voltage Regulator Output Voltage	V_{DD}			4.4	5.0	V
Undervoltage Lockout (UVLO) Threshold High	V_{UVLO_H}	V_{VIN} rising		4.275	4.45	V
Undervoltage Lockout (UVLO) Hysteresis	V_{UVLO_HYST}			60		mV
Shutdown Supply Current	I_{VIN_SD}	I_{VIN} with V_{EN}=0V			1	µA
Standby Supply Current	I_{VIN_STDBY}	V_{EN} = 1.8V I^2C_STDBY=1			300	
Supply voltage for digital I/Os	V_{DDIO}		1.08		5.5	V
Supply current for digital I/Os	I_{VDDIO}	EN=0V or 1.8V, SDA=SCL=0V or VDDIO, measure at VDDIO=1.8V		8		µA
Thermal Shutdown Threshold (3)	T_{TSD}			150		°C
Thermal Shutdown Hysteresis (3)	T_{TSD_HYST}			20		°C
Soft Start Time-Out Duration				10		mS
STEP-UP CONVERTER – BOOST						
Output Voltage Range[4,6]	V_{OUT}		18		45	V
Maximum Output Power[5]			10			Watts

Electrical Characteristics[1]

V_{IN} = 7.4V, V_{AGND} = V_{PGND} = 0V, V_{EN} = 1.8V, T_A = T_J = -30°C to +85°C, unless otherwise noted. Typical values are at T_A = T_J = 25°C with 8p12s.

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Boost Switching Frequency Range	f_{SW_BOOST}	I²C interface only FSW_BOOST [4:0]	10011		0.512		MHz
			01001		1.024		
			00101		1.707		
			00011		2.56		
		Non-I²C interface only	SDA = VDD		1.138		
			SDA = open		0.731		
			SDA = AGND		0.51		
Boost Switching Frequency Accuracy				-6		+6	%
Boost Minimum Off-Time	$T_{OFF\_BOOST\_MIN}$				50		ns
Boost Minimum On-Time	$T_{ON\_BOOST\_MIN}$				50		ns
Boost Low-Side Switch Current Limit, Cycle-by-Cycle	I_{BOOST_LIMIT}	I_{LX} rising	BOOST_ILIM[1:0]=00		2.0		A
			BOOST_ILIM[1:0]=01		1.0		
			BOOST_ILIM[1:0]=10		3.0		
			BOOST_ILIM[1:0]=11		4.0		

Notes

1. *Min/Max specifications are 100% production tested at TA=TJ=25°C, unless otherwise noted. Limits over the operating range are guaranteed by design.*
2. *Guaranteed by design.*
3. *Thermal shutdown is not production tested.*
4. *V_{in} and V_{out} ranges must meet valid operating regions as shown on graph (see page 11).*
5. *Higher output power possible under certain operating conditions (contact factory).*
6. *At very light loads in DCM mode, VOUT may be higher than expected. However, LED current regulation is not adversely affected.*

Table 3: Electrical Characteristics

Electrical Characteristics (cont.)[1]

V_{IN} = 7.4V, V_{AGND} = V_{PGND} = 0V, V_{EN} = 1.8V, T_A = T_J = -30°C to +85°C, unless otherwise noted. Typical values are at T_A = T_J = 25°C with 8p12s.

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STEP-UP CONVERTER – CHARGE PUMP							
Output Over-Current Threshold	I_{OUT_OC}	IOUT rising		375			mA
Output Over-voltage Threshold	V_{OUT_OVP}	$O_{VP\_TH[3:0]}$	0000		47.5		V
			0001		45.625		
			…				
			1111		19.375		
Output Over-voltage Hysteresis	$V_{OUT\_OVP\_HYST}$				0.35		V
Accuracy of Output Over-Voltage Protection Threshold	V_{UVLO_HYST}			-5		5	%
LED CURRENT SINKS (LED1 to LED8)							
ISET Voltage	V_{ISET}				0.4		V
ISET Pin Voltage Accuracy				-3		3	V
ISET Recommended Resistor Range	R_{ISET}	Excluding resistor tolerance (E96, 1% tolerance)		13.3		133	kΩ
Current Multiplier	K_{ISET}	I^2C Register Setting MAX_I[4:0]	MAX_I[4:0]=00000		400		A/A
			MAX_I[4:0]=00001		433		
			…		…		
			MAX_I[4:0]=11111		1433		
LED Current Full-Scale Output Range	I_{LED_MAX}	I^2C Register Setting MAX_I[4:0]	MAX_I [4:0]=00000		12		mA
			MAX_I [4:0]=00001		13		
			…		…		
			MAX_I [4:0]=11111		43		
Minimum Sink Current LED1-8	I_{LEDx_MIN}	I_{LED} programmed to 30 mA, linear mapping			7.3		µA
Leakage Current	$I_{LED\_LEAKAGE}$	LED1,..,8=0, VOUT = 36V			0.75	2	µA
LED Current Matching[2]	$I_{LED\_MATCHING}$	ILEDX programmed to 30 mA		-1		1	%
LED Current Matching[2]	$I_{LED\_MATCHING}$	ILEDX programmed to 0.5 mA		-2.5		2.5	%

Electrical Characteristics[1]

V_{IN} = 7.4V, V_{AGND} = V_{PGND} = 0V, V_{EN} = 1.8V, T_A = T_J = -30°C to +85°C, unless otherwise noted. Typical values are at T_A = T_J = 25°C with 8p12s.

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LED Current Accuracy	$I_{LED\_ACCURACY}$	ILEDX programmed to 30 mA		-2		2	%
LED Regulation Voltage	$V_{LED\_REGULATION}$	I_{LEDX} programmed to 30 mA, T_A = 25°C			500		mV
LED Shorted String Detection Threshold		V_{LEDX} falling	LED_SHORT_VTH[1:0]=00		4.35		V
			LED_SHORT_VTH[1:0]=01		4.85		
			LED_SHORT_VTH[1:0]=10		5.25		
			LED_SHORT_VTH[1:0]=11		5.75		
Current Ripple		I_{LED} programmed to 30 mA, T_A = 25°C, DC LED current output				1	%
INTERNAL PWM DIMMING							
Transition Point Between Internal PWM and Analog Dimming[3]		DIM_MODE=0			0%		
		DIM_MODE=1	PWM_IX[1:0]=00		12.5%		
			PWM_IX[1:0]=01		25% (Default)		
			PWM_IX[1:0]=10		50%		
			PWM_IX[1:0]=11		100%		
		Non-I^2C interface[3]			25%		
LED PWM Output Frequency	f_{ILEDX}	I^2C interface, PWM_DIM_FREQ[2:0]		2.5		40	kHz
		Non-I^2C interface			2.5		
LED Current Sink Minimum Output Pulse Width					200		ns

Notes:

1. *Min/Max specifications are 100% production tested at TA=TJ=25°C, unless otherwise noted. Limits over the operating range are guaranteed by design.*
2. *The LED current accuracy is defined/tested as: 100*(ILED_AVG-ILED_Target)/ILED_AVG. The sink current matching is defined/tested as (ILED_MAX-ILED_MIN)/ILED_AVG.*
3. *Default is 25%. Can be trimmed to 0, 12.5%, 50% or 100% if needed for non-I^2C mode.*

Table 4: Electrical Characteristics (cont.)

Electrical Characteristics (cont.)[1]

V_{IN} = 7.4V, V_{AGND} = V_{PGND} = 0V, V_{EN} = 1.8V, T_A = T_J = -30°C to +85°C, unless otherwise noted. Typical values are at T_A = T_J = 25°C with 8p12s.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
DIRECT PWM DIMMING						
Direct PWM Input to Output Timing Skew				100		ns
LOGIC INTERFACE						
EN Logic Input High Voltage	V_{IH_EN}		1.2			V
EN Logic Input Low Voltage	V_{IL_EN}				0.4	V
PWM Logic Input High Voltage	V_{IH_PWM}		0.9			V
PWM Logic Input Low Voltage	V_{IL_PWM}				0.5	V
Logic Input Current	I_{PWM}, I_{EN}		-1.0		1.0	µA
ADDR Input Resistance	I_{ADDR_R}	I²C interface only		100		kΩ
ADDR Input Low Voltage	V_{IL_ADDR}	I²C interface only			0.4	V
ADDR Input High Voltage	V_{IH_ADDR}	I²C interface only	V_{DD}-0.4			V
SDA, SCL Pin Input Resistance	I_{SDA/SCL_R}	Non-I²C interface only		100		kΩ
SDA, SCL Pin Input Low Voltage	$V_{IL\_SDA/SCL}$	Non-I²C interface only			0.4	V
SDA, SCL Pin Input High Voltage	$V_{IH\_SDA/SCL}$	Non-I²C interface only	V_{DD}-0.4			V
PWM Pin Input Frequency for Internal PWM mode	F_{IPWM}		0.2		40	KHz
PWM Pin Input Frequency for Direct PWM mode	F_{DPWM}		0.2		20	KHz
PWM Pin Minimum Input High Pulse			100			ns
PWM Pin Minimum Input Low Pulse			100			ns
I²C SERIAL INTERFACE (SCL, SDA, VDDIO)						
VDDIO Supply Voltage Range	V_{DDIO}		1.08		5.5	V

Electrical Characteristics (cont.)[1]

V_{IN} = 7.4V, V_{AGND} = V_{PGND} = 0V, V_{EN} = 1.8V, T_A = T_J = -30°C to +85°C, unless otherwise noted. Typical values are at T_A = T_J = 25°C with 8p12s.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SDA, SCL Input High Voltage	V_{IH}		0.7 x V_{VDDIO}			V
SDA, SCL Input Low Voltage	V_{IL}				0.3 x V_{VDDIO}	V
SDA, SCL Input Hysteresis	VHYS		0.05 x V_{VDDIO}			V
SDA, SCL Input Current	ISCL, ISDA		-1		1	µA
SDA Output Low Level	VOL	I_{SDA} = 20mA			0.4	V
I^2C Interface Initial Wait Time		Initial Wait time from EN logic high to 1st I^2C command accepted	1000			µs
MTP Non-Volatile Memory Write Cycle Time				34	50	ms
SDA, SCL Pin Capacitance	CI/O				10	pF

Notes:

Min/Max specifications are 100% production tested at TA=TJ=25°C, unless otherwise noted. Limits over the operating range are guaranteed by design.

Table 5: Electrical Characteristics (cont.)

Electrical Characteristics (cont.)

V_{IN} = 7.4V, V_{AGND} = V_{PGND} = 0V, V_{EN} = 1.8V, TA = TJ = -30°C to +85°C, unless otherwise noted. Typical values are at TA = TJ = 25°C with 8p12s.

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
I²C INTERFACE TIMING CHARACTERISTICS FOR STANDARD, FAST MODE AND FAST MODE PLUS					
Serial Clock Frequency	F_{SCL}	Standard mode		100	kHz
		Fast mode		400	kHz
		Fast mode plus		1	MHz
Clock Low Period	t_{LOW}	Standard mode	4.7		µs
		Fast mode	1.3		µs
		Fast mode plus	0.5		µs
Clock High Period	t_{HIGH}	Standard mode	4		µs
		Fast mode	600		ns
		Fast mode plus	260		ns
BUS Free Time between a STOP and a START condition	t_{BUF}	Standard mode	4.7		µs
		Fast mode	1.3		µs
		Fast mode plus	0.5		µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$	Standard mode	4.7		µs
		Fast mode	600		ns
		Fast mode plus	260		ns
Hold Time for a Repeated START condition	$t_{HD:STA}$	Standard mode	4		µs
		Fast mode	600		ns
		Fast mode plus	260		ns
Setup Time of STOP condition	$t_{SU:STO}$	Standard mode	4		µs
		Fast mode	600		ns
		Fast mode plus	260		ns
Data Setup Time	$t_{SU:DAT}$	Standard mode	250		ns
		Fast mode	100		ns
		Fast mode plus	50		ns
Data Hold Time	t_{HD_DAT}	Standard mode	0		µs
		Fast mode	0		ns
		Fast mode plus	0		ns
Rise Time of SCL Signal	t_{RCL}	Standard mode		1000	ns
		Fast mode	20	300	ns
		Fast mode plus		120	ns

Electrical Characteristics (cont.)

V_{IN} = 7.4V, V_{AGND} = V_{PGND} = 0V, V_{EN} = 1.8V, TA = TJ = -30°C to +85°C, unless otherwise noted. Typical values are at TA = TJ = 25°C with 8p12s.

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Fall Time of SCL Signal	t_{FCL}	Standard mode		300	ns
		Fast mode		300	ns
		Fast mode plus		120	ns
Rise Time of SDA Signal	t_{RDA}	Standard mode		1000	ns
		Fast mode	20	300	ns
		Fast mode plus		120	ns
Fall Time of SDA Signal[2]	t_{FDA}	Standard mode		300	ns
		Fast mode	20 x V_{DDIO}/ 5.5V	300	ns
		Fast mode plus	20 x V_{DDIO}/ 5.5V	120	ns
Data Valid Time	t_{VD}	Standard mode		3.45	µs
		Fast mode		900	ns
		Fast mode plus		450	ns
Data Valid Acknowledge Time	t_{VDA}	Standard mode		3.45	µs
		Fast mode		900	ns
		Fast mode plus		450	ns
Capacitive Load for SDA and SCL	C_{BUS}	Standard mode		400	pF
		Fast mode		400	pF
		Fast mode plus		550	pF

Notes:

Min/Max specifications are 100% production tested at TA=TJ=25°C, unless otherwise noted. Limits over the operating range are guaranteed by design.

Table 6: Electrical Characteristics (cont.)

Pin Configuration

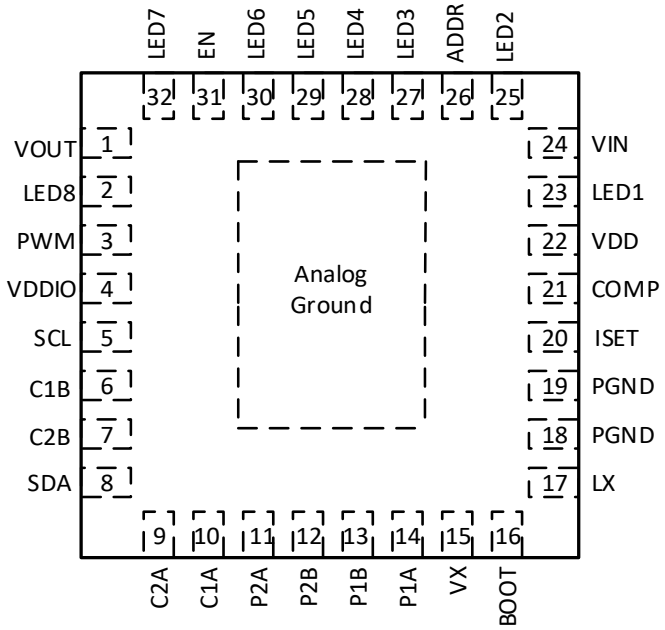


Figure 3:ARC3C0845 32-PIN QFN Top View

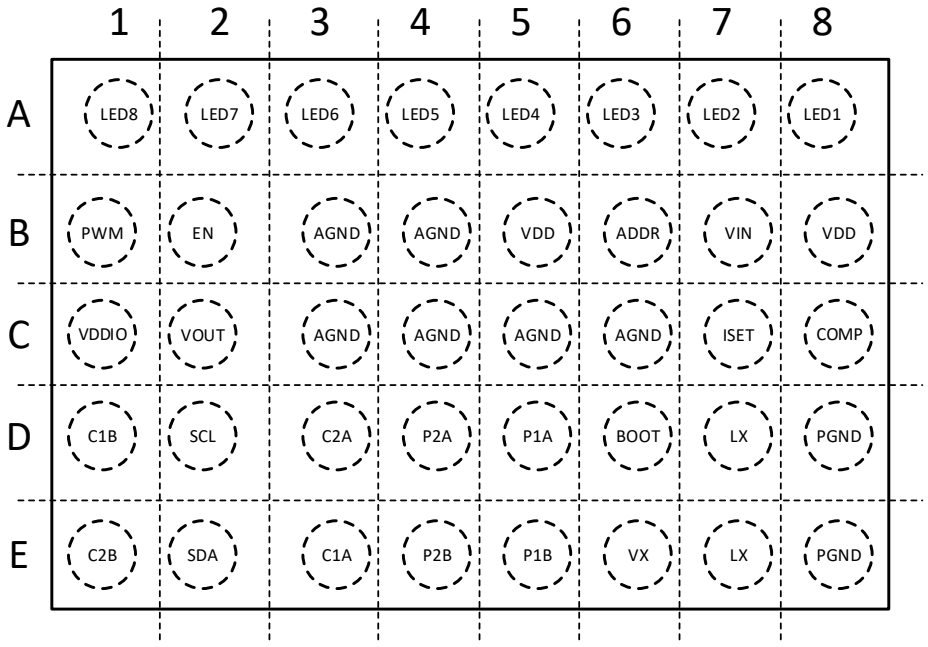


Figure 4: ARC3C0845W WLCSP40 Top View

Pin Descriptions

ARC3C0845 32P QFN PIN #	ARC3C0845W WLCSP40 PIN #	PIN NAME	DESCRIPTION
EP Pad	B3,B4,C3,C4,C5,C6	AGND	Analog and LED current sink ground, must tie externally to ground plane and to the PGND pins.
1	C2	VOUT	Power converter output voltage. Connect to the high side of all LED strings. Connect externally to COUT capacitor. See Component Selection for capacitor selection guideline.
2	A1	LED8	Individual LED current sink. Connect to the low side of individual LED strings.
3	B1	PWM	PWM dimming input for brightness control. Must be connected to VDD pin if not used.
4	C1	VDDIO	Digital IO supply voltage for I^2C interface, used as I2C VIH and VIL reference. Can be tied to the VDD pin. Connect to AGND to use non-I^2C interface.
5	D2	SCL	Serial Clock for I^2C bus. Also used in non-I2C mode to select between three different dimming modes.
6	D1	C1B	Charge pump fly capacitor positive node. Connect capacitor from C1B to P1B. See Component Selection for capacitor selection guideline.
7	E1	C2B	Charge pump fly capacitor positive node. Connect capacitor from C2B to P2B. See Component Selection for capacitor selection guideline.
8	E2	SDA	Serial Data for I2C bus. Also used in non-I2C mode to select between three different switching frequencies.
9	D3	C2A	Charge pump fly capacitor positive node. Connect capacitor from C2A to P2A.
10	E3	C1A	Charge pump fly capacitor positive node. Connect capacitor from C1A to P1A. See Component Selection for capacitor selection guideline.
11	D4	P2A	Charge pump fly capacitor phase node. Connect capacitor from P2A to C2A. See Component Selection for capacitor selection guideline.
12	E4	P2B	Charge pump fly capacitor phase node. Connect capacitor from P2B to C2B.
13	E5	P1B	Charge pump fly capacitor phase node. Connect capacitor from P1B to C1B.
14	D5	P1A	Charge pump fly capacitor phase node. Connect capacitor from P1A to C1A.
15	E6	VX	Charge pump input node, internally driven by the output of the boost converter. Connect a capacitor Cx between this pin and PGND. See Component Selection for capacitor selection guideline.

ARC3C0845 32P QFN PIN #	ARC3C0845W WLCSP40 PIN #	PIN NAME	DESCRIPTION
16	D6	BOOT	Bootstrap capacitor for the Boost stage high side FET. Connect a 22nF, 10V or higher capacitor from BOOT to LX.
17	D7,E7	LX	Fully synchronous switching node for the boost power inductor, which connects between LX and input voltage VIN. See Component Selection for inductor selection guideline.
18,19	D8,E8	PGND	Power Ground, must tie externally to ground plane and to the AGND EP pad. High current path.
20	C7	ISET	LED current setting pin. Connect a resistor from this pin to AGND to set the full scale LED current in non-I^2C mode or when the ISET_EXT bit is set to 1 in I^2C mode.
21	C8	COMP	External compensation pin. See Switching Converter Compensation for detail.
22	B5,B8	VDD	Internal LDO output pin. Connect a capacitor CVDD between this pin and PGND. See Component Selection for capacitor selection guideline.
23	A8	LED1	Individual LED current sink. Connect to the low side of individual LED strings.
24	B7	VIN	Input voltage, battery power supply pin.
25	A7	LED2	Individual LED current sink. Connect to the low side of individual LED strings.
26	B6	ADDR	Sets lower three bits of the I2C slave address. Tie to AGND pin for '000'. Leave floating for '010'. Tie to VDD pin for '101'.
27	A6	LED3	Individual LED current sink. Connect to the low side of individual LED strings.
28	A5	LED4	Individual LED current sink. Connect to the low side of individual LED strings.
29	A4	LED5	Individual LED current sink. Connect to the low side of individual LED strings.
30	A3	LED6	Individual LED current sink. Connect to the low side of individual LED strings.
31	B2	EN	Enable input.
32	A2	LED7	Individual LED current sink. Connect to the low side of individual LED strings.

Table 7: Pin Description

Operating Voltage Range and Charge Pump Ratio

The ARC3C0845/ARC3C0845W uses a 2X/3X charge-pump to improve efficiency. The charge pump architecture requires the input voltage to be less than the output voltage divided by 2.15x in 2X mode and 3.2x in 3X mode:

$$\text{For 2X Charge Pump Mode} = Vin \leq \frac{Vout}{2.15}$$

$$\text{For 3X Charge Pump Mode} = Vin \leq \frac{Vout}{3.2}$$

A graph of the output voltage versus input voltage is shown in Figure 5 In addition to maintaining the minimum Vout/Vin requirement for 2X/3X charge pump mode, the graph also shows a region called “Out of Regulation Zone for 2X/3X Charge Pump Mode” that is not supported for normal operation. Failure to maintain the minimum Vout/Vin requirement or attempting to operate in the “Out of Regulation Zone for 2X/3X Charge Pump Mode” may result in the ARC3C0845/ARC3C0845W having lower efficiency, faulting off and/or requiring a re-start. To prevent VX over voltage condition, the charge pump must be operating in 3X charge pump mode for VOUT>40V.

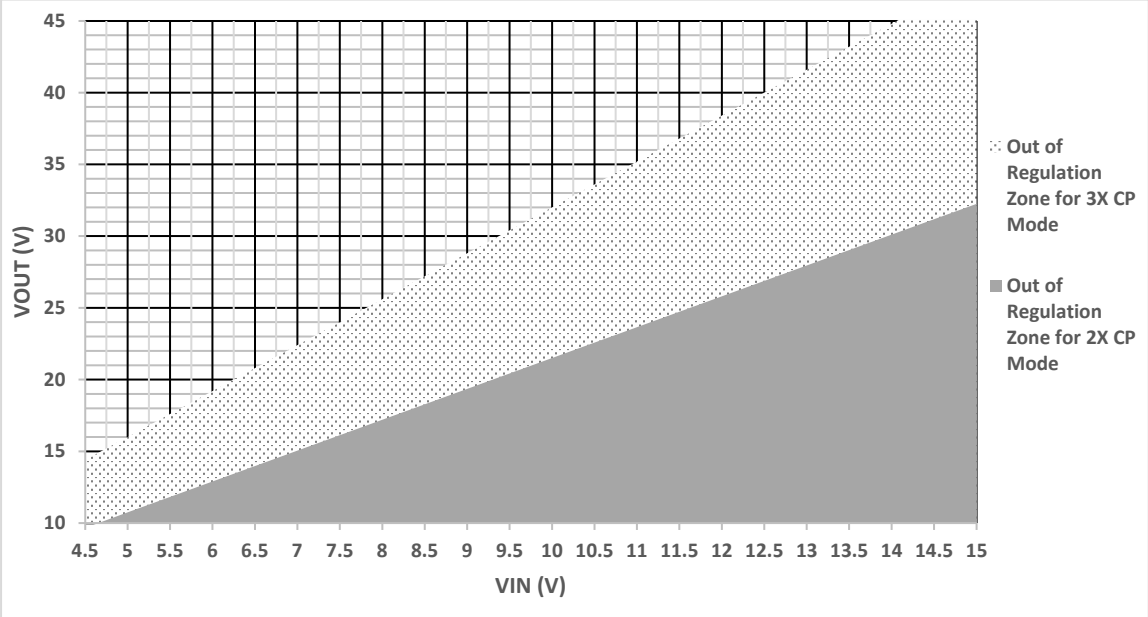


Figure 5: V_{OUT} vs. V_{IN} requirement

The ARC3C0845/ARC3C0845W has an automatic feature (AUTOCP) to switch between 2X/3X charge pump depending on VIN and VOUT conditions to optimize efficiency. This feature is enabled by setting the AUTO_CP_RATIO register bit to 0. The charge pump ratio can also be set to a fixed 2X or 3X ratio by setting the AUTO_CP_RATIO bit to 1 to and use the SEL_CP_RATIO to select 2X or 3X charge pump.

When using the AUTOCP feature, it is important the 2X to 3X charge pump switch over does not cause out of regulation issue for the application operating range. For example, a VIN=12V and the LED current is increasing to push the VOUT from 37V into 38V. The charge pump would transition from 2X into 3X ratio. In 2x ratio, the minimum VOUT requirement to prevent out of regulation is 25.8V, which is below the 37V operation condition. But in 3X ratio, the minimum VOUT requirement to prevent out of regulation is 38.4V, which is over the 38V operation condition and causes out of regulation issue. With this example, it is recommended to operate the charge pump in a fixed 2X mode to prevent out of regulation issues. Please see Table 8 for the charge pump ratio in the AUTOCP mode for different VIN and VOUT conditions.

The charge pump is automatically switched from 2X to 3X or 3X to 2X when the VIN and/or VOUT conditions cross over the threshold. The grayed out area indicates out of regulation operation for 3X mode and it is recommended to set the charge pump operation to fixed 2X CP mode. The blacked out area indicates out of regulation operation for 2X mode. When VOUT is 40V or higher, the charge pump must set to fixed 3X CP mode to avoid overvoltage condition on the VX pin.

VOUT\VIN	4.5	5	5.5	6	6.5	7	7.5	8	8.5	9	9.5	10	11	12	13
20	3X	3X	3X	2X	2X	2X	2X	2X	2X	2X					
21	3X	3X	3X	3X	2X	2X	2X	2X	2X	2X	2X				
22	3X	3X	3X	3X	2X	2X	2X	2X	2X	2X	2X	2X			
23	3X	3X	3X	3X	3X	2X	2X	2X	2X	2X	2X	2X			
24	3X	3X	3X	3X	3X	2X	2X	2X	2X	2X	2X	2X	2X		
25	3X	3X	3X	3X	3X	3X	2X	2X	2X	2X	2X	2X	2X		
26	3X	3X	3X	3X	3X	3X	2X	2X	2X	2X	2X	2X	2X	2X	
27	3X	3X	3X	3X	3X	3X	3X	2X	2X	2X	2X	2X	2X	2X	
28	3X	3X	3X	3X	3X	3X	3X	2X	2X	2X	2X	2X	2X	2X	2X
29	3X	3X	3X	3X	3X	3X	3X	3X	2X	2X	2X	2X	2X	2X	2X
30	3X	3X	3X	3X	3X	3X	3X	3X	3X	2X	2X	2X	2X	2X	2X
31	3X	3X	3X	3X	3X	3X	3X	3X	3X	2X	2X	2X	2X	2X	2X
32	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	2X	2X	2X	2X	2X
33	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	2X	2X	2X	2X	2X
34	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	2X	2X	2X	2X
35	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	2X	2X	2X	2X
36	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	2X	2X	2X
37	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	2X	2X	2X
38	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X
39	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X
40	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X
41	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X
42	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X
43	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X
44	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X
45	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X	3X

Table 8: AUTOCP Charge Pump Ratio at Different V_{OUT} and V_{IN} Conditions

(Grayed-out area indicates out of regulation operation for 3X CP operation

Blacked-out area indicates out of regulation operation for 2X CP operation)

Functional Block Diagram

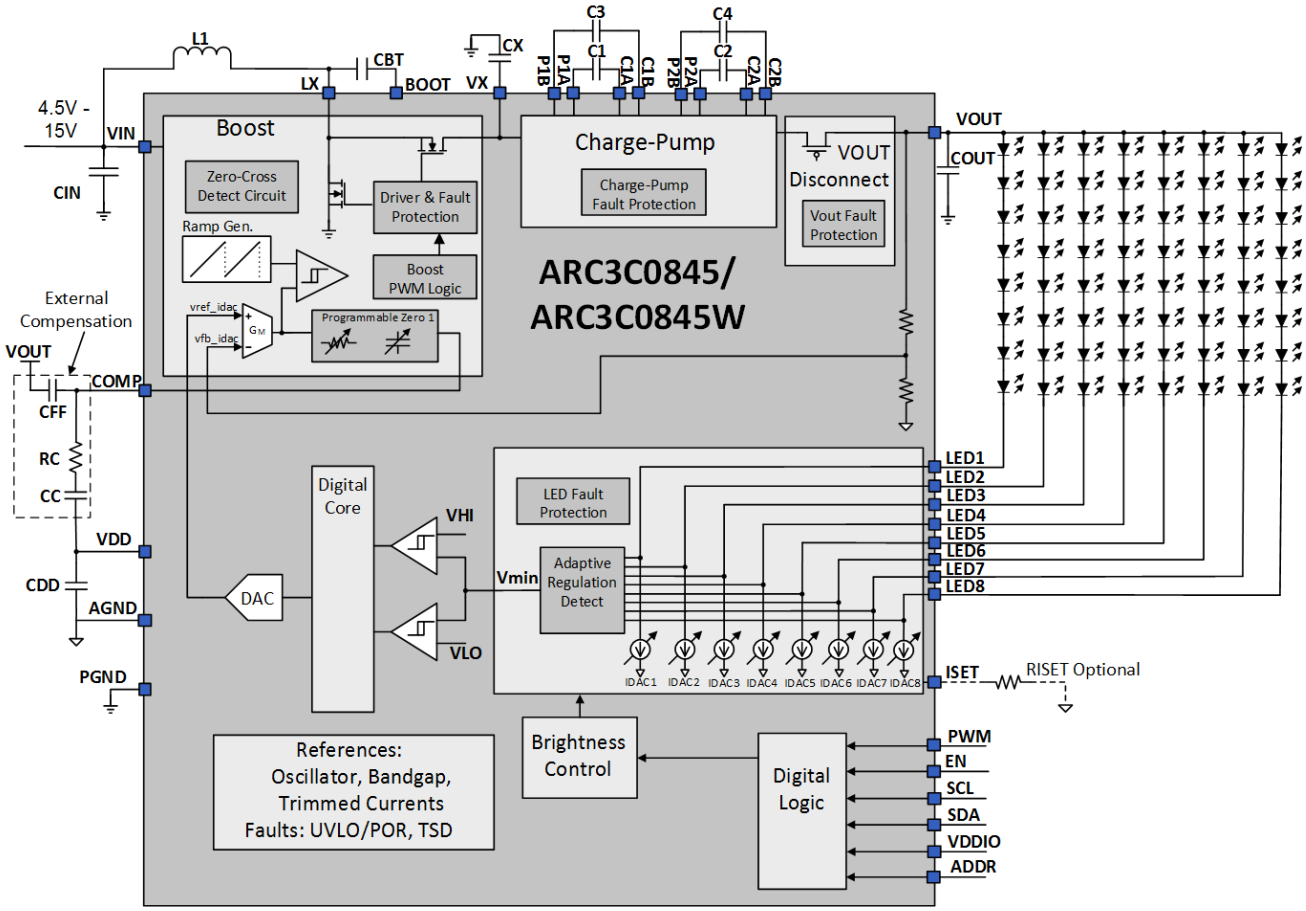


Figure 6: Block Diagram

Application Circuit

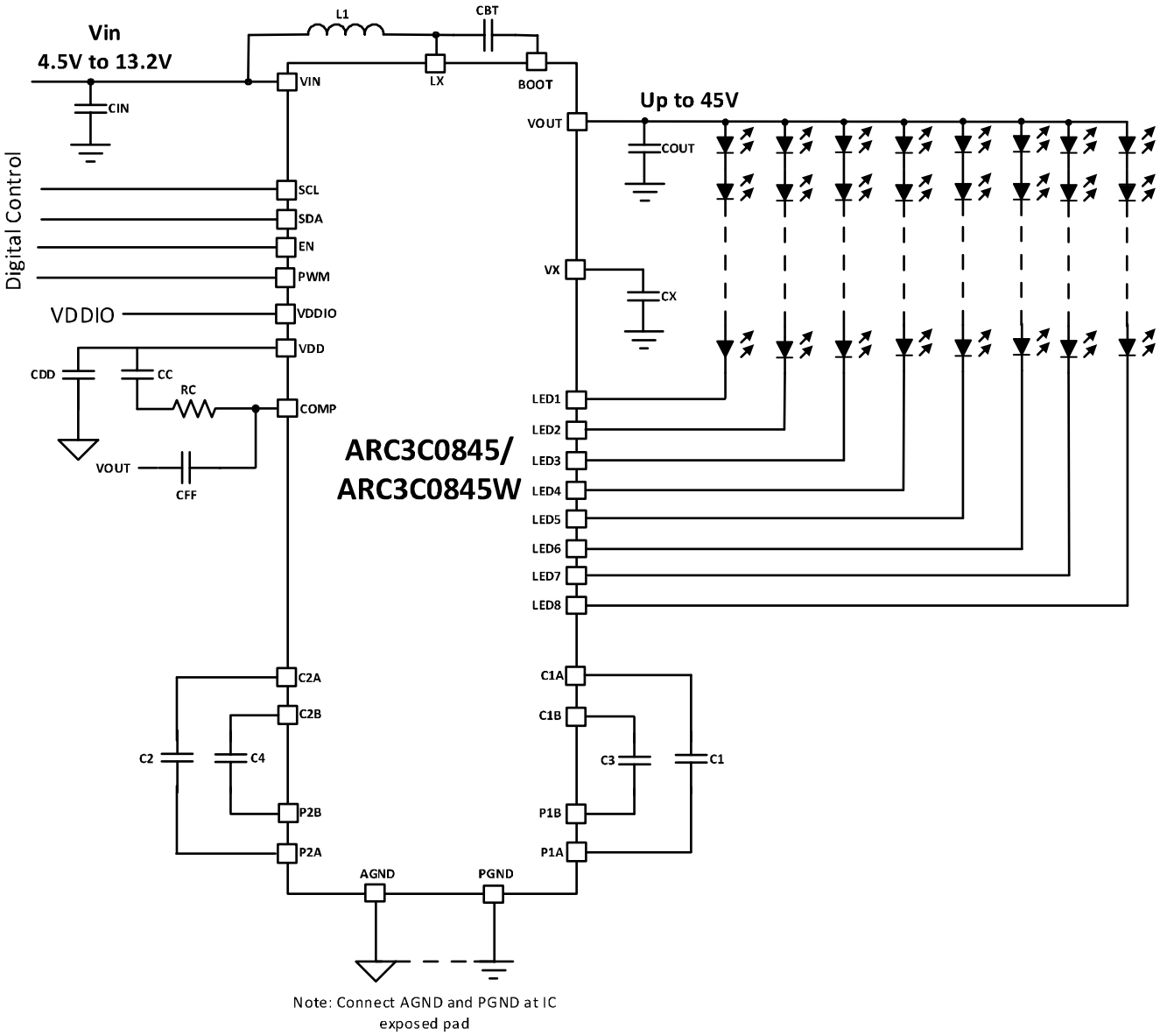


Figure 7: Application Schematic for I²C interface

Note: Connect PGND and AGND at IC's exposed pad (EP) for ARC3C0845 or at IC's AGND bumps for ARC3C0845W

Typical Characteristics

Unless otherwise specified: Cout=4.7 µF, LED VF=3V at 20 mA (typ.) analog dimming

LED efficiency – 2-cell only input voltage with 2.2 µH, 1.2 mm high chip inductor (Part # DFE322512F-2R2M), 931 kHz boost frequency

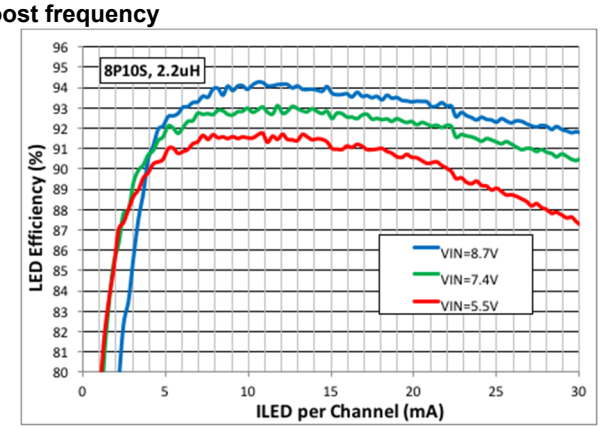


Figure 8: 8P10s LED Efficiency, 2.2 µH Inductor

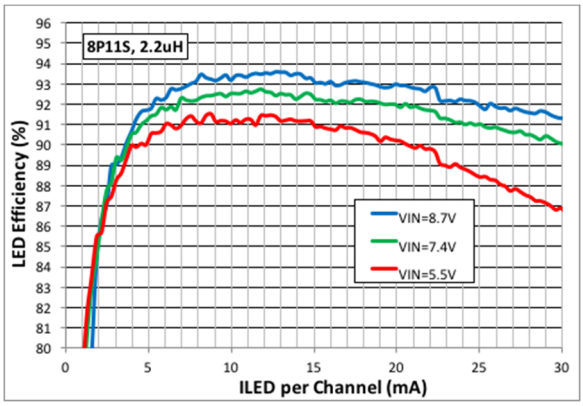


Figure 9: 8P11s LED Efficiency, 2.2 µH Inductor

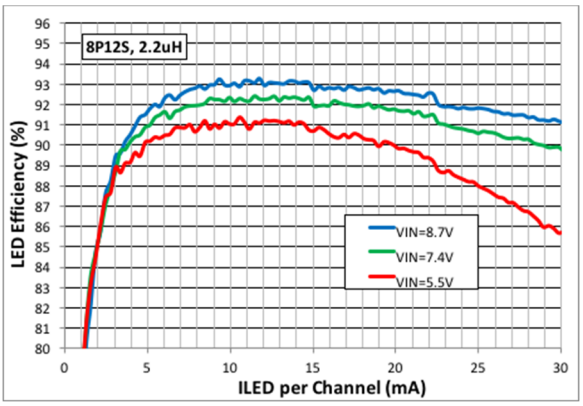


Figure 10: 8P12s LED Efficiency, 2.2 µH Inductor

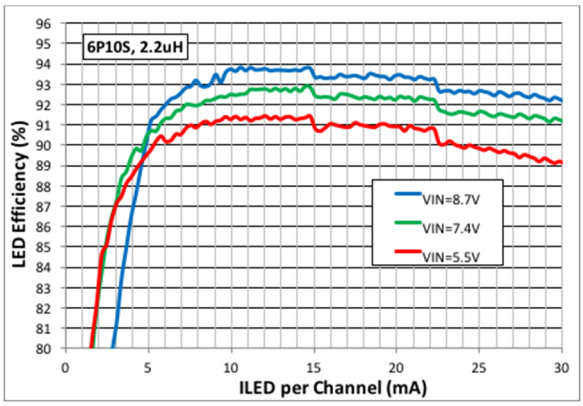


Figure 11: 6P10s LED Efficiency, 2.2 µH Inductor

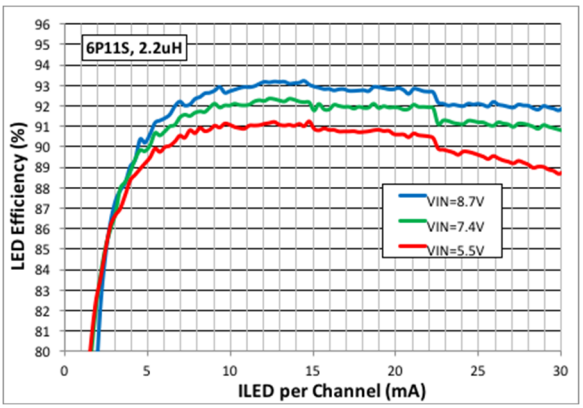


Figure 12: 6P11s LED Efficiency, 2.2 µH Inductor

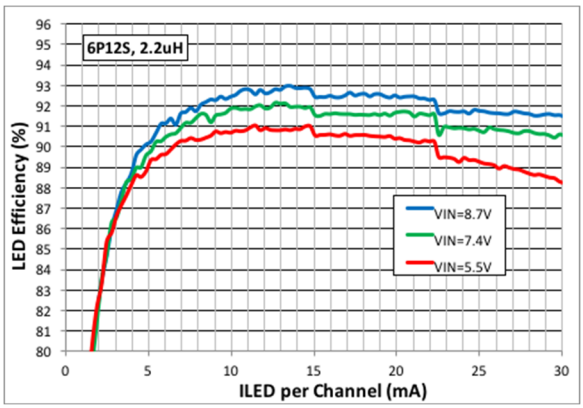


Figure 13: 6P12s LED Efficiency, 2.2 µH Inductor

Typical Characteristics

Unless otherwise specified: Cout=4.7 µF, LED VF=3V at 20mA (typ.), analog dimming

LED efficiency – 2-cell only input voltage with 4.7 µH, 1.2 mm high chip inductor (Part # DFE322512F-4R7M), 787 kHz boost frequency

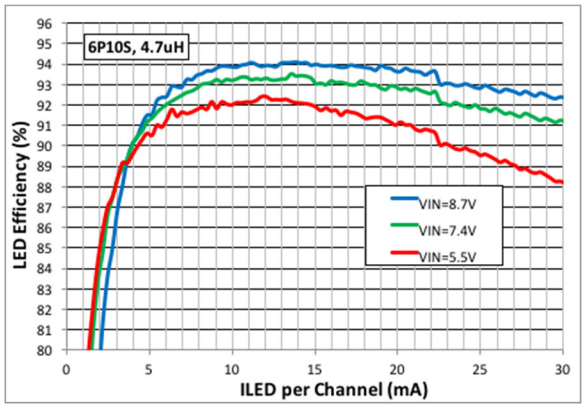


Figure 14: 6P10s LED Efficiency, 4.7 µH Inductor

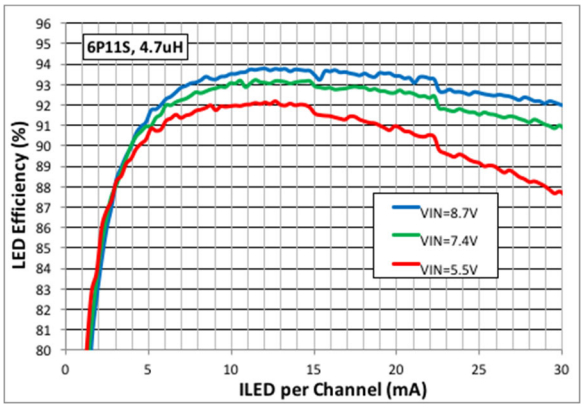


Figure 15: 6P11s LED Efficiency, 4.7 µH Inductor

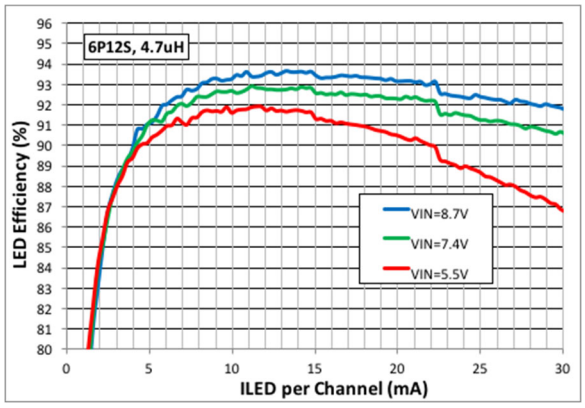


Figure 16: 6P12s LED Efficiency, 4.7 µH Inductor

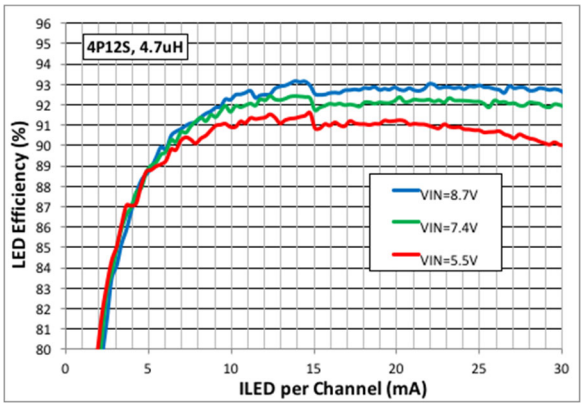


Figure 17: 4P12s LED Efficiency, 4.7 µH Inductor

Typical Characteristics

Unless otherwise specified: Cout=4.7 µF, LED V=3FV at 20 mA (typ.), analog dimming

LED efficiency – 3-cell only input voltage with 6.8 µH, 1.2 mm high chip inductor (Part # DFE322512F-6R8M), 731 kHz boost frequency

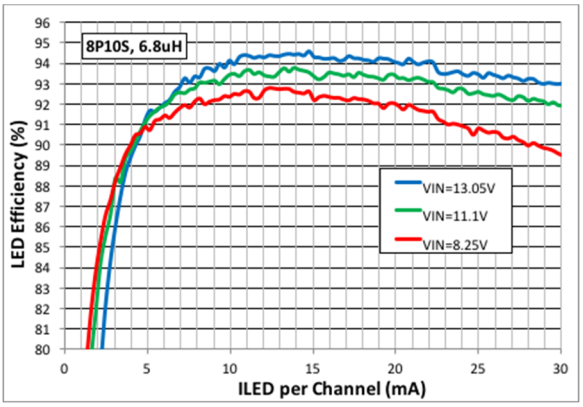


Figure 18: 8P10s LED Efficiency, 6.8 µH Inductor

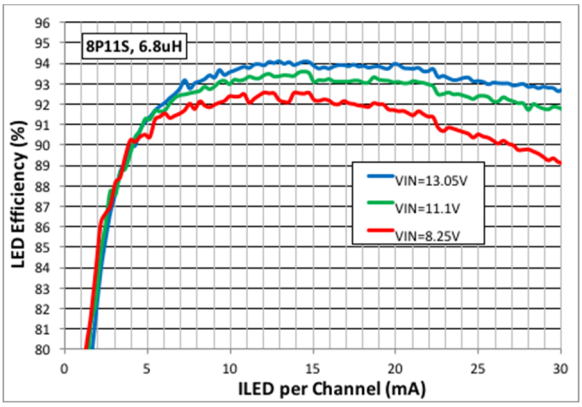


Figure 19: 8P11s LED Efficiency, 6.8 µH Inductor

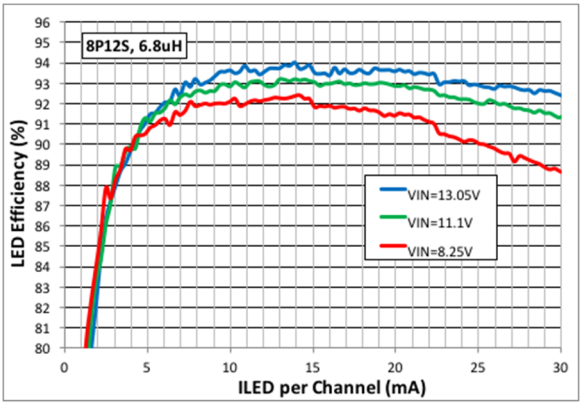


Figure 20: 8P12s LED Efficiency, 6.8 µH Inductor

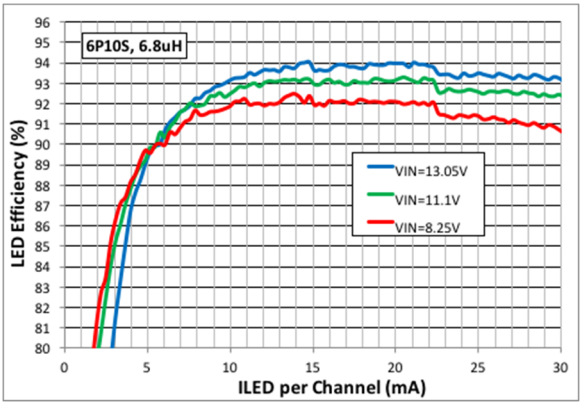


Figure 21: 6P10s LED Efficiency, 6.8 µH Inductor

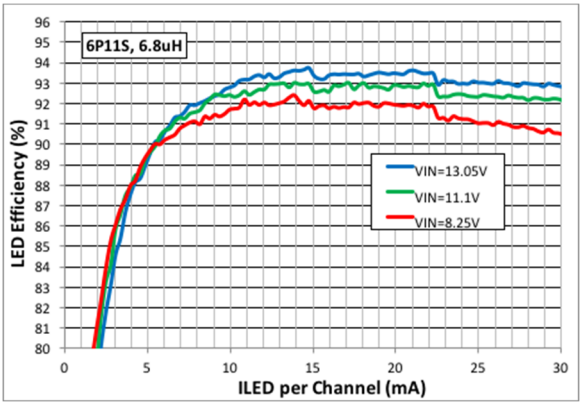


Figure 22: 6P11s LED Efficiency, 6.8 µH Inductor

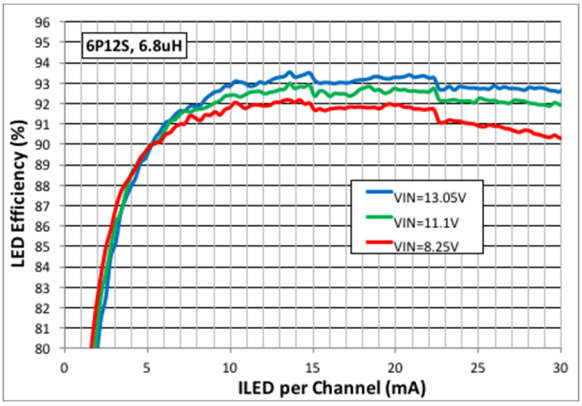


Figure 23: 6P12s LED Efficiency, 6.8 µH Inductor

Typical Characteristisc

Unless otherwise specified: Cout=4.7 µF, LED VF=3V at 20 mA (typ.), analog dimming

LED efficiency – 3-cell only input voltage with 6.8 µH (Part # DFE322512F-6R8M) and 10 µH (Part # DFE322512F-100M) 1.2 mm high chip inductors, 731 kHz boost frequency

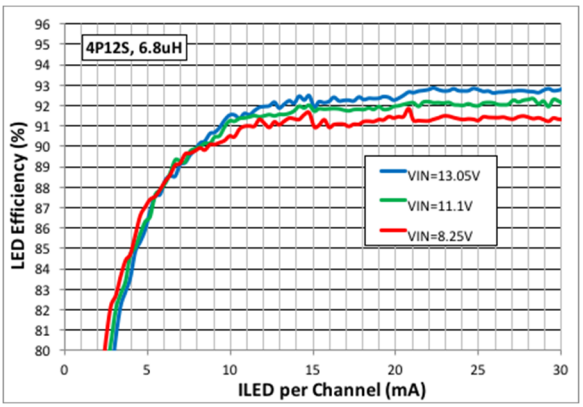


Figure 24: 4P12s LED Efficiency, 6.8 µH Inductor

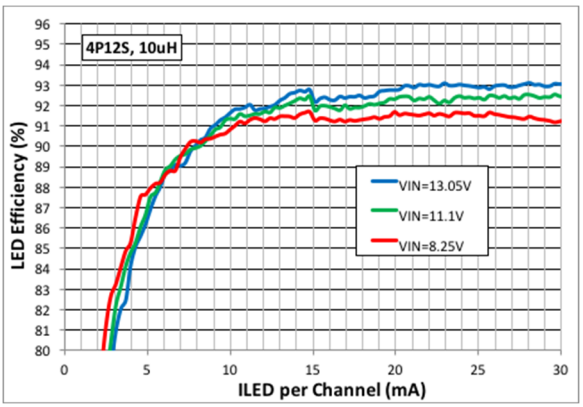


Figure 25: 4P12s LED Efficiency, 10 µH Inductor

Typical Characteristics

Unless otherwise specified: Cout=4.7 µF, LED VF=3V at 20 mA (typ.), analog dimming

LED efficiency –2-cell and 3-cell NVDC input voltage with 3.3 µH (Part # DFE322512F-3R3M), 1.2 mm inductor, 853 kHz boost frequency

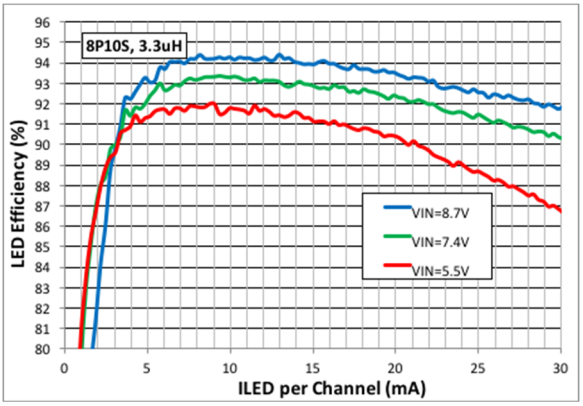


Figure 26: 2S, 8P10s LED Efficiency, 3.3 µH Inductor

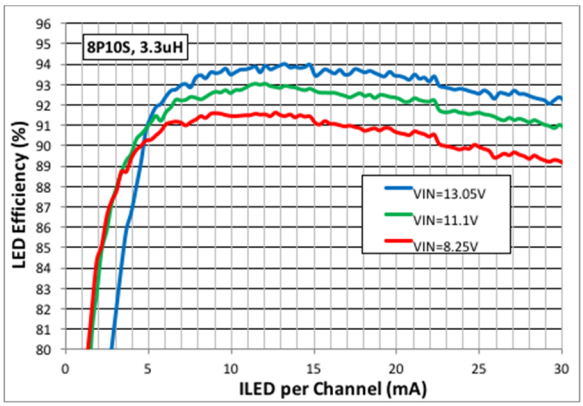


Figure 27: 3S, 8P10s LED Efficiency, 3.3 µH Inductor

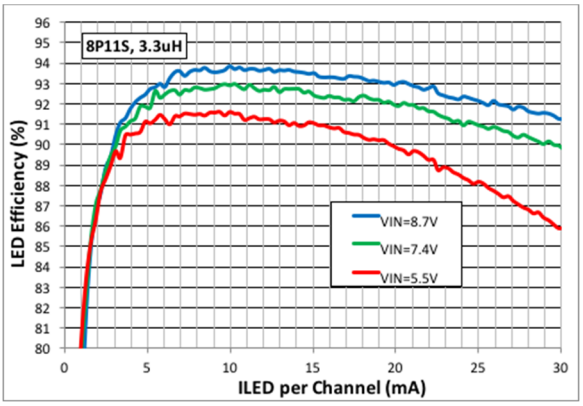


Figure 28: 2S, 8P11s LED Efficiency, 3.3 µH Inductor

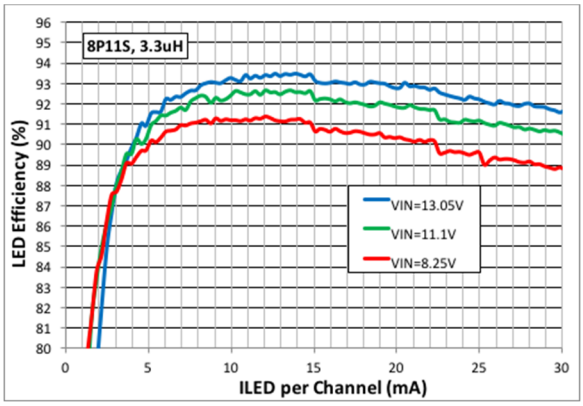


Figure 29: 3S, 8P11s LED Efficiency, 3.3 µH Inductor

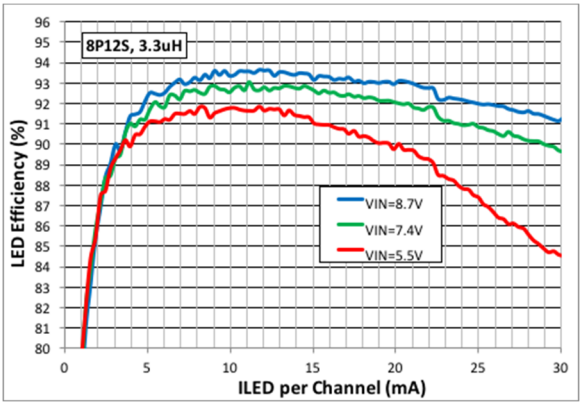


Figure 30: 2S, 8P12s LED Efficiency, 3.3 µH Inductor

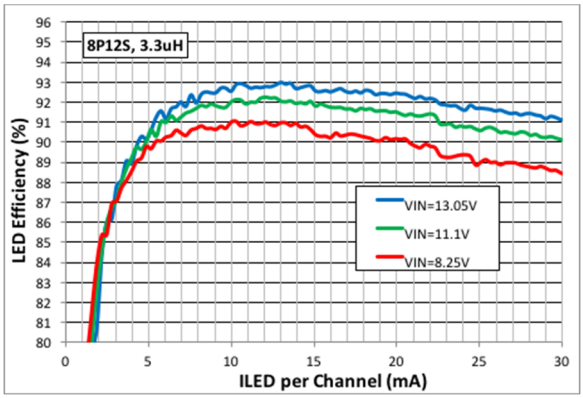


Figure 31: 3S, 8P12s LED Efficiency, 3.3 µH Inductor

Typical Characteristics

Unless otherwise specified: Cout=4.7 µF, LED VF=3V at 20 mA (typ.), analog dimming

LED Efficiency – 2-cell and 3-cell NVDC input voltage with 3.3 µH (Part # DFE322512F-3R3M), 1.2 mm inductor, 853 kHz boost frequency

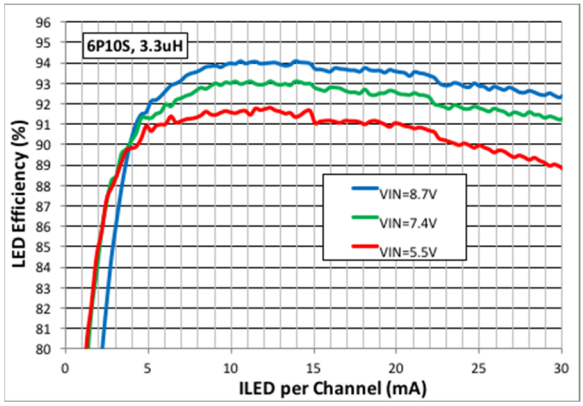


Figure 32: 2S, 6P10s LED Efficiency, 3.3 µH Inductor

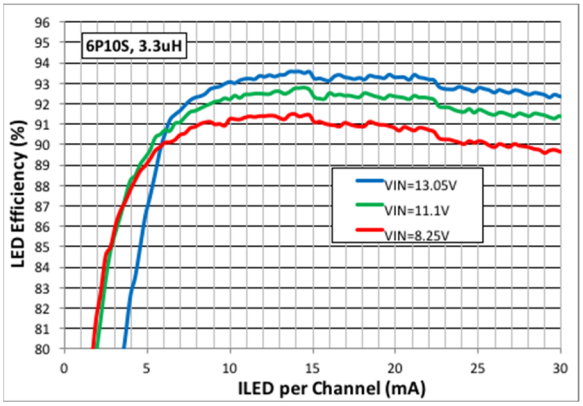


Figure 33: 3S, 6P10s LED Efficiency, 3.3 µH Inductor

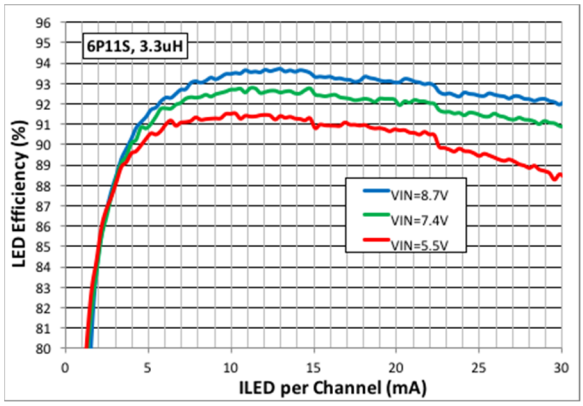


Figure 34: 2S, 6P11s LED Efficiency, 3.3 µH Inductor

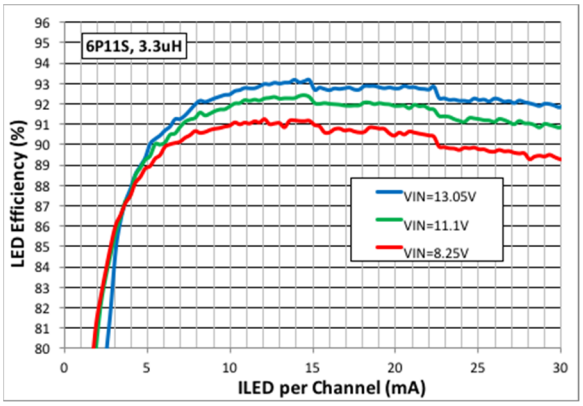


Figure 35: 3S, 6P11s LED Efficiency, 3.3 µH Inductor

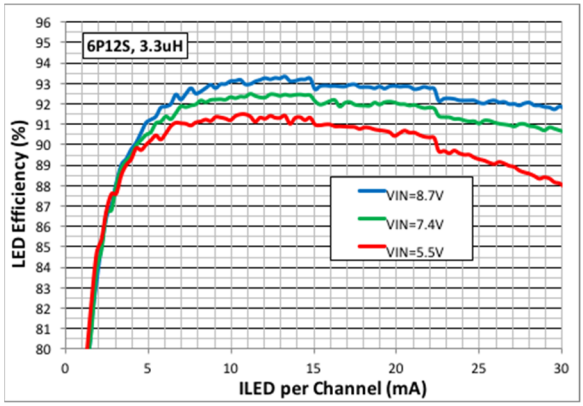


Figure 36: 2S, 6P12s LED Efficiency, 3.3 µH Inductor

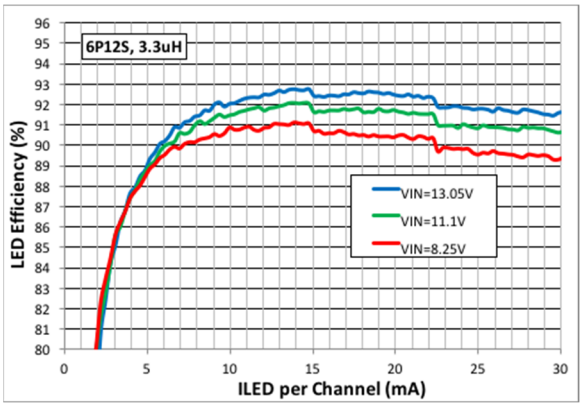


Figure 37: 3S, 6P12s LED Efficiency, 3.3 µH Inductor

Typical Characteristics

Unless otherwise specified: Cout=4.7 µF, LED VF=3V at 20 mA (typ.), analog dimming

LED efficiency – 2-cell and 3-cell NVDC input voltage with 3.3 µH (Part # DFE322512F-3R3M), 1.2 mm inductor, 853 kHz boost switching frequency

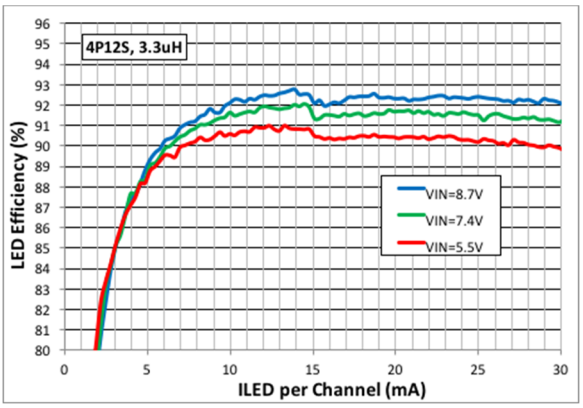


Figure 38: 2S, 4P12s LED Efficiency, 3.3 µH Inductor

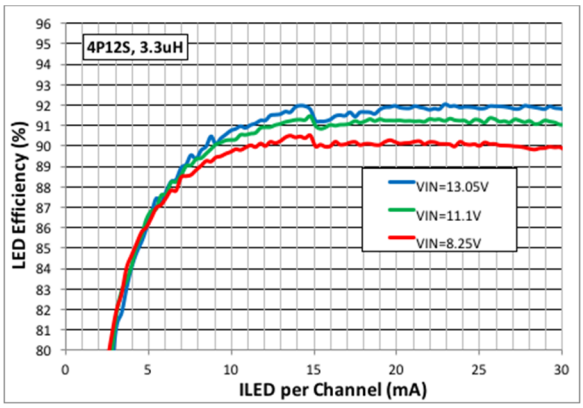


Figure 39: 3S, 4P12s LED Efficiency, 3.3 µH Inductor

LED Current Sinks

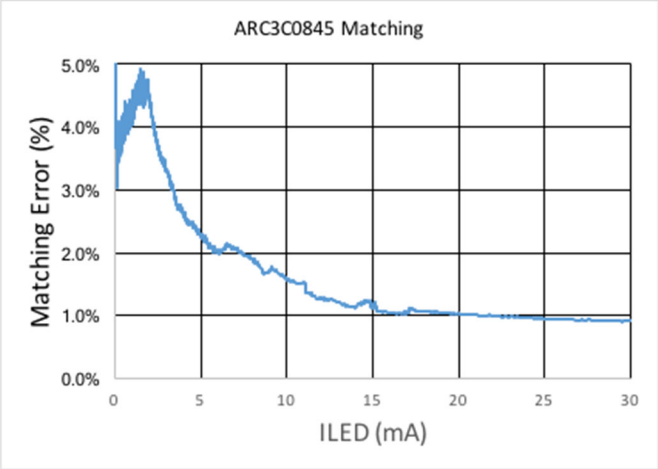


Figure 40: LED Mismatch – Linear Mode

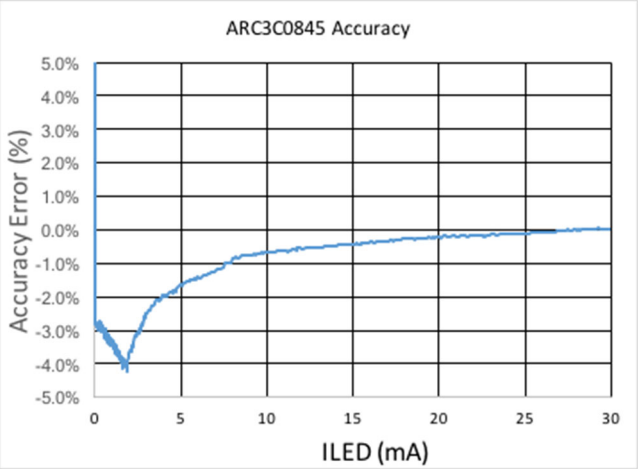


Figure 41: LED Accuracy – Linear Mode

Startup Characteristics

Unless otherwise specified: Cout=4.7 µF, LED VF=3V at 20 mA (typ.), analog dimming

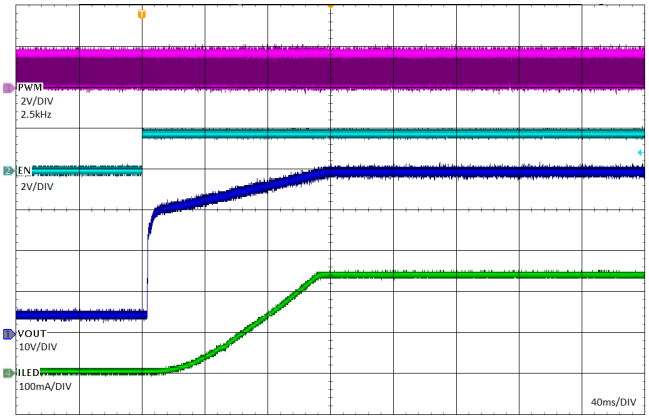


Figure 42: Startup Under 99% PWM Condition. 8P12S Configuration. Vin=7.4V, 3X Charge Pump Ratio

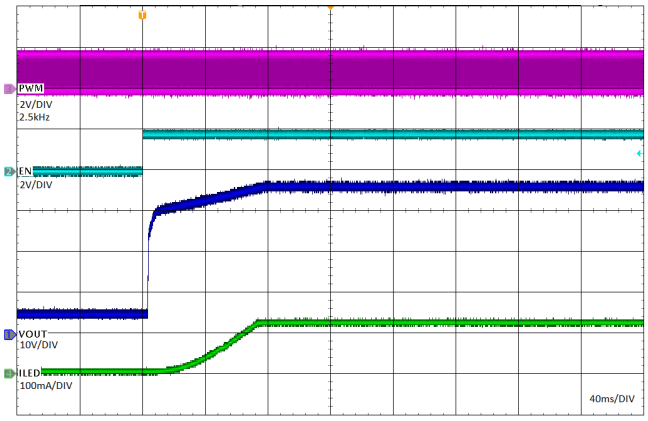


Figure 43: Startup Under 50% PWM Condition. 8P12S Configuration. Vin=7.4V, 3X Charge Pump Ratio

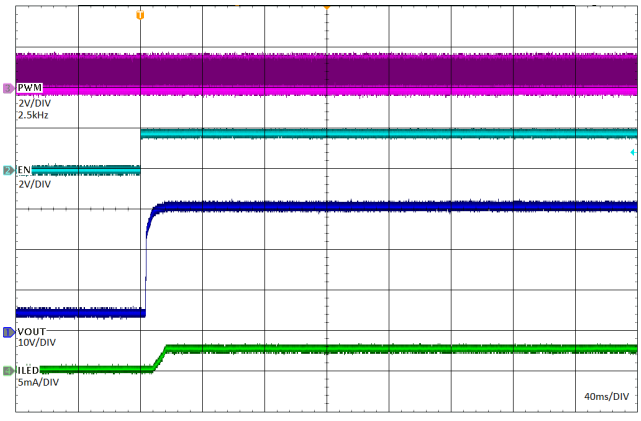


Figure 44: Startup Under 1% PWM Condition. 8P12S Configuration. Vin=7.4V, 3X Charge Pump Ratio

Startup Characteristics

Unless otherwise specified: Cout=4.7 µF, LED VF=3V at 20 mA (typ.), analog dimming

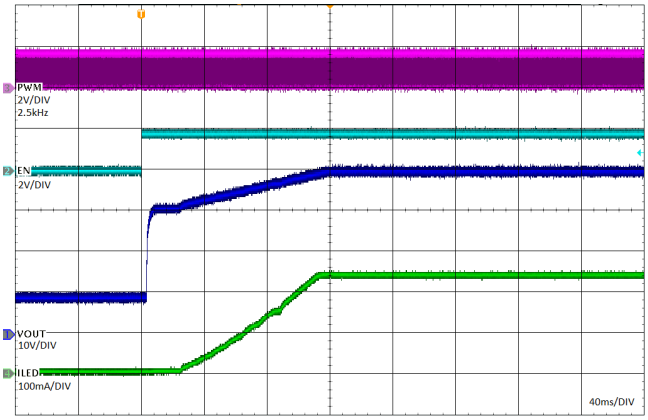


Figure 45: Startup Under 99% PWM Condition. 8P12S Configuration. Vin=11.1V, 2X Charge Pump Ratio

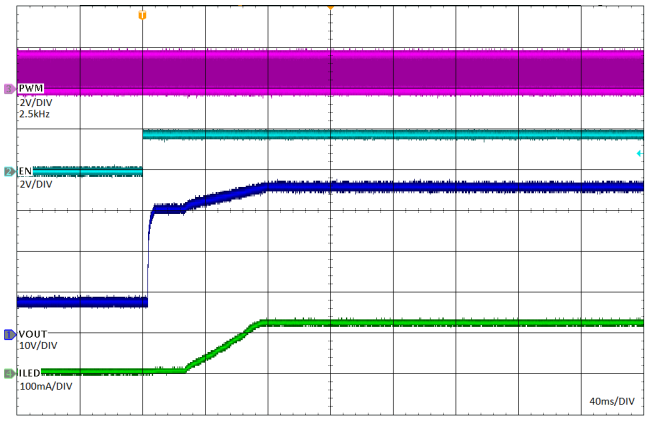


Figure 46: Startup Under 50% PWM Condition. 8P12S Configuration. Vin=11.1V, 2X Charge Pump Ratio

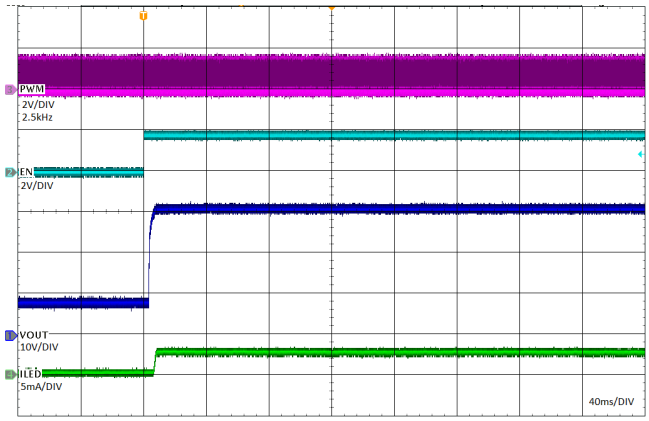


Figure 47: Startup Under 1% PWM Condition. 8P12S Configuration. Vin=11.1V, 2X Charge Pump Ratio

Thermal Performance

Unless otherwise specified: Cout=4.7 µF, LED VF=3V at 20 mA (typ.), analog dimming

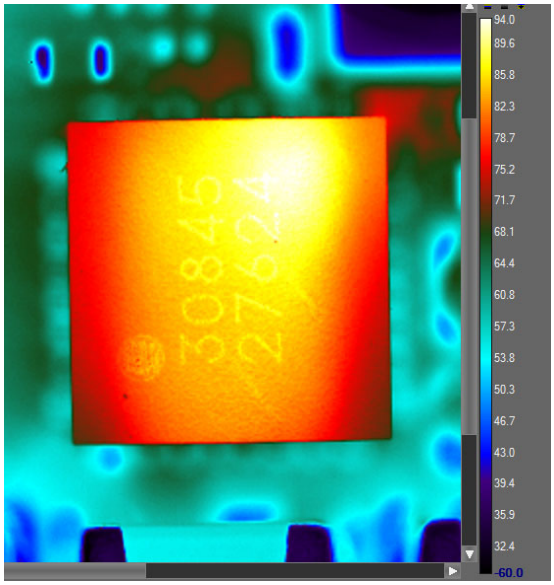


Figure 48: ARC3C0845 Thermal Performance

8p12s configuration, 38.5 VOUT, 240 mA, 5.5VIN, 1.5W Power Dissipation,

1.2mm 4.7 µH Inductor (DFE322512F-4R7M, Ambient Temperature 23.7°C

Maximum temperature is 94°C close to the LX and PGND pins of the package

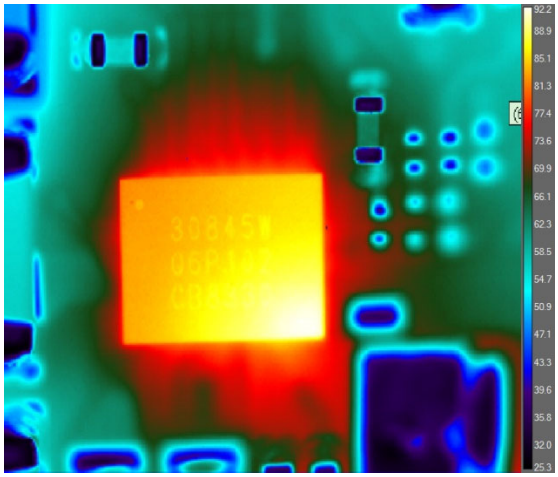


Figure 49: ARC3C0845W Thermal Performance

8p12s configuration, 37.5 VOUT, 240 mA, 5.5VIN, 1.45W Power Dissipation,

1.2mm 4.7 µH Inductor (DFE322512F-4R7M, Ambient Temperature 23.5°C

Maximum temperature is 92.2°C close to the LX and PGND bumps of the package

Detailed Description

The ARC3C0845/ARC3C0845W utilizes a proprietary architecture with a charge pump driven by a synchronous boost converter to achieve very high peak efficiencies and superior efficiency over the two-cell/three-cell lithium battery input voltage range. This architecture further realizes excellent performance across a range of LED forward voltages, allowing freedom in the selection of LEDs.

The ARC3C0845/ARC3C0845W supports 1 to 8 LED strings. Unused LEDx pins should be tied to ground. This provides maximum design flexibility for wide variety of LCD screens.

The ARC3C0845/ARC3C0845W supports both I^2C and non-I^2C operation. It can be configured through I2C interface or external settings, and allows combined I^2C command settings with the PWM signal to adjust LED brightness.

The ARC3C0845/ARC3C0845W provides a full set of protection features to guarantee robust system operation, which include: input battery voltage under voltage lockout (UVLO), thermal shutdown (TSD), boost and charge pump over current protection (OCP), boost and charge pump output over-voltage and under-voltage protection (OVP and UVP), and LED open and short detection.

Input Sequencing Requirements

V_{DDIO} determines if the device starts up in I^2C or non-I^2C mode. This input must be taken high (for I^2C mode) or low (for non-I^2C mode) before both V_{IN} and EN are asserted. V_{DDIO} must not be left floating. With V_{DDIO} already established, then both V_{IN} and EN can be asserted high to enable the internal VDD LDO. When V_{DD} is above the VDD UVLO threshold (3V typical) for ~100us, the ARC3C0845/ARC3C0845W detects the V_{DDIO} level to determine device is in I^2C or non-I^2C mode. Then the ARC3C0845/ARC3C0845W becomes operational. In I^2C mode the first command can be given 1ms after both V_{IN} and EN are asserted.

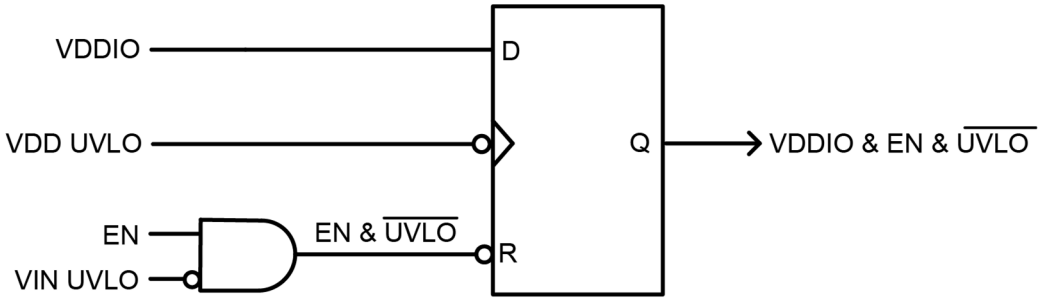


Figure 50: Input Sequencing Logic Diagram

If the part is enabled in non-I^2C mode, VDDIO needs to be connected to the GND plane with a low inductance trace. In I^2C mode, V_{DDIO} should be connected to the same pull up voltage used by SDA and SCL signals as the SDA and SCL VIH and VIL are referenced to V_{DDIO}. If this voltage drops too low, I^2C communication will stop; however, the device will retain all its register values. I^2C communication can resume 5µs after V_{DDIO} becomes stable within its allowable voltage range.

In I^2C mode, SCL and SDA serve as clock and data lines. In non-I^2C mode SCL can be used to select three different dimming modes and SDA can be used to select three different boost switching frequencies depending on whether the pins are logic low, logic high or floating.

The sequence for the PWM pin does not matter. It can be switching according to the application requirements while all other signals are being turned on and off. Please see Table 9 for further clarification on various ARC3C0845/ARC3C0845W input signals.

VIN	EN	VDDIO	SCL	SDA	PWM	DEVICE STATUS
Low	-	-	-	-	Switching	Non-operational
High	Low	-	-	-	Switching	Non-operational
High	High	High	Clock	Data	Switching	I^2C operation
Note: "-" Denotes level can be either High or Low and does not affect operation						

Table 9: Input Signals

Under-voltage Lockout (UVLO)

ARC3C0845/ARC3C0845W provides continuous monitoring of the VIN input. When VIN voltage drops below approximately 4.3V, the ARC3C0845/ARC3C0845W will immediately shut down.

Output Over-voltage and Under-voltage Protection

The ARC3C0845/ARC3C0845W protects against excessive output voltage by initiating over-voltage protection (VOUT_OVP) when VOUT rises above the over-voltage threshold V_{OUT_OVP}. When a VOUT OVP occurs, the VOUT_OVP bit of the STATUS1 register is updated to a 1, and the ARC3C0845/ARC3C0845W turns off the boost converter. The boost converter automatically restarts after an OVP event when VOUT decreases below the threshold plus 0.5V typical hysteresis.

The over-voltage threshold can be configured through OVP_TH[3:0] bits in COMMAND register. The accuracy of each over-voltage threshold is +/-5%.

VOUT_OVP_SEL[3:0]	VOUT OVER-VOLTAGE THRESHOLD (V)
0000	47.5
0001	45.625
0010	43.75
0011	41.875
0100	40.0
0101	38.125
0110	36.25
0111	34.375
1000	32.5
1001	30.625
1010	28.75
1011	26.875
1100	25.0
1101	23.125
1110	21.25
1111	19.375

Table 10: Over-Voltage Threshold

In non-I²C mode, the OVP threshold is fixed at 47.5V (factory default) but can be programmed to a different level in the non-volatile memory.

The user should select the output over-voltage threshold with enough voltage margin above the highest expected operating VOUT voltage in the application, in order to guarantee proper LED open or grounded string fault detection. The highest expected operating VOUT voltage is a function of the number of series LEDs used, the highest LED forward voltage expected and the regulation voltage at the LED pins during the maximum LED current used in the application per channel.

Reset and Standby Functions

Table 11 explains all RESET and Standby states when the part uses the I²C interface.

For all modes: UVLO high = POR IC (entire chip shut-down).

EN PIN LOGIC LEVEL	I2C_STANDBY	LEDEN[8:1]	RESET	STATUS	INTERNAL BLOCK ON	REGISTER
0	-	-	-	OFF	None	Cleared
1	0	0	0	Ready	References ON, Boost/CP off, LED drivers on standby	I²C accessible
1	0	>0	0	ON	All ON	I²C accessible
1	1	-	-	Standby	All off except UVLO + critical reference circuits	I²C accessible
1	0	-	1 (self clearing)	Reset -> Ready (self clearing)	Ready state after self-clearing reset	Cleared
Note: "-" Denotes that level can be either High or Low and does not affect operation.						

Table 11: RESET and Standby States for I²C Interface

The STATUS1 and STATUS2 register bits are all cleared upon read, so repeated read-back of a logic-high fault bit indicates the fault event remains persistent.

Boost Output Over-voltage and Under-voltage Protection

The ARC3C0845/ARC3C0845W monitors the boost output (VX) voltage by initiating over-voltage protection (VX_OV) when VX rises above a typical over-voltage threshold of 17V (3x charge pump ratio) or 22.25 (2x charge pump ratio). When a VX OVP occurs, the VX_OVP bit of the STATUS1 register is updated to a 1, and the ARC3C0845/ARC3C0845W turns off the boost converter. The boost converter automatically restarts after a VX_OV event when VX decreases below the VX_OV threshold plus a 0.5V typical hysteresis.

If the boost output voltage (VX) falls below the VIN voltage plus a VIN-proportional offset after the LED current sinks have turned on, the ARC3C0845/ARC3C0845W will shut down the switching converter and the LED current sinks immediately and register bit VX_UV in STATUS1 register is set to 1. The switching converter and the LED current sinks remain latched off and will not start unless the part is shutdown or reset as explained in Table 11.

The ARC3C0845/ARC3C0845W is able to detect a missing or unconnected inductor upon startup by monitoring the boost output prior to enabling the switching converter and LED strings. When an inductor open is detected, the switching converter and LED strings remain off and both the SS_TIMEOUT and VX_UV bits in the STATUS1 register will be set and are cleared upon read.

Soft-start Time-out

The ARC3C0845/ARC3C0845W implements a soft-start time out fault. Depending on the CP ratio setting, if the output voltage doesn't rise above 2x/3x the input voltage within 10ms, the switching converter and the LED current sinks are disabled. The SS_TIMEOUT bit in STATUS1 register is set to 1. This is a latched fault. The ARC3C0845/ARC3C0845W won't start up until a reset event occurs, i.e. by toggling EN low or setting the RESET bit in the CONFIG4 register (which clears itself).

LED Short Protection

The ARC3C0845/ARC3C0845W includes a fault comparator on each LEDx pin to detect a shorted LED condition. This comparator enables when at least one LED pin is in regulation and the shorted LED fault is triggered when a LEDx voltage rises above the shorted LED voltage threshold. The shorted LED voltage threshold can be programmed to 4.35V, 4.85V, 5.25V and 5.75V by using the LED_SHORT_VTH[1:0] bits in the CONFIG3 register. This fault condition may occur when some LEDs in a string are electrically bypassed making that LED string shorter than the other LED strings.

The reduced forward voltage causes the current sink attached to that string to have a higher voltage than other current sinks, which could cause over-heating of that current sink. When this fault is detected, the faulty current sink is disabled, and an LED short fault is recorded in the STATUS1 register. The faulty current sink can only be re-enabled by turning off all LED current sinks first, or if a reset event occurs.

LED Open Circuit Protection

When one of the LED strings is open, the output will rise until it crosses the VOUT OVP threshold. Any string that is under-regulation at that moment is blocked from controlling VOUT, resulting in the output decreasing to a level needed to regulate the remaining non-open LED strings. An LED open fault is recorded in STATUS2 register.

If the open LED string is re-connected, the LED current sink will re-establish current to the level it is able based on the output voltage, but it will not be allowed to control the VOUT voltage. All LEDs need to be turned off or the part needs to be reset in order to re-enable output control for any faulted strings.

Over-current and Short Circuit Protection

The boost converter has a cycle-by-cycle over-current limit, but starts up initially with a derated over-current limit of 1.0A typically for soft-start. The cycle-by-cycle over-current limit can be programmed to 1A, 2A, 3A or 4A by using the BOOST_ILIM[1:0] bits in CONFIG1 register. The boost low-side switch turns off when the inductor current reaches the current limit threshold and remains off until the beginning of the next switching cycle. This fault is not reported in the STATUS1 or STATUS2 registers.

For more severe over-current faults where the cycle-by-cycle over-current limit cannot prevent the inductor current from continuing to ratchet up, a secondary over-current protection is implemented. When the inductor current through the boost low-side switch exceeds the secondary current limit, which is 2A above the BOOST_ILIM[1:0] settings, the converter and the LED current sinks are disabled immediately. The BST_ILIM_SEC bit in the STATUS1 register will be set and is cleared upon read. The switching converter and LED current sinks remain latched off and will not restart unless the part is shutdown or reset.

A separate short-circuit detection is implemented where if the output voltage drops suddenly forcing a large current out of the charge-pump, the output will be disconnected from the charge pump and the LED current sinks are temporarily disabled. The boost and charge pump remain switching, regulating at the last known voltage level. The DISC_OCP bit in the STATUS1 register will be set. The LED current sinks are enabled again when the fault at the VOUT pin is removed.

Current Setting

In I²C mode, the maximum current of the LED outputs is set by the MAX_I[4:0] register bits in the CONFIG2 register. The default maximum current is 43mA per LED string with 31 further settings available: 12 mA to 43 mA in 1 mA increment per step.

Fine tuning of the maximum current of the LED outputs can be set in I²C mode by the IMAXTUNE[3:0] register bits in the VREG_IMAXTUNE register. This allows incremental increases in the maximum output current from the MAX_I[4:0] setting mentioned above, in 4-bit resolution (16 steps) over a range from 0% to 7.66% with an average 0.51% per step. The Table 12 shows an example for MAX_I[4:0] bit settings with respect to ISET_EXT bit settings. Note that PSemi trims parts for current accuracy at the default MAX_I[4:0] of 30 mA. Using IMAXTUNE[3:0] to increase maximum output current from these default values will result in some loss of accuracy.

MAX_I[4:0]	FULL SCALE ILED CURRENT (ISET_EXT=0)	KISET CURRENT MULTIPLIER	MAX_I[4:0]	FULL SCALE ILED CURRENT (ISET_EXT=0)	KISET CURRENT MULTIPLIER (ISET_EXT=1)
00000	12 mA	400.00	1 0000	28 mA	933.33
00001	13 mA	433.33	1 0001	29 mA	966.66
00010	14 mA	466.67	1 0010	30 mA	999.99
00011	15 mA	500.00	1 0011	31 mA	1033.33
00100	16 mA	533.33	1 0100	32 mA	1066.66
00101	17 mA	566.67	1 0101	33 mA	1099.99
00110	18 mA	600.00	1 0110	34 mA	1133.33
00111	19 mA	633.33	1 0111	35 mA	1166.66
01000	20 mA	666.66	1 1000	36 mA	1199.99
01001	21 mA	700.00	1 1001	37 mA	1233.33
01010	22 mA	733.33	1 1010	38 mA	1266.66
01011	23 mA	766.66	1 1011	39 mA	1299.99
01100	24 mA	800.00	1 1100	40 mA	1333.32
01101	25 mA	833.33	1 1101	41 mA	1366.66
01110	26 mA	866.66	1 1110	42 mA	1399.99
01111	27 mA	900.00	1 1111	43 mA	1433.32

Table 12: Current Settings

In addition, the maximum current can be adjusted by an external resistor, RISET connected between ISET pin and ground, when the ISET_EXT bit is set to 1 in the CONFIG3 register. RISET controls the full scale LED current in conjunction with the current determined by the MAX_I register bits as follows:

$$I_{LED\_FULL} = \frac{0.4}{R_{ISET}} * K_{ISET}$$

The RISET range is between 13.3 KΩ to 133 KΩ. In PWM mode, the output current of the LED can be calculated from the duty cycle of the PWM input as follows:

$$I_{LED} = \frac{0.4}{R_{ISET}} * K_{ISET} * PWM\ Duty\ Cycle$$

In non-I²C mode, the above formula applies with KISET = 999.99 by default (KISET can be changed by re-programming MTP).

Boost Converter Switching Frequency

In I²C mode, the ARC3C0845/ARC3C0845W's boost converter provides wide frequency selection to meet different users' requirements. Five bits are used to set the boost switching frequency, which are the FSW_BOOST[4:0] bits in the CONFIG1 register. See Table 13.

In non-I²C mode, the boost switching frequency is set by the SDA pin, which is sampled once at startup. Changing the SDA pin bias after boost switching has started will not change the boost switching frequency. Table 13 shows the boost switching frequency settings through I²C register value and SDA pin in both I²C and non-I²C mode.

The choice of inductor, charge pump fly capacitors and compensation components is dependent on the selected boost switching frequency for proper part operation. Contact pSemi for recommended component types and values.

FREQ (KHZ)	FSW_BOOST[4:0]	NON-I2C	FREQ (KHZ)	FSW_BOOST[4:0]	NON-I2C
	BINARY CODE	SDA PIN		BINARY CODE	SDA PIN
3413	00010		569	10001	
2560	00011		539	10010	
2048	00100		512	10011	Tie to AGND
1707	00101		488	10100	
1463	00110		465	10101	
1280	00111		445	10110	
1138	01000	Tie to VDD	427	10111	
1024	01001		410	11000	
931	01010		394	11001	
853	01011		379	11010	
788	01100		366	11011	
731	01101	Floating	353	11100	
683	01110		341	11101	
640	01111		330	11110	
602	10000		320	11111	

Table 13: Boost Switching Frequency Settings

SDA shorted to VDD pin	1138 kHz
SDA open	731 kHz
SDA shorted to AGND pin[1]	512 kHz

1. Depended on FSW_BOOST[4:0] bits default setting.

Charge Pump Switching Frequency

Table 14 lists the default relationship between the LED brightness setting and the charge-pump frequency ratio from the boost switching frequency. The charge-pump frequency ratio and relationship to the LED brightness setting are programmable using the CP_FREQ_TRAN, SEL_CP_FREQ and CP_FREQ_DIV[1:0] bits in the CONFIG_CP register. See Table 14 for the Charge Pump frequency ratio setting at different CP_FREQ_TRAN, SEL_CP_FREQ and CP_FREQ_DIV[1:0] bit settings and LED brightness level. Detailed bit function is listed in the "Detailed Register Description" CONFIG_CP section.

CP_FREQ_TRAN	SEL_CP_FREQ	CP_FREQ_DIV[1]	CP_FREQ_DIV[0]	CP FREQUENCY RATIO
0	0	X	X	1/8 at <50% LED brightness 1/4 between ≥50% and <75% LED brightness 1/2 at ≥75% LED brightness
0	1	0	0	1/2 across entire LED brightness range
0	1	0	1	1/4 across entire LED brightness range
0	1	1	0	1/8 across entire LED brightness range
0	1	1	1	1/8 across entire LED brightness range
1	X	X	0	1/4 at <50% LED brightness 1/2 at ≥50% LED brightness
1	X	X	1	1/8 at <50% LED brightness 1/4 at ≥50% LED brightness

Table 14: Charge-Pump Frequency Ratio

Switching Converter Compensation

The switching converter operates in voltage-mode control and uses Type-III compensation which requires 3 external components:

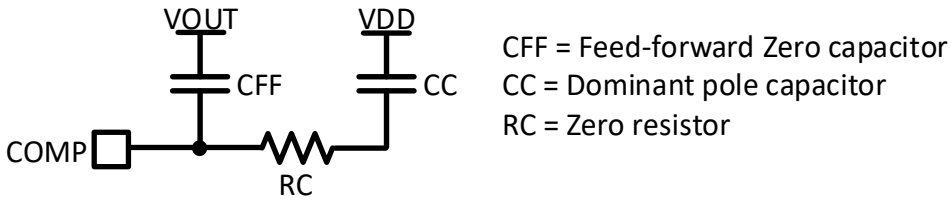


Figure 51: Compensation Components

Table 15 shows the recommended compensation component selection for different inductor values.

The SEL_VR[2:0] sets the control loop DC gain.

For a more specific set of compensation components to optimize bandwidth and phase margin for your application, please contact pSemi.

INDUCTOR VALUE	RC VALUE	CC VALUE	CFF VALUE	SEL_VR[2:0] SETTING
2.2 µH	680Ω	10 nF	220 pF	111
3.3 µH	820Ω	10 nF	220 pF	111
4.7 µH	1kΩ	10 nF	220 pF	111
6.8 µH	1.2kΩ	10 nF	220 pF	111
10 µH	1.5kΩ	10 nF	220 pF	111

Table 15: Compensation Components

LED Current Output Dimming

The ARC3C0845/ARC3C0845W supports four LED current output dimming options for maximum application flexibility in choosing among low noise, converter efficiency, optical efficiency and minimal WLED color shift at low brightness levels. These options are Analog, Phase Shift PWM, Hybrid PWM (Mixed-Mode), and Direct PWM (DPWM) dimming.

Analog Dimming

In I^2C mode, when CONFIG2 register, DIM_MODE bit is set to 0, dimming is set to Analog only. In analog dimming, the LED current sink output is always a dc current across the entire brightness range. As brightness is reduced, the LED current sink output dc level decreases which also decreases the LED forward voltage. The adaptive output voltage regulation loop decreases the VOUT voltage at the top of the LED strings, which can also reduce power dissipation in the switching converter. Operating the LEDs with a dc current output also minimizes noise in the system.

When using a non-I^2C interface, the analog dimming mode is selected by floating the SCL pin. The full-scale output current per channel can be scaled using an external resistor, R_{ISET}, connected between the ISET pin and analog ground. The tolerance of the external resistor R_{ISET} directly affects the accuracy of the LED current sink output, so using a precision resistor is recommended. The recommended R_{ISET} resistor range is 13.3kΩ to 133kΩ, with 13.3kΩ corresponding to 43 mA full-scale current output per channel with MAX_I[4:0] bits set to 11111.

Phase Shift PWM Dimming

In I^2C mode, when CONFIG2 register, DIM_MODE bit is set to 1, PWM dimming is enabled. Under this mode, the mixed dimming block generates phase shifted PWM signals to dim active LED strings when the required LED current is below the threshold set by PWM_IX[1:0] register bits. The phase difference between active strings is automatically adjusted to 360 degrees divided by the number of active strings. This phase shifting reduces noise in the audio band.

When the LED current outputs are PWM dimming, their switching frequency can be selected from one of 5 frequency settings between 2.5kHz and 40kHz using the PWM_DIM_FREQ[2:0] register bits. When using a non-I^2C interface, the PWM dimming frequency of the LED current outputs is 2.5kHz (factory default) with the SCL pin grounded. Contact PSemi for alternate frequency options or reprogram the MTP.

Hybrid PWM (Mixed-Mode) Dimming

The ARC3C0845/ARC3C0845W allows a mixed dimming output scheme for better optical efficiency. The switch point from analog to PWM dimming is set by register bits DIM_MODE=1 and PWM_IX[1:0], and can be, 12.5%, 25%, 50% or 100% of the brightness range. 100% means PWM dimming is used across the whole brightness range. In the brightness range above the switch point, analog dimming is adopted, and below the switch point, PWM dimming is adopted. With this arrangement, good optical efficiency at low brightness levels is achieved while minimizing system noise at higher brightness levels.

PWM_IX[1:0]=11 results in a dc output current only when the LED brightness setting is at 100%, otherwise the LED current sink switches off and on to 100% of its full-scale output level.

PWM_IX[1:0]=10 results in a dc output current only when the LED brightness setting is at 50% or greater, otherwise the LED current sink switches off and on to 50% of its full-scale output level.

PWM_IX[1:0]=01 results in a dc output current only when the LED brightness setting is at 25% or greater, otherwise the LED current sink switches off and on to 25% of its full-scale output level.

PWM_IX[1:0]=00 results in a dc output current only when the LED brightness setting is at 12.5% or greater, otherwise the LED current sink switches off and on to 12.5% of its full-scale output level.

An example of the LED current output for any one channel at the PWM_IX[1:0]=01 setting is shown in the Figure 52.

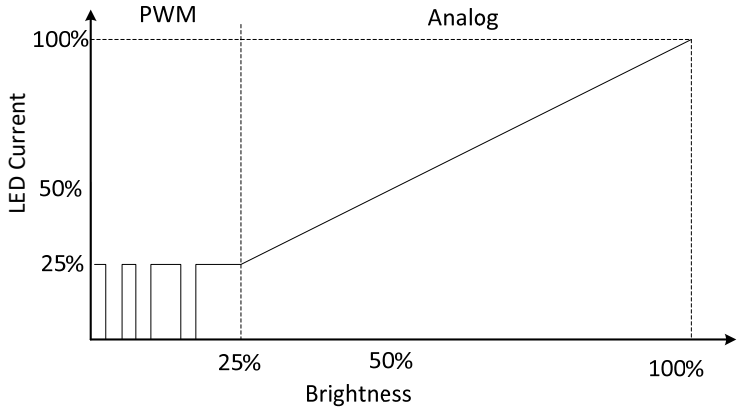


Figure 52: Mixed-Mode Dimming

The choice of four brightness transition points between analog dimming and PWM dimming at the LED current sink output provides flexibility in optimizing between good optical efficiency and good matching of the LED brightness and color shift. Since the LED current output peak during PWM dimming scales proportionally with the brightness transition point, the LED current pulse width also has to scale inversely for a given brightness setting. For example, at a 10% LED brightness setting, the LED current pulse width at PWM_IX[1:0]=01 (25% transition point) is four times longer than at PWM_IX[1:0]=11 (PWM-only dimming) to get an equivalent output brightness. The minimum controllable LED current on pulse or off pulse is 200ns typically.

In non-I^2C mode, when the SCL pin is grounded, the mixed dimming control scheme is enabled and the brightness transition point between analog dimming and PWM dimming is 25% (factory default).

In non-I²C mode, the LED output dimming options are selected by the SCL pin, which is sampled once at startup. Changing the SCL pin bias after boost switching has started will not change the LED dimming scheme. See Table 16 for the SCL pin setting to dimming scheme in non-I²C mode.

SCL PIN[1]	DIMMING SCHEME
Tied to AGND pin[2]	Mixed dimming with 25% transition point
Floating	Analog dimming
Tied to VDD pin	Direct PWM dimming
Notes: *1. Do not set DIMCODE[1:0] to 11 as default setting.* *2. Depended on DIM_MODE bit default setting.*	

Table 16: SCL Pin Setting

Direct PWM (DPWM) Dimming

The brightness is directly proportional to the duty cycle applied at the PWM pin. The LED current outputs are no longer phase-shifted but are synchronized with the timing edges at the PWM pin.

In I²C mode, when the DIMCODE[1:0] register bits are set to 11, the direct PWM dimming mode is selected. In non-I²C mode, tying the SCL pin to the VDD pin will select direct PWM dimming.

In direct PWM dimming mode, the input PWM signal switches the LED strings on and off directly, with the LED current on when PWM is high. The mixed dimming block is bypassed, and there is no phase shift among the LED strings. The minimum PWM pulse width allowed under direct PWM dimming is 200ns. The PWM input frequency range is from 200 Hz to 20 KHz in this mode.

LED Current Full-Scale or 100% Brightness

The maximum LED Current full-scale can be programmed using either I²C or an external resistor, both of which provide for fine tuning. For details please refer to Current Setting section.

LED Brightness Control

In I²C mode, the LED brightness is controlled by the duty cycle of the PWM input signal, the WLED_ISET_MSB and WLED_ISET_LSB registers written via the I²C interface, or both. The register bits DIMCODE[1:0] select 4 different brightness control options.

DIMCODE=00

When DIMCODE=00, the LED current is controlled only by the PWM input duty cycle. The PWM detector block extracts the duty cycle of the PWM input signal. The duty cycle goes through a mapping to generate a DC current level or phase-shifted PWM currents at the LED strings.

When the I²C interface is not used, LED dimming is controlled by the PWM input only, with the full scale current set by the resistor on the ISET pin.

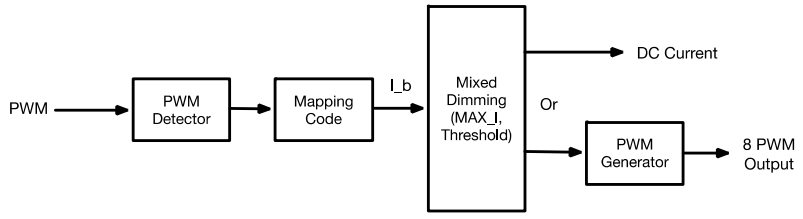


Figure 53: DIMCODE=00

DIMCODE=01

When DIMCODE=01, the LED current is controlled by the WLED_ISET_MSB and WLED_ISET_LSB registers via the I²C interface. The register codes go through a mapping first, then through the mixed dimming block to generate a DC current level or eight phase-shifted PWM currents at the LED strings. The user must first write to the WLED_ISET_LSB register and then the WLED_ISET_MSB register to update the 12-bit dimming value.

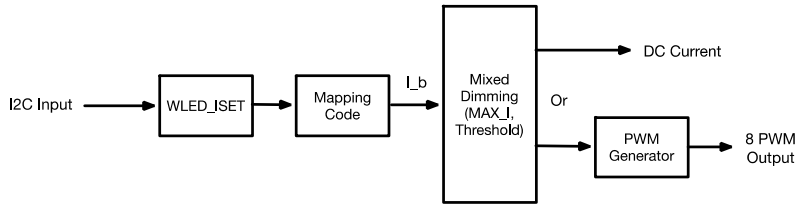


Figure 54: DIMCODE=01

DIMCODE=10

When DIMCODE=10, the LED current is controlled by both the PWM input duty cycle and the WLED_ISET_MSB and WLED_ISET_LSB register values via the I²C interface. The register codes go through a mapping first and then are multiplied by the PWM-based brightness code. After multiplication, the resulting code goes into the dimming block to generate a DC current level or eight phase-shifted PWM currents.

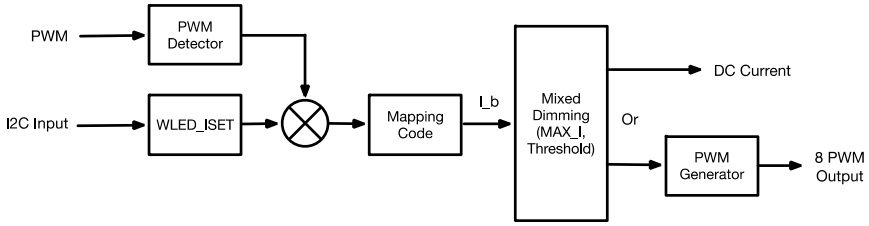


Figure 55: DIMCODE=10

DIMCODE=11

When DIMCODE=11, direct PWM dimming is enabled. Under this setting, the input PWM signal turns the active LED strings on and off directly while the internal decoding circuitry and mixed dimming block are bypassed. The minimum input PWM pulse width is limited to 200ns under direct PWM dimming. The LED current at each string switches from zero current to the full-scale current level set by MAX_I[4:0] and if used, the external ISET resistor.

Linear and Logarithmic Mapping

In linear mapping mode, the dimming settings presented either via the PWM input or WLED_ISET_MSB and WLED_ISET_LSB registers are translated linearly into the LED current. This is the factory default setting. There are 4095 possible brightness states in this mode with the dither function disabled (DITHER_ENABLE bit=0), and 32767 possible brightness states with the dither function enabled (DITHER_ENABLE bit=1).

For a better visual experience, ARC3C0845/ARC3C0845W can also translate the dimming settings via a logarithmic mapping to produce the LED current. The user can set the LOG_MODE bit to 1 in the CONFIG2 register to enable this feature. There are 1023 possible brightness states in this mode with the dither function disabled (DITHER_ENABLE bit=0), and 8191 possible brightness states with the dither function enabled (DITHER_ENABLE bit=1).

With the dither function enable, the ARC3C0845/ARC3C0845W utilizes the DITHER_LSB[2:0] bits combined with WLED_ISET_MSB[11:4] and WLED_ISET_LSB[3:0] to form a 15-bit LED output current setting, where the DITHER_LSB[2:0] bits become the lower LSBs. The user can then write to the 8 MSBs in register 0x06 first then the 7 LSBs in register 0x05 for a 15-bit resolution LED dimming adjustment.

Operation with DIMCODE=00 or 10

In these modes, the ARC3C0845/ARC3C0845W's PWM input frequency range is from 200 Hz to 40 KHz. The input frequency is independent of the PWM output frequency which is the eight phase LED current switching frequency. In I^2C mode, the PWM output frequency is set by the PWM_DIM_FREQ[2:0] register bits. In non-I^2C mode, the PWM output frequency defaults to 2.5kHz with the SCL pin grounded.

Note that since the on-chip clock is 10.24MHz, a full 12 bit PWM input resolution can obtained with a ≤2.5KHz PWM input signal ($10.24MHz/2^{12}$ = 2.5KHz). Higher PWM input frequencies will reduce PWM input resolution, with 8 bits of PWM input resolution available at 40KHz.

The same resolution limitation occurs with the PWM output frequency. This effect is most pronounced with 100% PWM dimming (PWM_IX[1:0]=11) with 8 bits of dimming resolution. When 25% PWM dimming is used, a 40KHz PWM output frequency provides 10 bits of dimming resolution relative to the full-scale LED output current.

For 12-bit brightness control, the PWM Generator uses the register 0x06 as the msb portion mapped as bits [11:4] and the upper nibble of register 0x05 as the lsb [3:0] in the 12 bit value. The LED intensity is updated at the start of every LED output PWM cycle with the frequency set by the PWM_DIM_FREQ[2:0] bits.

In general, the dimming resolution at the LED current output is related to the PWM dimming frequency and the hybrid transition point, with a higher resolution achieved with a lower PWM dimming frequency and lower transition point. For example, for a 25% transition point, a 12-bit resolution is possible at the 10kHz PWM_DIM_FREQ[2:0]=010 setting or lower, an 11-bit resolution is possible at the 20kHz PWM_DIM_FREQ[2:0]=011 setting, and so forth. This example is based on I^2C control when the PWM input frequency is ≤2.5KHz.

The ARC3C0845/ARC3C0845W provides a dithering function by increasing the dimming resolution above 12 bits. With the DITHER_ENABLE bit set to 1, the dimming resolution increases up to 15 bits by utilizing the DITHER_LSB[2:0] bits as the lower 3 LSB. These three LSB bits combine with the WLED_ISET[11:0] to provide 15-bit of dimming resolution. Figure 56 and Figure 57 show how the register bits are used.

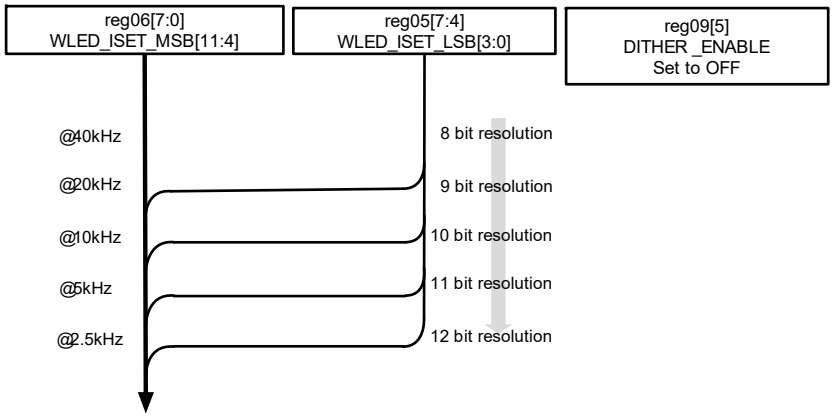


Figure 56: Relationship Between Frequency and Resolution in Phase Shift PWM Dimming with Dither "OFF"

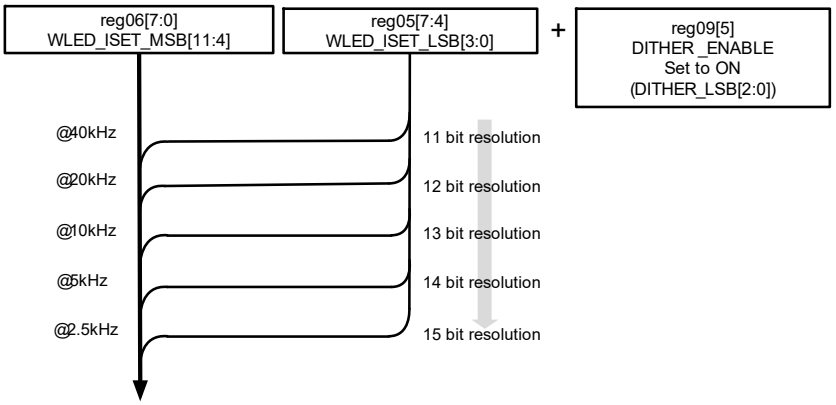


Figure 57: Relationship Between Frequency and Resolution in Phase Shift PWM Dimming with Dither "ON"

Fade In/Out Control

The Fade In/Out control makes a smooth transition from one brightness value to another for a better human eye experience. ARC3C0845/ARC3C0845W provides extensive selection of the time for brightness changes from one level to another. The fading speed is selected by the FADING_SPEED[7:0] bits in the FADING_SPEED register. This register can set the speed from 50us/step (0x01) to 12.75ms/step (0xFF) or disabled (0x00) based on user preference. See the register FADING_SPEED section for detailed description.

In non-I^2C mode, FADING_SPEED defaults to 0x00.

Digital R-C Filter for Non-DPWM Mode Brightness Change

Due to the variability in the rate of consecutive discrete input brightness changes, it is not possible to pick a single fading speed and still produce a visibly smooth output brightness change for all use cases. To resolve this issue, an RC-filter is used to filter the output brightness change response to each input brightness change.

2 bits RCFILTER[1:0] control the coefficient of this RC time constant as shown in Table 17 for a specific case of brightness changes between 1% and 99%. The RC filter coefficient is independent of the PWM_DIM_FREQ[2:0] frequency settings. The RCFILTER[1:0] bits are available in I^2C mode through the FILTER_SETTINGS register.

RCFILTER[1:0]	RC TIME CONSTANT (T)
00	Disabled
01	417 ms
10	207 ms
11	103 ms

Table 17: RC Filter Settings

Input PWM Filter for Non-DPWM Mode

When a duty cycle is applied at the PWM pin to control brightness in non-DPWM mode, the on-time and period are sampled by the internal 10.24MHz master clock to translate time-domain information into binary values. As inherent with any sampling of an asynchronous signal, the sampled binary values can jitter by +/-1 LSB at steady-state, which translates into jitter on the final brightness result and this can be visible as flicker. Adding some basic filtering to this sampled system can help eliminate this flicker at steady-state.

PWMFILTER[2:0] register bits in FILTER_SETTING register enable/disable this filter as well as control the amount of filtering. Furthermore, the filtering is dependent on the direction of the sampled PWM time-step as follows: if the PWM time-step has been decreasing, the sampled binary value is allowed to decrement regardless of the delta time-step size but prevented from

incrementing unless the delta time-step size is greater than or equal to the programmed filter threshold. Conversely if the PWM time-step has been increasing, the sampled binary value is allowed to increment regardless of the delta time-step size but prevented from decrementing unless the delta time-step size is greater than or equal to the programmed filter threshold.

PWMFILTER[2:0]	MINIMUM PWM TIME-STEP SIZE
000	OFF
001	2 steps
010	4 steps
011	6 steps
100	8 steps
101	10 steps
110	12 steps
111	14 steps

Table 18: PWM Filter Settings

I²C Interface Bus Overview

The I²C bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to I²C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The ARC3C0845/ARC3C0845W operates as a slave and supports the following data transfer modes, as defined in the I²C-Bus specification: Standard mode (100 Kbps), fast mode (400 Kbps), and fast mode plus (1 Mbps). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as VIN voltage remains above UVLO and the EN pin remain asserted.

The data transfer protocol for standard and fast modes is exactly the same, therefore they are referred to as F/S-mode in this document. The ARC3C0845/ARC3C0845W supports 7-bit addressing; 10-bit addressing and general call address are not supported. The device 7-bit address is defined as ‘0110XXX‘.

Programming I²C Slave Address - Multiple Parts on One I²C Bus

To enable multiple ARC3C0845/ARC3C0845W parts to be addressed on one I²C bus, the lower 3 bits of the I²C slave address are programmable by using the ADDR pin. The ADDR pin configuration to the device 7-bit address is shown in Table 19.

ADDR PIN	DEVICE 7 BIT ADDRESS
Tied to AGND	0110000 (0x30)
Floating	0110010 (0x32)
Tied to VDD	0110101 (0x35)

Table 19: ADDR Pin Configuration

Standard-, Fast-, Fast-Mode Plus Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 58. All I²C-compatible devices should recognize a start condition.

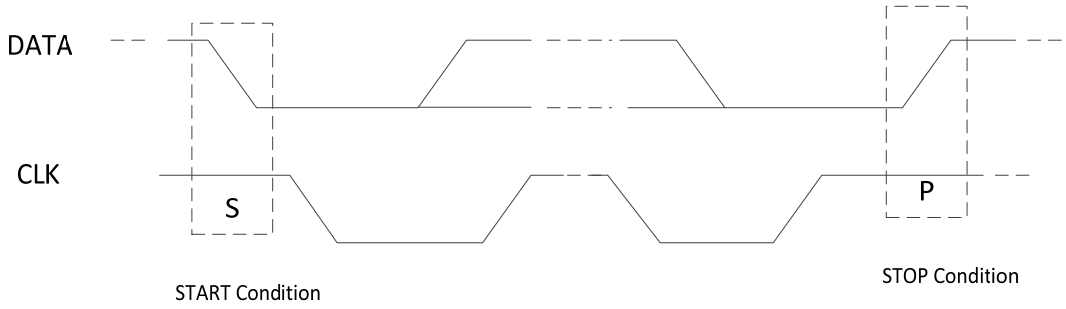


Figure 58: START and STOP Conditions

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit $R/\overline{W}$ on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 59). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 60) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that a communication link with a slave has been established.

The master generates further SCL cycles to either transmit data to the slave ($R/\overline{W}$ bit 0) or receive data from the slave ($R/\overline{W}$ bit 1). In either case, the receiver needs to acknowledge the data sent by transmitter. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 58). This releases the bus and stops the communication link with the addressed slave. All I²C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.

Attempting to read data from register addresses not listed in this section will result in FFh being read out.

ARC3C0845/ARC3C0845W I²C Update Sequence

The ARC3C0845/ARC3C0845W requires a start condition, a valid I²C address, a register address byte, and a data byte for a single update. After the receipt of each byte, ARC3C0845/ARC3C0845W device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the ARC3C0845/ARC3C0845W. The ARC3C0845/ARC3C0845W performs an update on the falling edge of the acknowledge signal that follows the LSB.

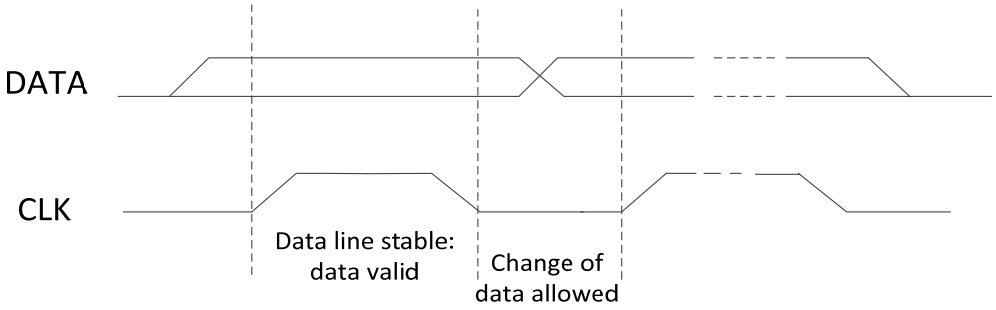


Figure 59: Bit Transfer on the Serial Interface

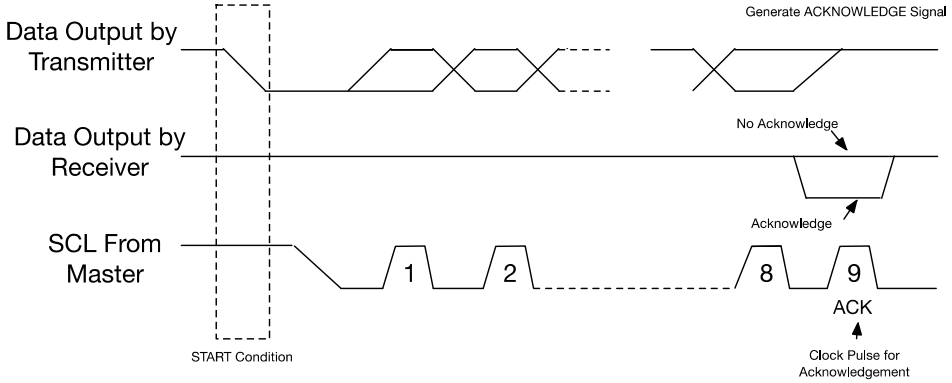


Figure 60: Acknowledge on the I²C Bus

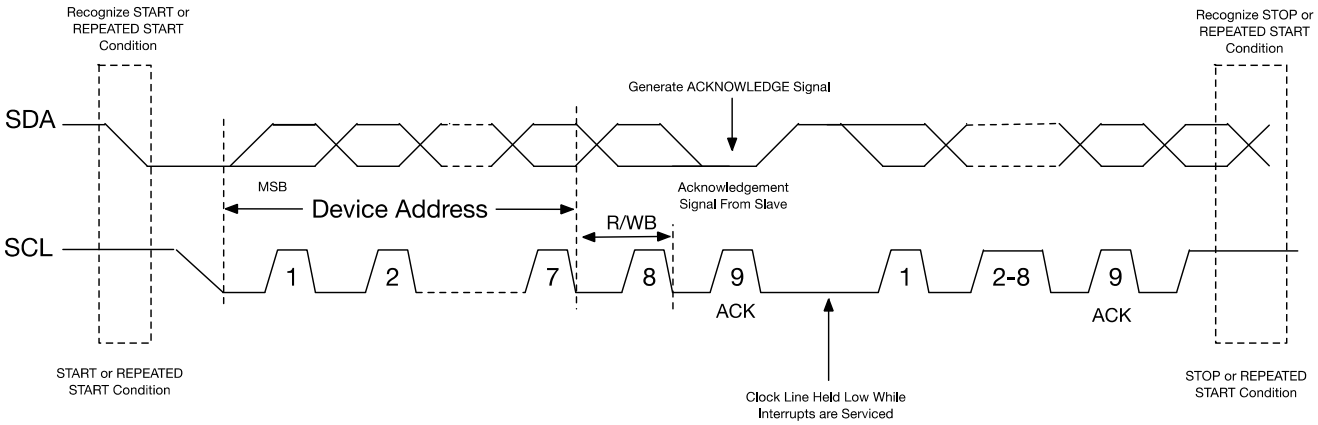


Figure 61: Bus Protocol

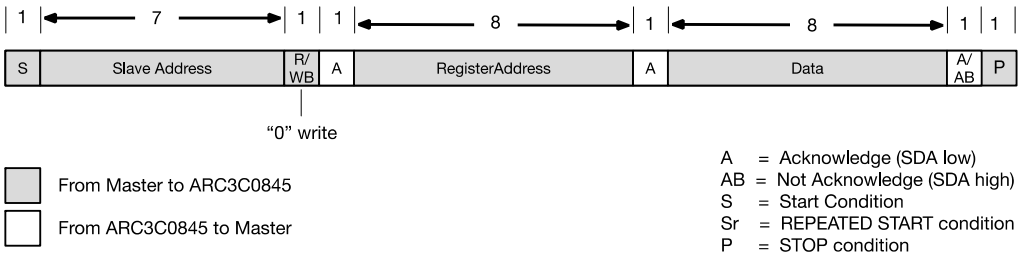


Figure 62: "Write" Data Transfer Format in Standard, Fast, Fast-Plus Modes

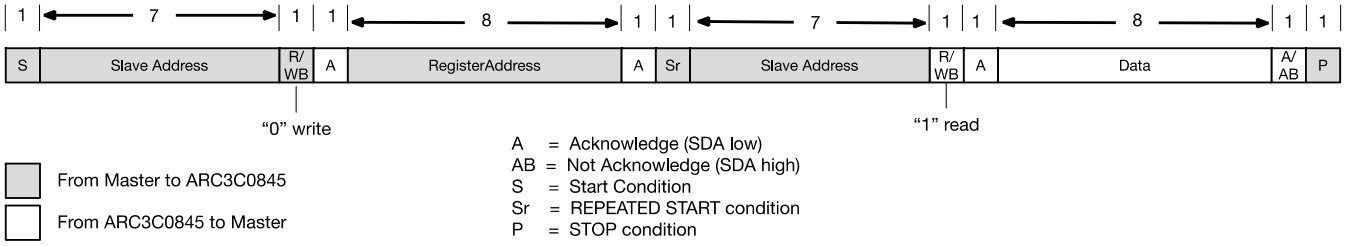


Figure 63: "Read" Data Transfer Format in Standard-, Fast, Fast-Plus Modes

ARC3C0845/ARC3C0845W MTP Non-volatile Memory Description

The ARC3C0845/ARC3C0845W contains non-volatile memory (NVM) to store the default values for registers 0x00 to 0x0B. The data in the NVM is recalled to the registers at the device POR event. This function saves system initialization time by allowing user to program the device default setting in the production line instead of programming these settings every time after POR event. To perform the MTP programming cycle, first write the desired values for registers 0x00 to 0x0B. Then set the MTP_WRITE_CMD[4:0] bits to 10010 to initialize the MTP programming. During the MTP programming cycle, the MTP_WRITE_CMD[4:0] bits remain at 10010 and MTP_WRITE_DNE bit is at 0. When the MTP programming cycle completes, the MTP_WRITE_CMD[4:0] bits automatically reset back to 00000 and MTP_WRITE_DNE bit is set to 1. The MTP programming cycle takes 50ms maximum to complete. During the MTP programming cycle, do not write to registers 0x00 to 0x0B to avoid data corruption.

Register Map

Slave Address: 0110000 (0x30)[1]

Register Configuration Parameters

REGISTER	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
COMMAND	0x00	SEL_VR [2:0]			BOOST_MODE	OVP_TH [3:0]			
CONFIG1	0x01	(Reserved)	BOOST_ILIM [1:0]		FSW_BOOST [4:0]				
FADING_SPEED	0x02	FADING_SPEED [7:0]							
CONFIG2	0x03	(Reserved)	LOG_ MODE	DIM_MODE	MAX_I [4:0]				
LEDEN	0x04	LEDEN_8	LEDEN_7	LEDEN_6	LEDEN_5	LEDEN_4	LEDEN_3	LEDEN_2	LEDEN_1
WLED_ISET_LSB	0x05	WLED_ISET_LSB [3:0]				DITHER_LSB[2:0]			(Reserved)
WLED_ISET_MSB	0x06	WLED_ISET_MSB [11:4]							
CONFIG3	0x07	ISET_EXT	LED_SHORT_VTH [1:0]		PWM_IX [1:0]		PWM_DIM_FREQ [2:0]		
CONFIG4	0x08	I2C_ STANDBY	RESET	(Reserved)					
FILTER_SETTINGS	0x09	DIMCODE [1:0]		DITHER_ ENABLE	RCFILTER [1:0]		PWMFILTER [2:0]		
VREG_IMAXTUNE	0x0A	LED_VREG_CNT_INIT [3:0]				IMAXTUNE [3:0]			
CONFIG_CP	0x0B	AUTO_CP_RATIO	SEL_CP_ RATIO	(Reserved)	(Reserved)	CP_FREQ_ TRAN	SEL_CP_ FREQ	CP_FREQ_DIV [1:0]	
CHKSUM0	0x0C	CHKSUM0 [7:0]							
CHKSUM1	0x0D	CHKSUM1[7:0]							
STATUS1	0x0E	BST_ILIM_SEC	VOUT_ OVP	VX_OV	VX_UV	DISC_OCP	TSD	SS_ TIMEOUT	LED_SHORT
STATUS2	0x0F	MTP_WRITE_CMD [4:0]					MTP_WRITE_DNE	CRC_OK	LED_OPEN

Note:

1. *ADDR pin tied to GND. Excluding read/write bit. 01100000 (0x60) if including read/write bit.)*

Detailed Register Description

Register COMMAND

ADDRESS	NAME	POR VALUE(1)
0x00	COMMAND	0xE0

Bit Assignment

7	6	5	4	3	2	1	0
SEL_VR [2:0]			BOOST_MODE	OVP_TH [3:0]			

Bit Description

FIELD NAME	BITS	TYPE	POR (1)	DESCRIPTION
SEL_VR [2:0]	[7:5]	R/$\overline{w}$	111	3-bit selection of Control Loop DC Gain: From Highest (000) to Lowest (111) in 2dB increment. Please refer to Switching Converter Compensation for recommended setting
BOOST_MODE	[4]	R/$\overline{w}$	0	0 = DCM fixed-frequency boost switching (no negative inductor current) 1 = Forced CCM fixed-frequency boost switching (negative inductor current allowed)
OVP_TH [3:0]	[3:0]	R/$\overline{w}$	0000	4-bit selection of VOUT OVP thresholds: From 47.5V (0000) to 19.375V (1111) in 1.875V decrements per step

Note:

1. *The POR value listed for each register is the factory programmed default value. These POR values maybe no longer valid after performing MTP programming.*

Register CONFIG1

ADDRESS	NAME	POR VALUE(1)
0x01	CONFIG1	0x53

Bit Assignment

7	6	5	4	3	2	1	0
Reserved	BOOST_ILIM [1:0]		FSW_BOOST[4:0]				

Bit Description

FIELD NAME	BITS	TYPE	POR (1)	DESCRIPTION
Reserved	[7]	R/w	0	
BOOST_ILIM [1:0]	[6:5]	R/w	10	Boost cycle-by-cycle ILIM threshold 00 = 2.0A 01 = 1.0A 10 = 3.0A (default) 11 = 4.0A
FSW_BOOST[4:0]	[4:0]	R/w	10011	Boost switching frequency. See Boost Converter Switching Frequency section for full frequency chart. <=02h = 3.41MHz 04h = 2.048MHz 09h = 1.024MHz 13h = 512kHz (default)

Note:

1. *The POR value listed for each register is the factory programmed default value. These POR values maybe no longer valid after performing MTP programming.*

Register FADING_SPEED

ADDRESS	NAME	POR VALUE(1)
0x02	FADING_SPEED	0x00

Bit Assignment

7	6	5	4	3	2	1	0
FADING_SPEED [7:0]							

Bit Description

FIELD NAME	BITS	TYPE	POR (1)	DESCRIPTION
FADING_ SPEED	[8]	R/$\overline{W}$	00000000	Sets the fading counter from 50us to 12.75ms in 50us steps. This is the period between each intensity step. 0x00 = No Fading 0x01 = 50us per step 0xFF = 12.75ms per step
Note: *1. The POR value listed for each register is the factory programmed default value. These POR values maybe no longer valid after performing MTP programming.*				

Register CONFIG2

ADDRESS	NAME	POR VALUE(1)
0x03	CONFIG2	0x32

Bit Assignment

7	6	5	4	3	2	1	0
Reserved	LOG_MODE	DIM_MODE	MAX_I [4:0]				

Bit Description

FIELD NAME	BITS	TYPE	POR (1)	DESCRIPTION
LOG_MODE	[6]	R/$\overline{w}$	0	Dimming mode selector 0 = Linear Mode (default) 1 = Logarithmic mode (log table uses 1023 codes with Dither function disable, up to 8191 codes with Dither function enable)
DIM_MODE	[5]	R/$\overline{w}$	1	Dimming mode selector 0 = Analog Dimming only 1 = Mixed-mode dimming (default)
MAX_I [4:0]	[4:0]	R/$\overline{w}$	10010	Program maximum current per string in 1mA steps: 00000 = 12mA 00001 = 13mA 00010 = 14mA 10010 = 30mA (Default) 11111 = 43mA

Note:

1. *The POR value listed for each register is the factory programmed default value. These POR values maybe no longer valid after performing MTP programming.*

Register LEDEN

ADDRESS	NAME	POR VALUE(1)
0x04	LEDEN	0x00

Bit Assignment

7	6	5	4	3	2	1	0
LEDEN_8	LEDEN_7	LEDEN_6	LEDEN_5	LEDEN_4	LEDEN_3	LEDEN_2	LEDEN_1

Bit Description

FIELD NAME	BITS	TYPE	POR (1)	DESCRIPTION
LEDEN_8,…, LEDEN_1	[7:0]	R/$\overline{W}$	0	LED string enabled 0 = string is disabled 1 = string is enabled
Note: *1. The POR value listed for each register is the factory programmed default value. These POR values maybe no longer valid after performing MTP programming.*				

Register WLED_ISET_LSB

ADDRESS	NAME	POR VALUE(1)
0x05	WLED_ISET_LSB	0x00

Bit Assignment

7	6	5	4	3	2	1	0
WLED_ISET[3:0]				DITHER_LSB[2:0]			Reserved

Bit Description

FIELD NAME	BITS	TYPE	POR (1)	DESCRIPTION
WLED_ISET[3:0]	[7:4]	R/$\overline{w}$	0000	LED output current setting Bits 3-0. For details please refer to the WLED section. If changing the LSB bits, these must be written before the MSB bits. Changes to these bits are only implemented when the next register is written, which is typically the MSBs but could be any register.
DITHER_LSB	[3:1]	R/$\overline{w}$	000	With DITHER_ENABLE=1, these three bits combine with WLED_ISET[11:0] as the lower LSBs to form a 15-bits ILED dimming control. Write to these bits along with WLED_ISET[11:0] for 15-bit dimming adjustment.
Reserved	[0]			

Note:

1. *The POR value listed for each register is the factory programmed default value. These POR values maybe no longer valid after performing MTP programming.*

Register WLED_ISET_MSB

ADDRESS	NAME	POR VALUE(1)
0x06	WLED_ISET_MSB	0x00

Bit Assignment

7	6	5	4	3	2	1	0
WLED_ISET[11:4]							

Bit Description

FIELD NAME	BITS	TYPE	POR (1)	DESCRIPTION
WLED_ISET[11:4]	[7:0]	R/$\overline{W}$	00000000	The MSB bits of the WLED_ISET[11:0] brightness code. For details please refer to the WLED section.

Note:
1. The POR value listed for each register is the factory programmed default value. These POR values maybe no longer valid after performing MTP programming.

Register CONFIG3

ADDRESS	NAME	POR VALUE(1)
0x07	CONFIG3	0x08

Bit Assignment

7	6	5	4	3	2	1	0
ISET_EXT	LED_SHORT_VTH [1:0]		PWM_IX [1:0]		PWM_DIM_FREQ[2:0]		

Bit Description

FIELD NAME	BITS	TYPE	POR (1)	DESCRIPTION
ISET_EXT	[7]	R/$\overline{w}$	0	0 = LED full-scale current set by MAX_I[4:0] (default) 1 = LED full-scale current set by ISET external resistor and MAX_I[4:0]
LED_SHORT_VTH [1:0]	[6:5]	R/$\overline{w}$	00	LED short detect threshold: 00 = 4.35V (default) 01 = 4.85V 10 = 5.25V 11 = 5.75V
PWM_IX [1:0]	[4:3]	R/$\overline{w}$	01	PWM_IX[1:0] transition point between analog dimming and PWM dimming during mode change: 00 = 12.5% 01 = 25% (default) 10 = 50% 11 = 100% (also 100% PWM dimming)
PWM_DIM_FREQ	[2:0]	R/$\overline{w}$	000	PWM_DIM_FREQ (KHz) 000 = 2.5kHz (default) 001 = 5kHz 010 = 10kHz 011 = 20kHz 100 = 40kHz 101, …, 111= reserved

Note:

1. *The POR value listed for each register is the factory programmed default value. These POR values maybe no longer valid after performing MTP programming.*

Register CONFIG4

ADDRESS	NAME	POR VALUE(1)
0x08	CONFIG4	0x00

Bit Assignment

7	6	5	4	3	2	1	0
I2C_STANDBY	RESET	Reserved					

Bit Description

FIELD NAME	BITS	TYPE	POR (1)	DESCRIPTION
I2C_STANDBY	[7]	R/$\overline{W}$	0	Quasi-low current mode with references and digital blocks disabled, but register contents retained (MTP not re-loaded) 0 = Not in standby 1 = Standby mode
RESET	[6]	R/$\overline{W}$	0	Power on reset bit – clears all register contents and MTP will be re-loaded
RESERVED	[5.0]			

Note:

1. *The POR value listed for each register is the factory programmed default value. These POR values maybe no longer valid after performing MTP programming.*

Register FILTER_SETTINGS

ADDRESS	NAME	POR VALUE(1)
0x09	FILTER_SETTINGS	0x24

Bit Assignment

7	6	5	4	3	2	1	0
DIMCODE[1:0]		DITHER_ENABLE	RCFILTER[1:0]		PWMFILTER[2:0]		

Bit Description

FIELD NAME	BITS	TYPE	POR (1)	DESCRIPTION
DIMCODE[1:0]	[7:6]	R/$\overline{w}$	00	Brightness control method: 00 = PWM control only (default) 01 = I2C control only 10 = Input PWM x I2C control 11 = DPWM mode
DITHER_ENABLE	[5]	R/$\overline{w}$	1	0 = Dithering disabled 1 = Enable dithering for up to 15-bit effective resolution for linear dimming mode, up to 13-bit effective resolution for logarithmic dimming mode.
RCFILTER[1:0]	[4:3]	R/$\overline{w}$	00	RC Filter Time Constant (τ) 00 = RC filter OFF (default) 01 = 417ms 10 = 207ms 11 = 103ms
PWMFILTER[2:0]	[2:0]	R/$\overline{w}$	100	Enables/disables the PWM filter and sets step size: 000 = Off 001 = 2 Steps 010 = 4 Steps 011 = 6 Steps 100 = 8 Steps (Default) 101 = 10 Steps 110 = 12 Steps 111 = 14 Steps

Note:

1. *The POR value listed for each register is the factory programmed default value. These POR values maybe no longer valid after performing MTP programming.*

Register VREG_IMAXTUNE

ADDRESS	NAME	POR VALUE(1)
0x0A	VREG_IMAXTUNE	0x70

Bit Assignment

7	6	5	4	3	2	1	0
LED_VREG_CNT_INIT[3:0]				IMAXTUNE[3:0]			

Bit Description

FIELD NAME	BITS	TYPE	POR (1)	DESCRIPTION
LED_VREG_CNT_INIT[3:0]	[7:4]	R/$\overline{W}$	0111	Initial starting target voltage, 2.27V increments per step: 0000 = 13.75V 0001 = 16.02V 0010 = 18.28V …. 0111 = 29.61V (default) 1000 = 31.88 …. 1110 = 45.47V 1111 = 47.73V
IMAXTUNE[3:0]	[3:0]	R/$\overline{W}$	0000	Sets percentage increase of LED full-scale current in approximately 0.51% increments starting from code 1h: 0000 = 0.00% increase 0001 = 0.47% increase …. 1101 = 7.12% increase 1111 = 7.66% increase

Note:

1. *The POR value listed for each register is the factory programmed default value. These POR values maybe no longer valid after performing MTP programming.*

Register CONFIG_CP

ADDRESS	NAME	POR VALUE(1)
0x0B	CONFIG_CP	0x00

Bit Assignment

7	6	5	4	3	2	1	0
AUTO_CP_RATIO	SEL_CP_RATIO	(Reserved)		CP_FREQ_TRAN	SEL_CP_FREQ	CP_FREQ_DIV[1:0]	

Bit Description

FIELD NAME	BITS	TYPE	POR (1)	DESCRIPTION
AUTO_CP_RATIO	[7]	R/$\overline{w}$	0	Sets the charge pump ratio: 0 = Device automatically selects 2x or 3x charge pump ratio based operating condition 1 = Charge pump ratio is fixed by the SEL_CP_RATIO bit
SEL_CP_RATIO	[6]	R/$\overline{w}$	0	Active only if AUTO_CP_RATIO=1: 0 = Device operates in 2x charge pump ratio only 1 = Device operates in 3x charge pump ratio only
Reserved	[5:4]	R/$\overline{w}$	00	
CP_FREQ_TRAN	[3]	R/$\overline{w}$	0	0 = Charge pump frequency changes at 75% and 50% LED brightness automatically 1 = Charge pump frequency changes at 50% LED brightness only, and as a function of CP_FREQ_DIV[0]
SEL_CP_FREQ	[2]	R/$\overline{w}$	0	When CP_FREQ_TRAN=0: 0 = Charge pump frequency changes at 75% and 50% LED brightness automatically 1 = Charge pump frequency is independent of LED brightness and selected by CP_FREQ_DIV[0] When CP_FREQ_TRAN=1: SEL_CP_FREQ bit is don't care
CP_FREQ_DIV[1:0]	[1:0]	R/$\overline{w}$	00	When CP_FREQ_TRAN=0, SEL_CP_FREQ=1: 00 = 1/2 01 = 1/4 10 = 1/8 11 = 1/8 When CP_FREQ_TRAN=1: CP_FREQ_DIV[0] = 0 then charge pump frequency changes between 1/2 (≥50% LED brightness) and 1/4 (<50% LED brightness) CP_FREQ_DIV[0] = 1 then charge pump frequency changes between 1/4 (≥50% LED brightness) and 1/8 (<50% LED brightness)

Note:

1. *The POR value listed for each register is the factory programmed default value. These POR values maybe no longer valid after performing MTP programming.*

Register CHKSUM0

ADDRESS	NAME
0X0C	CHKSUM0

Bit Assignment

7	6	5	4	3	2	1	0
CHKSUM0[7:0]							

Bit Description

FIELD NAME	BITS	TYPE	DESCRIPTION
CHKSUM0[7:0]	[7:0]	R	Lower 8-bit of the 16-bit register checksum for registers 0x00 to 0x0B. If incorrect, the MTP values are still loaded as long as the internal factory checksum is correct. After each MTP write, the CHKSUM0 register value is updated after toggling EN pin or cycling VIN.

Register CHKSUM1

ADDRESS	NAME
0x0D	CHKSUM1

Bit Assignment

7	6	5	4	3	2	1	0
CHKSUM1[7:0]							

Bit Description

FIELD NAME	BITS	TYPE	DESCRIPTION
CHKSUM1[7:0]	[7:0]	R	Upper 8-bit of the 16-bit register checksum for registers 0x00 to 0x0B. If incorrect, the MTP values are still loaded as long as the internal factory checksum is correct. After each MTP write, the CHKSUM1 register value is updated after toggling EN pin or cycling VIN.

Register STATUS1

ADDRESS	NAME	POR VALUE
0x0E	STATUS1	0x00

Bit Assignment

7	6	5	4	3	2	1	0
BST_ILIM_SEC	VOUT_OVP	VX_OV	VX_UV	DISC_OCP	TSD	SS_TIMEOUT	LED_SHORT

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
BST_ILIM_SEC	[7]	R	0	Status bit to flag a secondary current limit: 0 = No error 1 = Boost current exceeded secondary current limit
VOUT_OVP	[6]	R	0	Status bit to flag an output overvoltage condition: 0 = No error 1 = Output overvoltage
VX_OV	[5]	R	0	Status bit to flag a VX over-voltage condition: 0 = No error 1 = VX voltage is above over-voltage threshold
VX_UV	[4]	R	0	Status bit to flag a VX under-voltage condition: 0 = No error 1 = VX voltage is below under-voltage threshold
DISC_OCP	[3]	R	0	Status bit to flag a disconnect switch over-current event: 0 = No error 1 = Disconnect switch exceeded over-current threshold, or VOUT is shorted to ground
TSD	[2]	R	0	Status bit to flag a thermal shutdown condition: 0 = No error 1 = Part has exceeded thermal shutdown threshold
SS_TIMEOUT	[1]	R	0	Status bit to flag a soft start timeout condition: 0 = No error 1 = Soft start has not completed before the timeout event
LED_SHORT	[0]	R	0	Status bit to flag an LED shorted-string fault: 0 = No error 1 = An LED shorted-string event occurred on one or more enabled strings

Register STATUS2

ADDRESS	NAME	POR VALUE
0x0F	STATUS2	0x00

Bit Assignment

7	6	5	4	3	2	1	0
MTP_WRITE_CMD[4:0]					MTP_WRITE_DNE	CRCOK	LED_OPEN

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
MTP_WRITE_CMD[4:0]	[7:3]	R/$\overline{W}$	00000	Writing 10010 to this register bits automatically initiates an MTP programming cycle to register 0x00 to 0x0B. At the end of programming, this register is automatically cleared and MTP_WRITE_DNE read-only status bit will show '1'
MTP_WRITE_DNE	[2]	R	0	Status bit indicating the completion of MTP programming for registers 0x00 to 0x0B. Clears upon read.
CRCOK	[1]	R	0	Status bit indicating the CHECKSUM for registers 0x00 to 0x0B is good
LED_OPEN	[0]	R	0	Status bit to flag an open or grounded condition on any LED pin. 0 = No error 1 = One or more LED strings is grounded open

Application Schematic

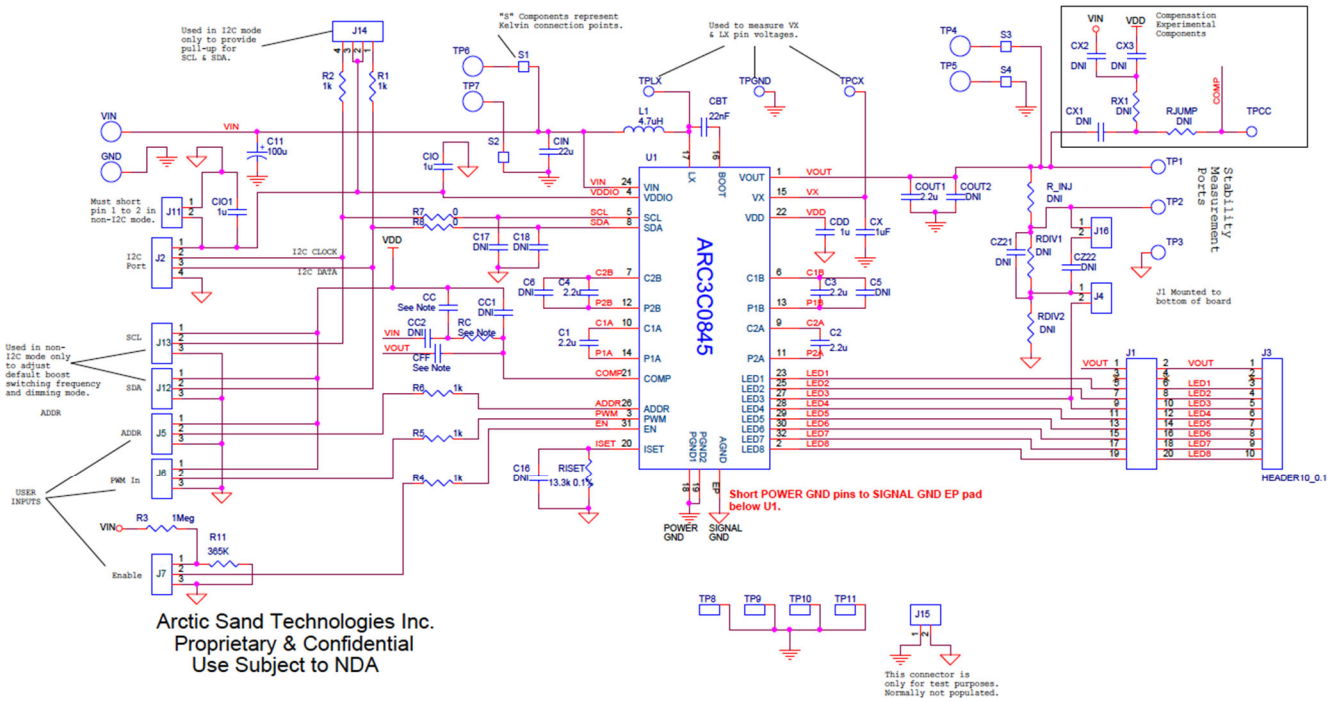


Figure 64: Detailed Application Schematic

Note: Contact factory for details of compensation

Application Circuit Part List [1]

COMPONENT	VALUE	PART SIZE	MANUFACTURER'S PART NUMBER
CBT	22 nF 50V X7R	0402	GRM155R71H223KA12D
CX	1 µF 35V X5R	0402	GRM155R6YA105KE11
C3, C4	2.2 µF 50V X5R	1206	GJ8319R61H225KA12
C1, C2	2.2 µF 25V X5R	0805	C2012X5R1E225K085AC
CIN [2]	1.0 µF 16V X5R	0603	GRM188R61C105KA12D
CC [3]		0201	
CFF [3]		0201	
COUT	2.2 µF 50V X5R	1206	GJ8319R61H225KA12
CDD, CIO	1 µF 10V X5R	0402	GRM155R61A105KE15D
L1 [4]	4.7 µH	3.2mmx2.5mmx1.2mm	DFE322512F-4R7M
RISET	13.3kΩ	0402	Use tighter than 1% tolerance
RC [3]		0201	

Notes:

1. *Components in this part list are optimized for 8P12S or higher applications. Contact PSemi for optimized selection based on your application.*
2. *Value may need to be adjusted based on proximity of the input source to eliminate input voltage ringing.*
3. *Please see Switching Converter Compensation section for general selection. Contact PSemi for optimized selection based on your application.*
4. *See also recommended inductor values below for varying operating conditions.*

Table 20: Application Circuit Part List(1)

Component Selection

Users of the ARC3C0845/ARC3C0845W should adhere closely to the parts selected for the Application Circuit Part List. Component selection is a complex process and several of the parameters of importance to the design are not typically specified for passive components. Users wishing to deviate from these components are urged to contact pSemi for guidance.

Efficiency Optimization

The ARC3C0845/ARC3C0845W is designed specifically to address 2-cell and 3-cell Narrow Voltage DC (NVDC) platforms, and for a wide range of LED configurations. The two-stage architecture relies less on the inductor for power and voltage conversion; therefore, reduction in the physical size of the inductor has less impact on the overall conversion efficiency compared with traditional single stage architectures. This enables the use of low profile, small footprint and low cost chip inductors versus wire-wound inductors used by traditional LED boost drivers.

Table 21 lists inductors optimized for platforms with an input voltage that is either 2-cell NVDC only; 3-cell NVDC only; or 2-cell NVDC AND 3-cell NVDC. The latter solution trades off a small amount of efficiency in exchange for a single bill-of-materials for platforms where cell count may vary. Refer to the typical performance data formeasured efficiency using for these different inductor and LED configurations for max ILED=30mA.

LED CONFIGURATION	2-CELL ONLY	3-CELL ONLY	2 CELL + 3-CELL
8P12S	2.2 µH	6.8 µH	3.3 µH
8P11S	2.2 µH	6.8 µH	3.3 µH
8P10S	2.2 µH	6.8 µH	3.3 µH
6P12S	2.2 µH, 4.7 µH	6.8 µH	3.3 µH
6P11S	2.2 µH, 4.7 µH	6.8 µH, 10 µH	3.3 µH
6P10S	4.7 µH	6.8 µH, 10 µH	3.3 µH
4P12S	4.7 µH	6.8 µH, 10 µH	3.3 µH

Table 21: Inductors Optimized for Platforms

Capacitors Selection

Due to component availability, size, second source requirement or other reasons causing the Application Circuit Part List cannot be followed, then use the following guideline to select appropriate capacitors for ARC3C0845.

Charge Pump Capacitors

The effective capacitance of the capacitors used for C1A, C2A, C1B and C2B should have a minimum value of 0.7µF and the ideal value is 1µF. The effective capacitance should match closely between charge pump capacitors; therefore, the same capacitor cannot be used for both the first and second charge pump stages. For example, with VOUT at 45V, 15V is applied across the first stage charge pump capacitors (C1A/C2A), and 30V is applied across the second stage charge pump capacitors (C1B/C2B). Following the Application Circuit Part List, the C2012X5R1E225K085AC capacitor selected for C1A/C2A has 1 µF effective capacitance at 15V and the GJ8319R61H225KA12 capacitor selected for C1B/C2B has 1.05 µF at 30V, which matches closely with the C1A/C2A capacitor. If the same GJ8319R61H225KA12 is used for C1A/C2A, then the effective capacitance at 15V would be 1.8 µF, which is much higher than 1.05 µF. This wide capacitance difference can lower efficiency.

If a single capacitor cannot meet the effective capacitor requirement, then two or more capacitors could parallel together to meet the effective capacitor requirement.

VX Capacitor

The VX boost convertor output capacitor should have an effective capacitance between 0.1 µF and 0.2 µF. VX voltage can easily be calculated. In 3x CP ratio, the VX is approximately VOUT/3. In 2x CP ratio, the VX is approximately VOUT/2.

VDD Capacitor

The VDD internal LDO capacitor should have a minimum effective capacitance of 0.5 µF. VDD pin typical output voltage is 4.4V with maximum output at 5V.

VOUT Capacitor

The VOUT LED output voltage capacitor should have a typical effective capacitance of 1 µF.

Layout Example

Figure 65 is an example of a compact 8 WLED string converter layout. Solution size is 95mm^2.

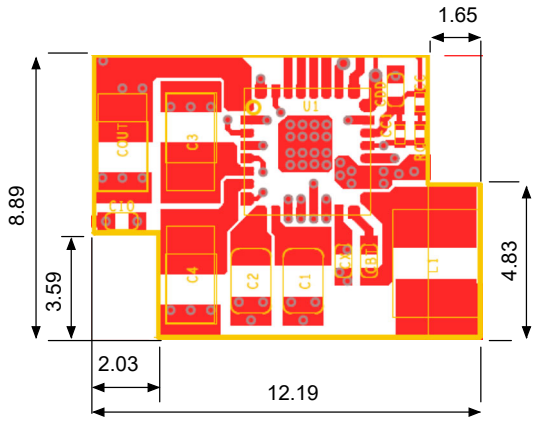


Figure 65: Layout Example

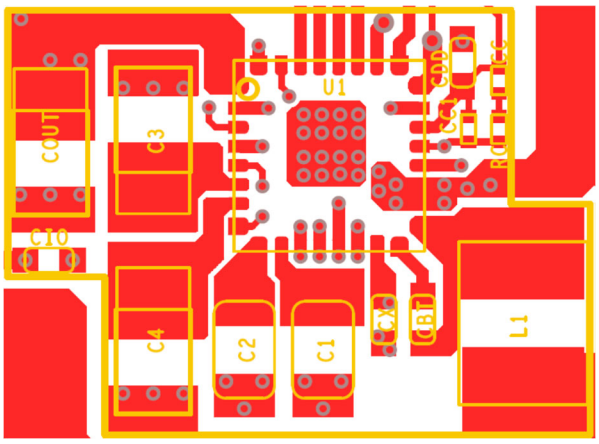


Figure 66: Top Layer

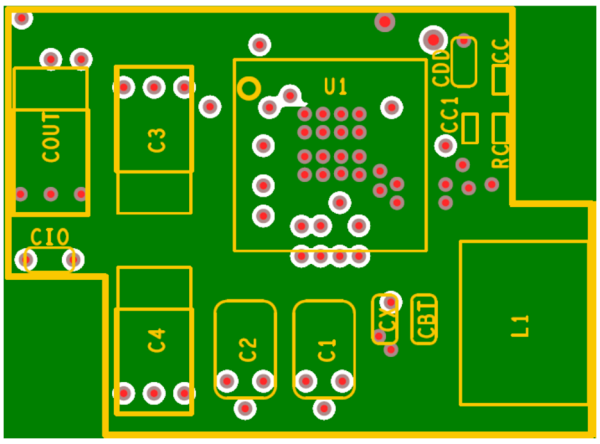


Figure 67: Layer 2

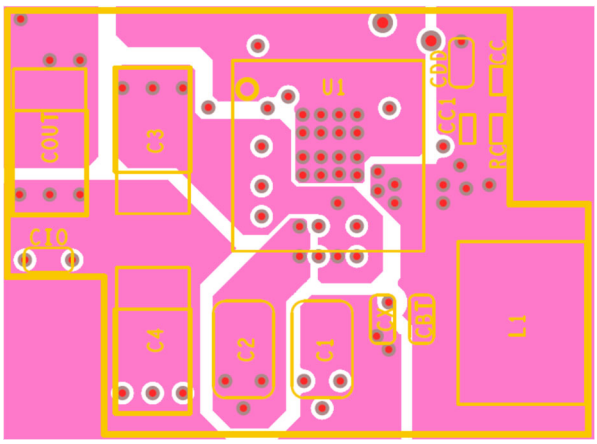


Figure 68: Layer 3

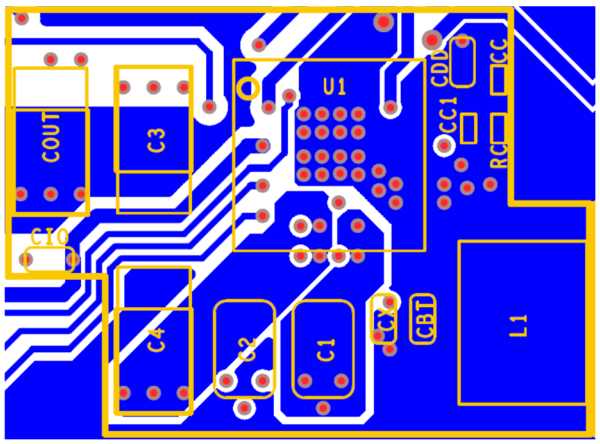


Figure 69: Bottom Layer

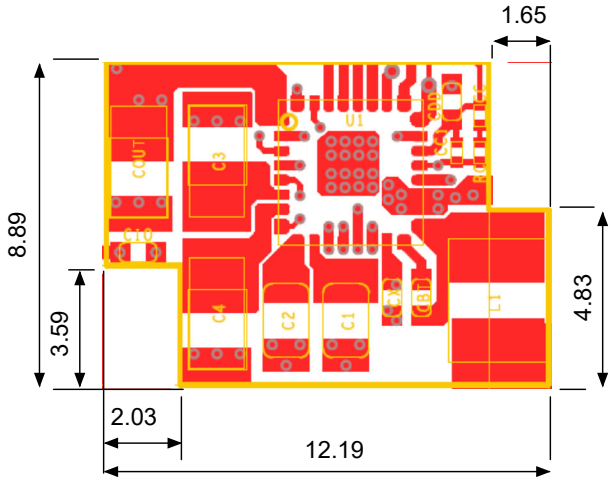


Figure 70: Layout Example

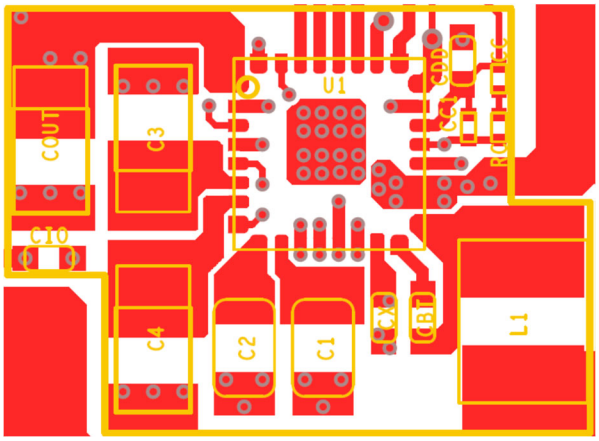


Figure 71: Top Layer

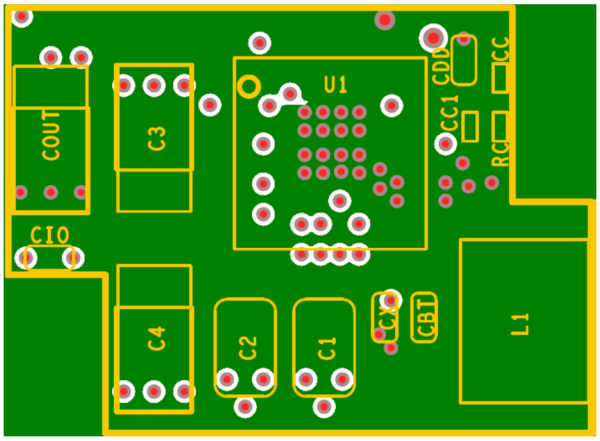


Figure 72: Layer 2

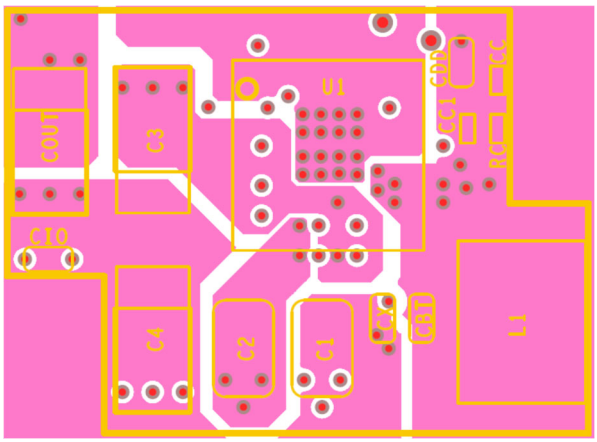


Figure 73: Layer 3

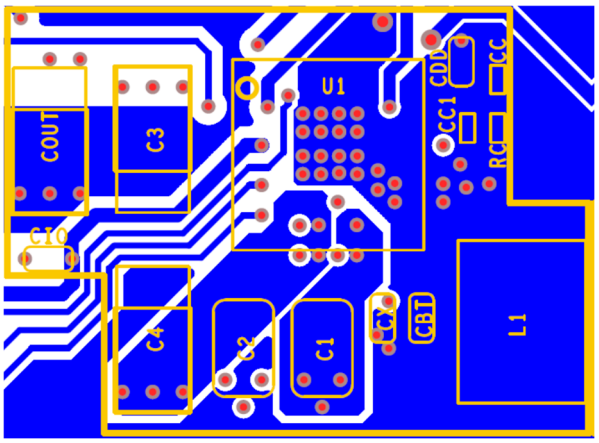


Figure 74: Bottom Layer

Package Mechanical Details

ARC3C0845

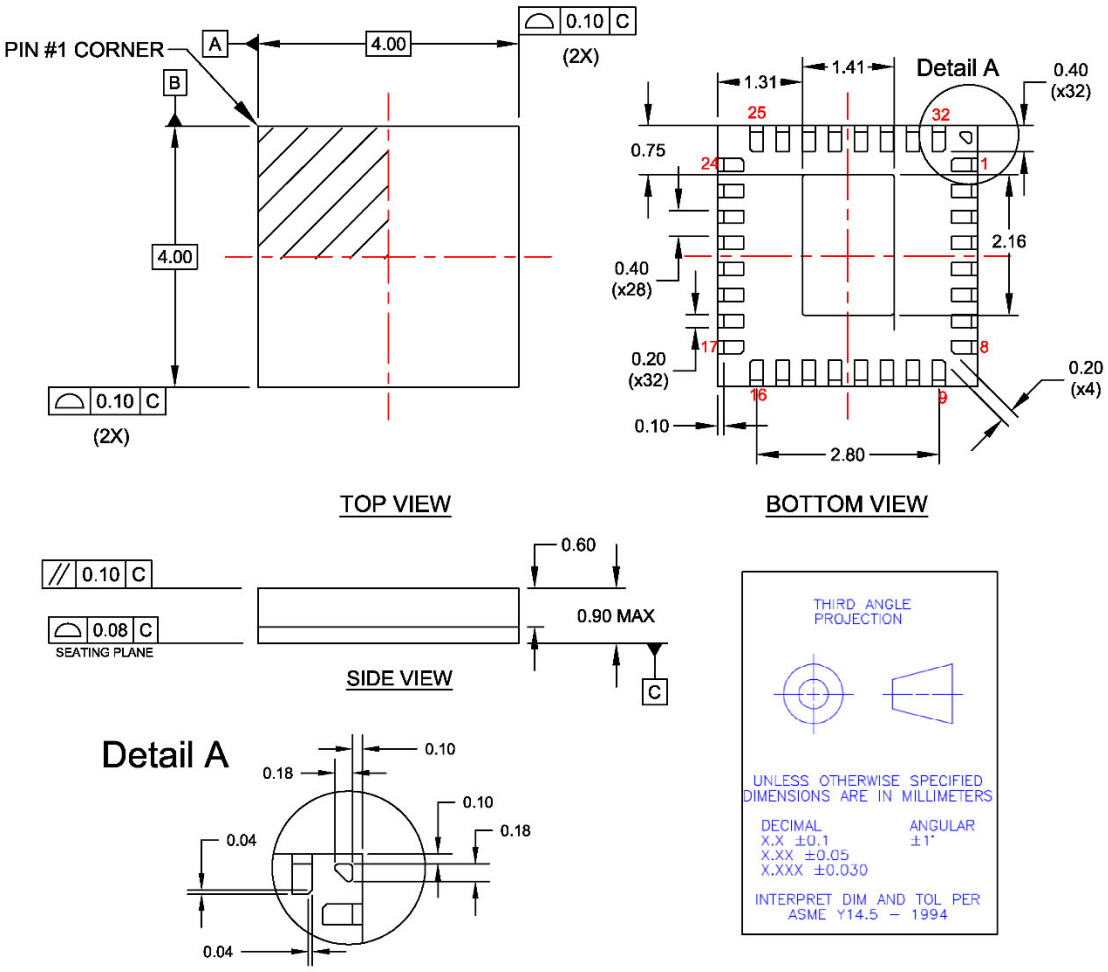
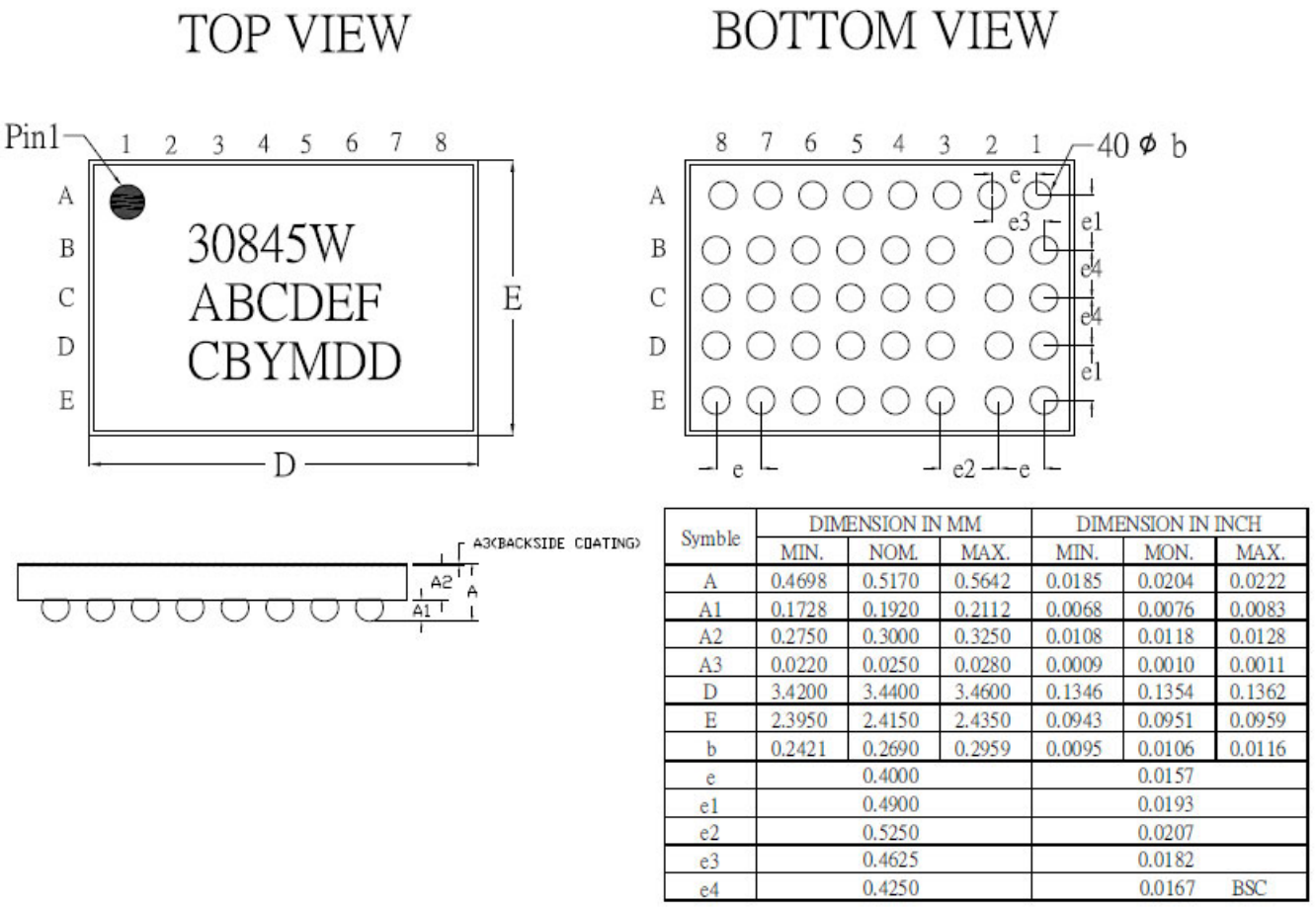


Figure 75: Package Mechanical Details (ARC3C0845)

ARC3C0845W



Symble	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	MON.	MAX.
A	0.4698	0.5170	0.5642	0.0185	0.0204	0.0222
A1	0.1728	0.1920	0.2112	0.0068	0.0076	0.0083
A2	0.2750	0.3000	0.3250	0.0108	0.0118	0.0128
A3	0.0220	0.0250	0.0280	0.0009	0.0010	0.0011
D	3.4200	3.4400	3.4600	0.1346	0.1354	0.1362
E	2.3950	2.4150	2.4350	0.0943	0.0951	0.0959
b	0.2421	0.2690	0.2959	0.0095	0.0106	0.0116
e		0.4000			0.0157	
e1		0.4900			0.0193	
e2		0.5250			0.0207	
e3		0.4625			0.0182	
e4		0.4250			0.0167	BSC

All dimensions in mm

Figure 76: Package Mechanical Details (ARC3C0845W)

Guidelines for PCB Land Design

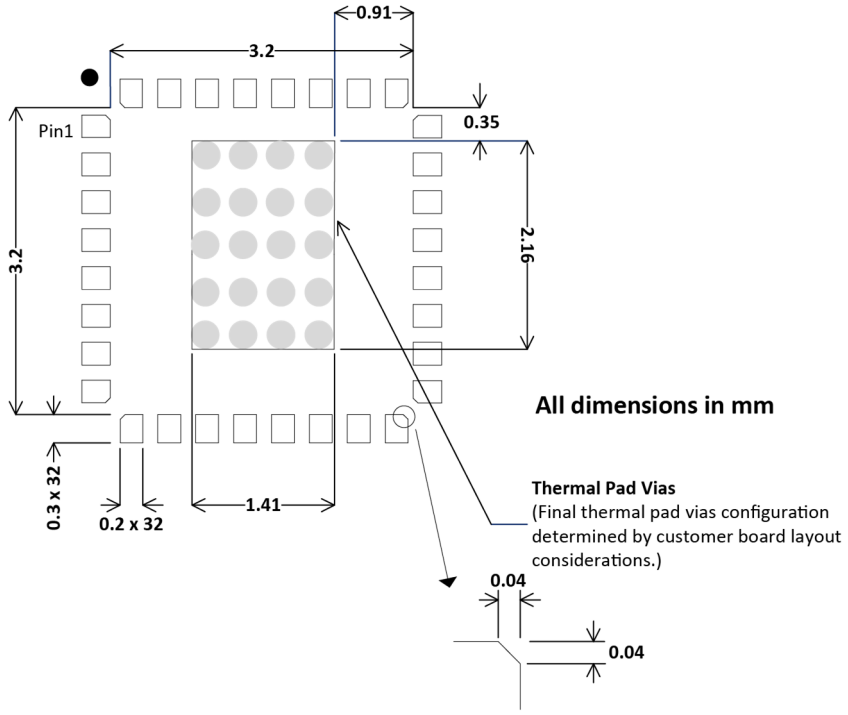


Figure 77: Recommended PCB Footprint for ARC3C08485 32P QFN

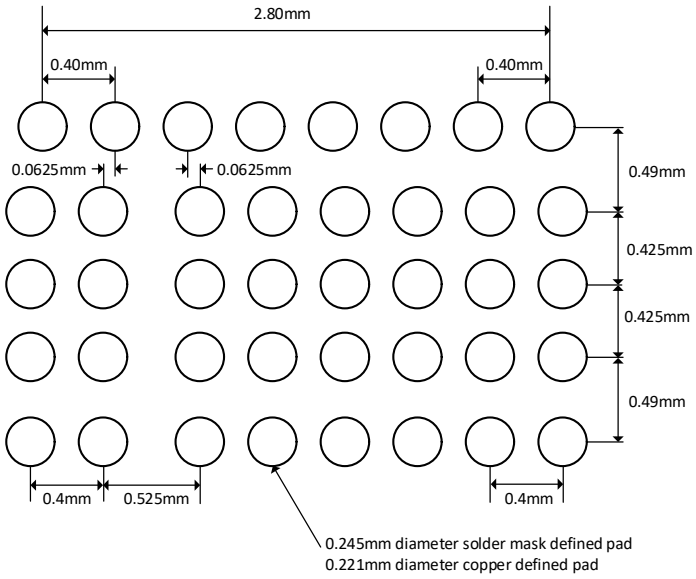


Figure 78: Recommended PCB Footprint for ARC3C08485 WLC SP-40

The solder mask openings should be larger with a typical 0.05 mm ring all around each of the perimeter pads. The center pad is solder mask defined, with the dimensions as given above. The copper for the center pad can be extended beyond the solder mask defined pad as needed to optimize the thermal performance. Put as many thermal vias as possible in this copper. There should be no PCB Layer 1 copper under any package exposed metal, except for the center pad. All the exposed metal is dimensioned in the package mechanical details.

Top Marking Information

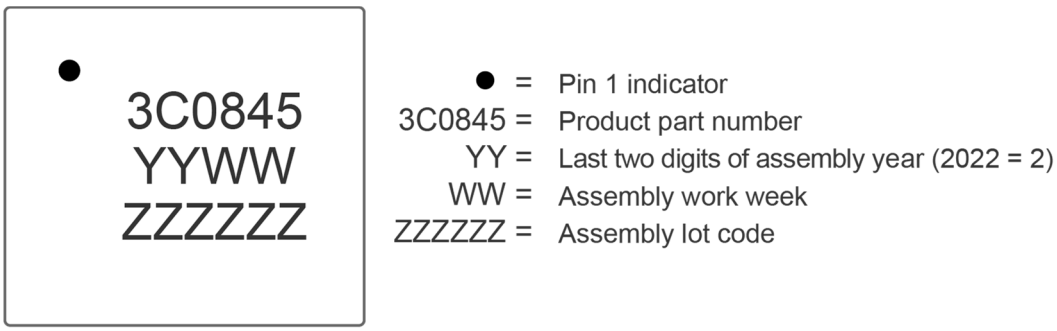


Figure 79: Packaging Marking Information for ARC3C0845

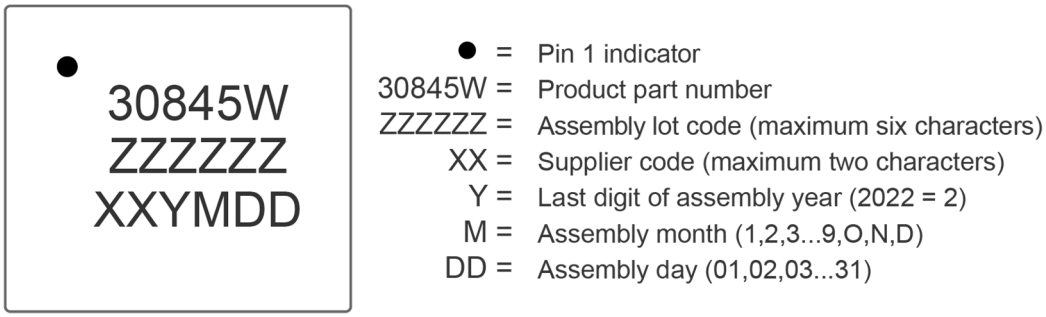
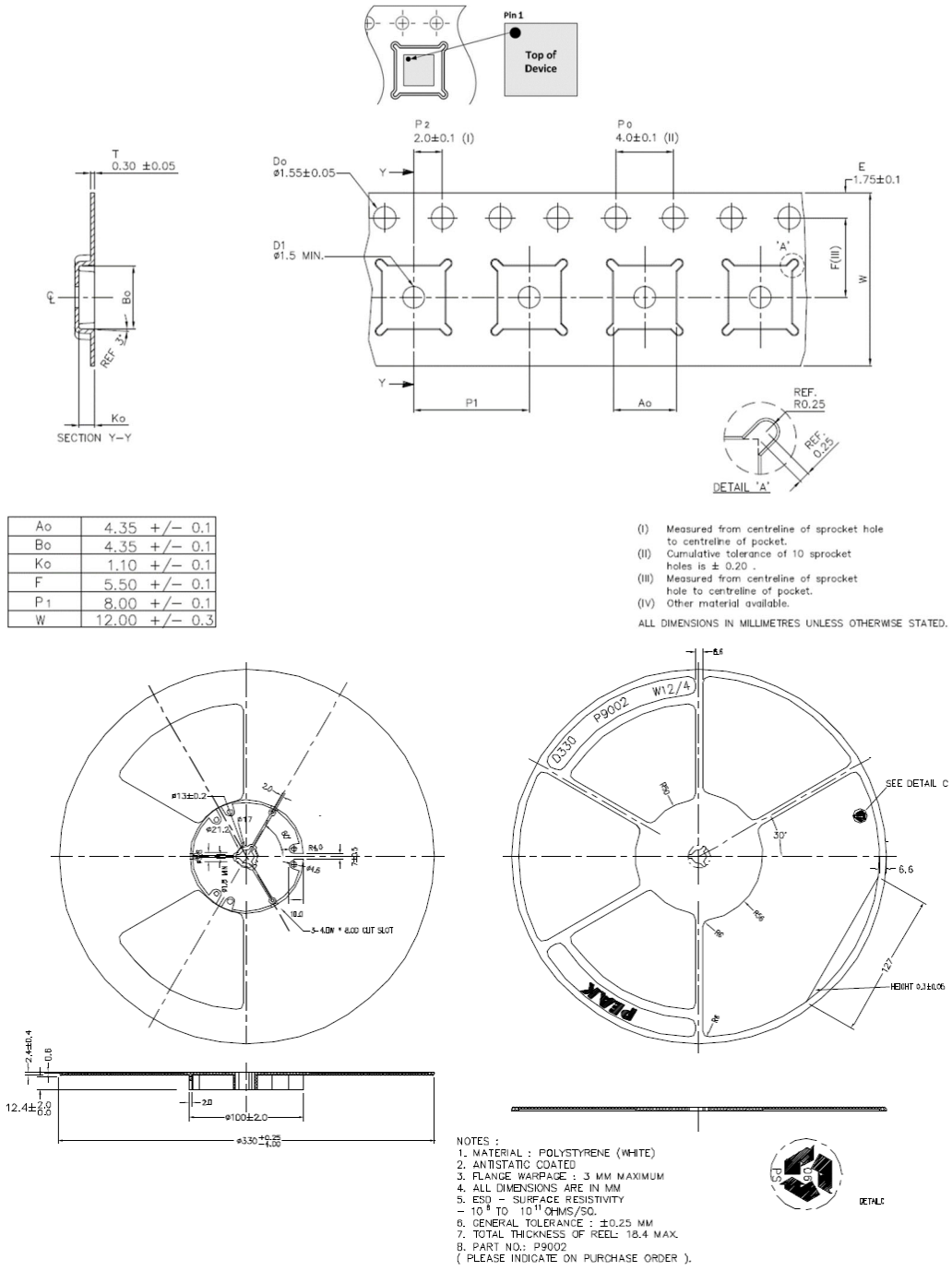


Figure 80: Packaging Marking Information for ARC3C0845W

Tape and Reel Information



Ao	4.35 +/– 0.1
Bo	4.35 +/– 0.1
Ko	1.10 +/– 0.1
F	5.50 +/– 0.1
P1	8.00 +/– 0.1
W	12.00 +/– 0.3

Figure 81: Tape and Reel Information for ARC3C0845

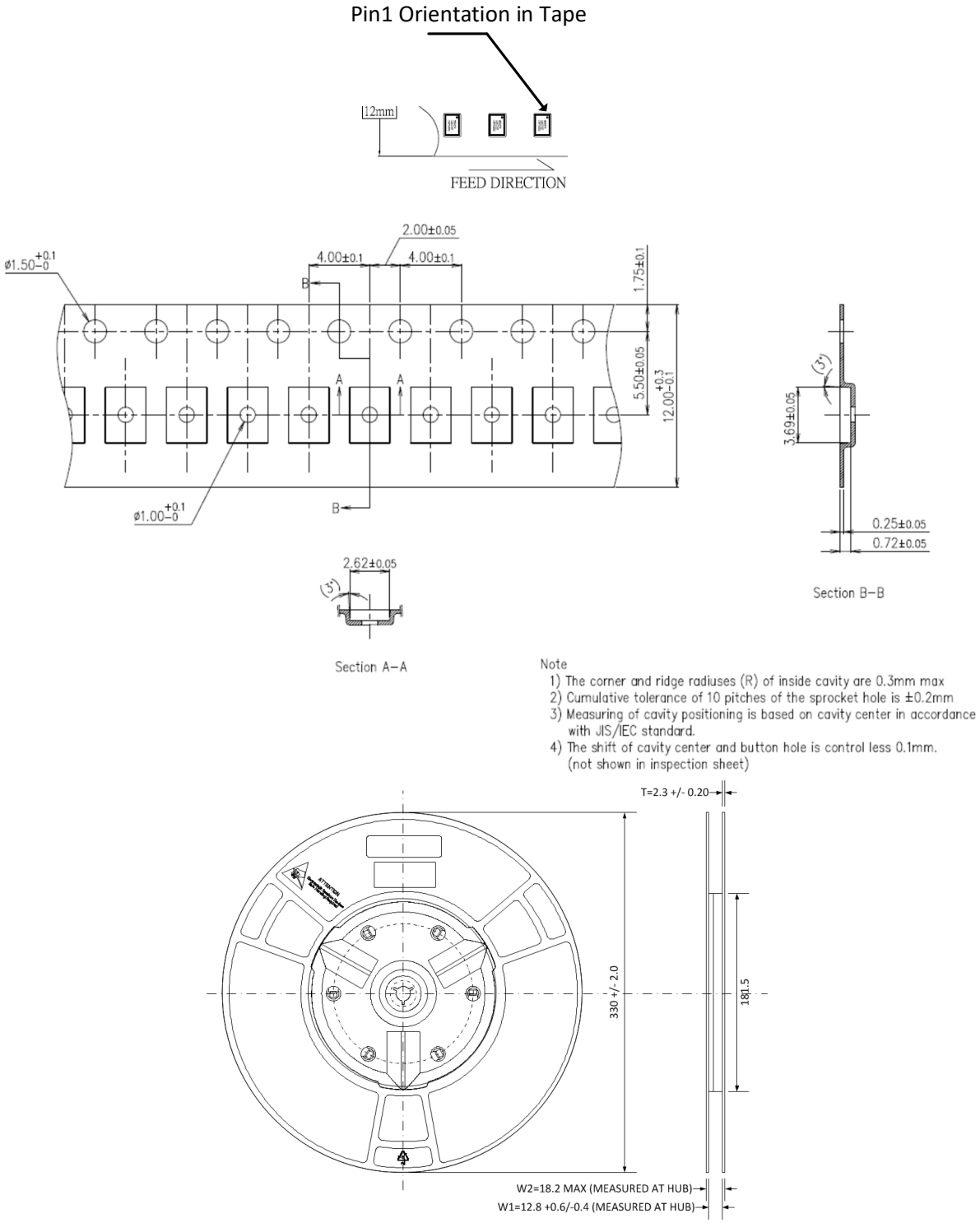


Figure 82: Tape and Reel Information for ARC3C0845W

Ordering Information

TA	PACKAGE	ORDERABLE DEVICE NUMBER	PINS	TRANSPORT MEDIA	MINIMUM ORDER QUANTITY
-30....+85°C	QFN32	ARC3C0845-R	32	Large tape-and-reel	5000
		ARC3C0845-V		Small tape-and-reel	250
		ARC3C0845-G		Sample waffle tray	10
	WLCSP40	ARC3C0845W-R	40	Large tape-and-reel	5000
		ARC3C0845W-V		Small tape-and-reel	250
		ARC3C0845W-G		Sample waffle tray	10

Table 22: Ordering Information

Notices

⚠ CAUTION

Limitation of Applications
Please contact us before using our products for the applications listed below which require especially high reliability for the prevention of defects which might lead to damage to life, body, or property.

- Aircraft equipment
- Aerospace equipment
- Undersea equipment
- Power plant control equipment
- Surgical implants
- Transportation equipment (vehicles, trains, ships, etc.)
- Traffic signal equipment
- Disaster prevention / crime prevention equipment
- Application of similar complexity and/or reliability requirements to the applications listed in the above

⚠ Notes

- Please make sure that your product has been evaluated and confirmed to your specifications when our product is used in your product.
- All the items and parameters in this approval sheet for product specification are based on the premise that our product is used for the purpose, under the condition and in the environment agreed upon between you and us. You are requested not to use our product in a manner deviating from such agreement.
- If you have any concerns about materials other than those listed in the RoHS directive, please contact us.
- Be sure to provide an appropriate fail-safe functionality in your product to prevent secondary damage that could be caused by the abnormal function or failure of our product.
- Do not allow our product to be exposed to excess moisture under any circumstances.

Document Categories

Advance Information
The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification
The datasheet contains preliminary data. Additional data may be added at a later date. Murata reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification
The datasheet contains final data. In the event Murata decides to change the specifications, Murata will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

Product Brief
The datasheet contains summary product information.

Sales Contact
For additional information, contact Sales at **https://www.murata.com/contactform.**

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