ATHEROS

Data Sheet

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Ver. 2.1

AR8035 Integrated 10/100/1000 Mbps Ethernet Transceiver

General Description

The AR8035 is part of the Arctic family of devices - which includes the AR8031, AR8033, and the AR8035. It is Atheros' 4th generation, single port 10/100/1000 Mbps Tri-speed Ethernet PHY. It supports RGMII interface to the MAC.™

The AR8035 provides a low power, low BOM (Bill of Materials) cost solution for comprehensive applications including consumer, enterprise, carrier and home networks such as PC, HDTV, Gaming machines, Blue-ray players, IPTV STB, Media Players, IP Cameras, NAS, Printers, Digital Photo Frames, MoCA/Homeplug (Powerline)/EoC/ adapters and Home Router & Gateways, etc.

The AR8035 integrates Atheros latest Green Ethos® power saving technologies and significantly saves power not only during work time, but also during overtime. Atheros Green Ethos® power savings include ultra-low power in cable unplugged mode or port power down mode, and automatic optimized power saving based on cable length. Furthermore, the AR8035 supports Wake-on-LAN (WoL) feature to be able to help manage and regulate total system power requirements.

The AR8035 embeds CDT (Cable Diagnostics Test) technology on-chip which allows customers to measure cable length, detect the cable status, and identify remote and local PHY malfunctions, bad or marginal patch cord segments or connectors. Some of the possible problems that can be detected include opens, shorts, cable impedance mismatch, bad connectors, termination mismatch, and a bad transformer.

The AR8035 also integrates a voltage regulator on chip. It reduces the termination R/C circuitry on both the MAC interface (RGMII) and line side.

The AR8035 supports IEEE 802.3az Energy Efficient Ethernet (EEE) standard and Atheros proprietary SmartEEE, which allows legacy MAC/SoC devices without 802.3az support to function as the complete 802.3az system. The key features supported by the device are:

- 10BASE-Te PHY supports reduced transmit amplitude.
- 100BASE-TX and 1000BASE-T use Low Power Idle (LPI) mode to turn off unused analog and digital blocks to save power while data traffic is in idle.

Features

- 10BASE-Te/100BASE-TX/1000 BASE-T IEEE 802.3 compliant
- Supports 1000 BASE-T PCS and auto-negotiation with next page support
- Supports RGMII interface to MAC devices with a broad I/O voltage level options including 2.5V, 1.8V and 1.5V, and is compatible with 3.3V I/O
- RGMII timing modes support internal delay and external delay on Rx path
- Error-free operation up to 140 meters of CAT5 cable
- Supports Atheros latest Green Ethos® power saving modes with internal automatic DSP power saving scheme
- Supports 802.3az (Energy Efficient Ethernet)
- Fully integrated digital adaptive equalizers, echo cancellers, and near end crosstalk (NEXT) cancellers
- Supports Wake-on-LAN (WoL) to detect magic packet and notify the sleeping system to wake up
- A robust Cable Discharge Event (CDE) tolerance of ± 6kV
- A robust surge protection with ±750V/ differential mode and ±4KV/common mode
- Jumbo Frame support up to 10KB (full duplex)
- All digital baseline wander correction
- Automatic channel swap (ACS)
- Automatic MDI/MDIX crossover
- Automatic polarity correction
- IEEE 802.3u compliant Auto-Negotiation
- Software programmable LED modes
- Multiple Loopback modes for diagnostics

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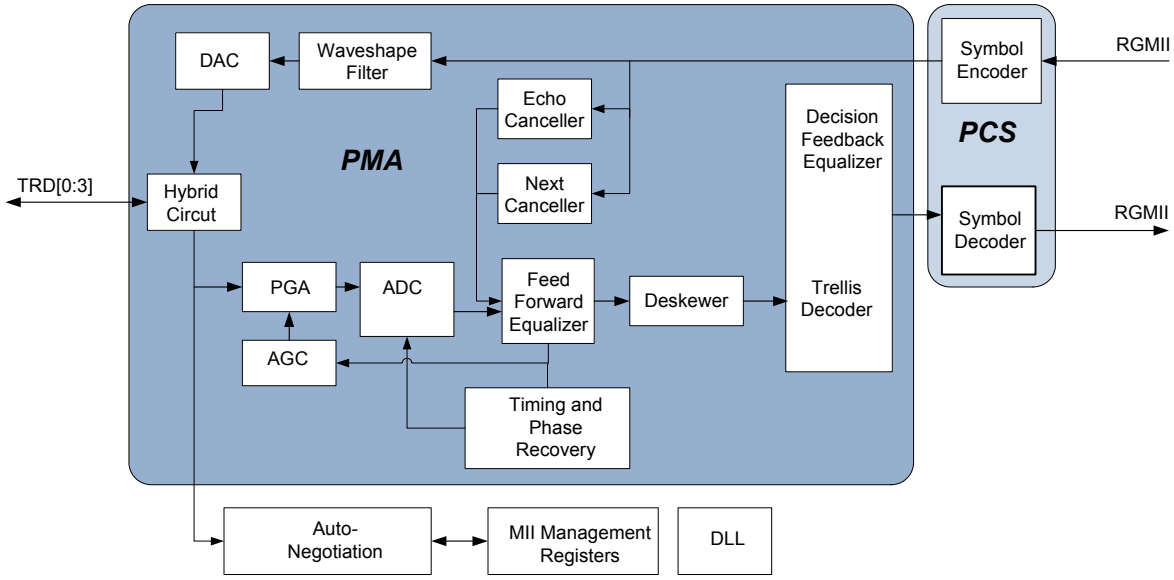
- Cable Diagnostic Test (CDT)
- Single power supply: 3.3V
- 5mm x 5mm. 40-pin QFN package

AR8035 Functional Block Diagram



Revision History

Date	Revsion Details	Revision
2011/3/15	First release	1.0
2011/11/25	Electrical Characteristics ■ Add a note under Recommended Operation Conditions Topside Marking ■ Add topside marking illustration	2.0
2012/3/1	Electrical Characteristics ■ Change MDIO tmdelay minimal value to 0 ns; typical value to 4 ns Ordering information ■ Remove AR8035-AL1B industrial tray pack ordering	2.1

Table of Contents

1. Pin Descriptions

This section contains a package pinout for the AR8035 QFN 40 pin and a listing of the signal descriptions (see Figure 1-1).

The following nomenclature is used for signal names:

Table 1-1.

NC	No connection to the internal die is made from this pin
n	At the end of the signal name, indicates active low signals
P	At the end of the signal name, indicates the positive side of a differential signal
N	At the end of the signal name indicates he negative side of a differential signal

The following nomenclature is used for signal types described in Table 1-1:

Table 1-2.

D	Open drain
IA	Analog input signal
I	Digital input signal
IH	Input signals with weak internal pull-up, to prevent signals from floating when left open
IL	Input signals with weak internal pull-down, to prevent signals from floating when left open
I/O	A digital bidirectional signal
OA	An analog output signal
O	A digital output signal
P	A power or ground signal
PD	Internal pull-down for input
PU	Internal pull-up for input

Figure 1-1 shows the pinout diagram for the AR8035.

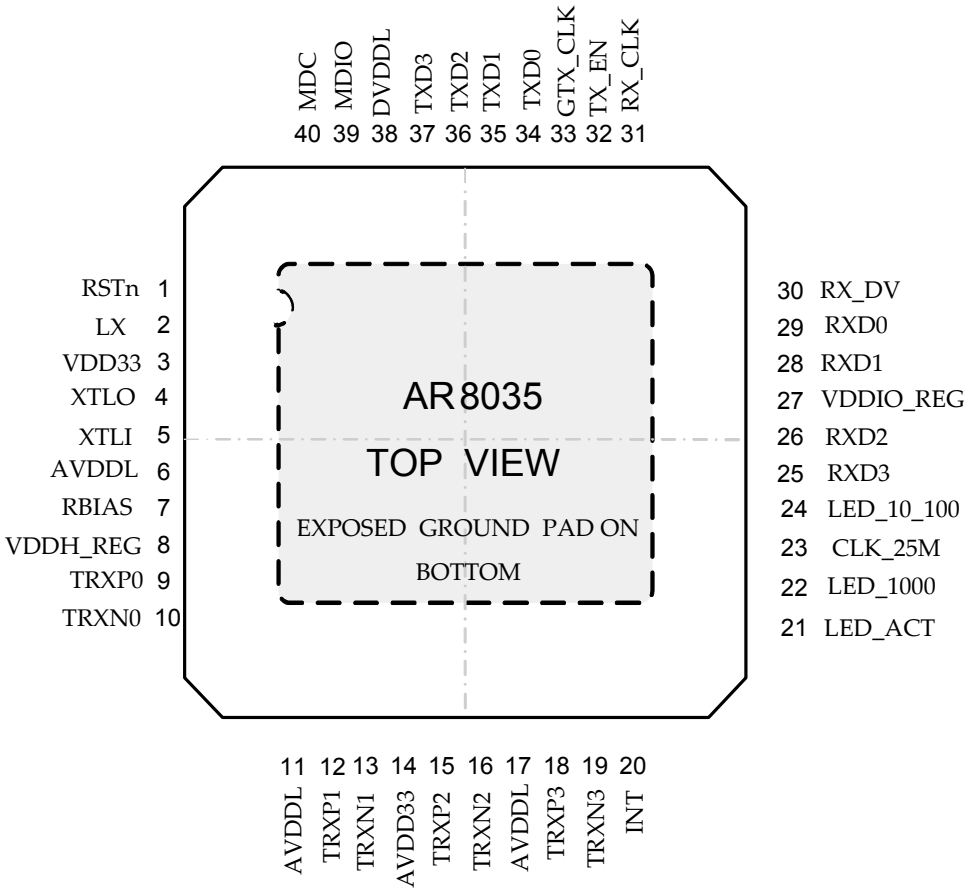


Figure 1-1. **Pinout Diagram**

NOTE: There is an exposed ground pad on the back side of the package.

Table 1-3.

Symbol	Pin	Type	Description
MDI			
TRXP0, TRXN0	9, 10	IA, OA	Media-dependent interface 0, 100 Ω transmission line
TRXP1, TRXN1	12, 13	IA, OA	Media-dependent interface 1, 100 Ω transmission line
TRXP2, TRXN2	15, 16	IA, OA	Media-dependent interface 2, 100 Ω transmission line
TRXP3, TRXN3	18, 19	IA, OA	Media-dependent interface 3, 100 Ω transmission line
RGMII			
GTX_CLK	33	I, PD	RGMII transmit clock, 125 MHz digital. Adding a 22Ω damping resistor is recommended for EMI design near MAC side.
RX_CLK	31	I/O, PD	125MHz digital, adding a 22Ω damping resistor is recommended for EMI design near PHY side.
RX_DV	30	I/O, PD	RGMII receive data valid
RXD0	29	I/O, PD	RGMII received data 0
RXD1	28	I/O, PD	RGMII received data 1
RXD2	26	I/O, PD	RGMII received data 2
RXD3	25	I/O, PD	RGMII received data 3
TX_EN	32	I, PD	RGMII transmit enable
TXD0	34	I, PD	RGMII transmit data 0
TXD1	35	I, PD	RGMII transmit data 1
TXD2	36	I, PD	RGMII transmit data 2
TXD3	37	I, PD	RGMII transmit data 3
Management Interface and Interrupt			
MDC	40	I, PU	Management data clock reference
MDIO	39	I/O, D, PU	Management data, 1.5KΩ pull-up to 3.3V/2.5V
INT	20	I/O, D, PD	Interrupt Signal to System; default OD-gate, needs an external 10KΩ pull-up, active low; can be configured to I/O by register, active high.
LED			
LED_ACT	21	I/O, PU	Parallel LED output for 10/100/1000 BASE-T activity, active blinking. LED active based upon power-on strapping. If pulled up — active low, if pulled down — active high
LED_1000	22	I/O, PU	Parallel LED output for 1000 BASE-T link, LED active based upon power-on strapping. If pulled up — active low, if pulled down — active high

Table 1-3.

Symbol	Pin	Type	Description	
LED_10_100	24	I/O, PU	Parallel LED output for 10/100 BASE-T link. LED active based upon power-on strapping of LED_1000. If LED_1000 is pulled up, this pin is active low; If LED_1000 is pulled-down, active high.	
			High, external PU	10 Mbps
			Low, external PU	100 Mbps
System Signal Group/Reference				
CLK_25M	23	O, PD	25 MHz clock output (default). It can be 125, 62.5 or 50 MHz clock output	
RSTn	1	I	System reset, active low. Requires an external pull-up resistor	
XTLI	5	IA	Crystal oscillator input. Requires a 27 pF capacitor to GND. Support external 25 MHz, 1.2V swing clock input through this pin.	
XTLO	4	OA	Crystal oscillator output; 27 pF to GND	
RBIAS	7	OA	External 2.37 kΩ 1% to GND to set bias current	
Power				
LX	2	OA	Power inductor pin. Add an external 4.7 µH power inductor between this pin and pin 38.	
VDDH_REG	8	OA	2.5 V regulator output. A 1uF capacitor connected to this pin	
VDDIO_REG	27	OA	1.5V/1.8V regulator output.If RGMII interface voltage level is 2.5V, connect this pin to pin 8 directly.	
AVDDL	6, 11, 17	P	1.1 V analog power input. Connect to Pin 38 through a bead	
DVDDL	38	P	1.1 V digital core power input. Connect to power inductor and 10uF+0.1uF ceramic capacitors to GND	
VDD33	3	P	3.3 V power for switching regulator	
AVDD33	14	P	Analog 3.3 V power input for PHY, from VDD33 through a bead	
-	-		Exposed ground pad on back of the chip, tie to ground	

Table 1-4.

PHY Pin	PHY Core Configuration Signal	Description	Default Internal Weak Pull-up/Pull-down
RXD0	PHYADDRESS0	LED_ACT, RXD[1:0] sets the lower three bits of the physical address. The upper two bits of the physical address are set to the default, "00"	0
RXD1	PHYADDRESS1		0
LED_ACT	PHYADDRESS2		1
RX_DV	MODE0	mode select bit 0	0
RXD2	MODE1	mode select bit 1	0
LED_1000	MODE2	mode select bit 2	1
RXD3	MODE3	mode select bit 3	0
RX_CLK	1.8V/1.5V	Select the RGMII/RMII I/O voltage level 1: 1.8V I/O 0: 1.5V I/O	0

NOTE: 0=Pull-down, 1=Pull-up

NOTE: Power on strapping pins are latched during power-up reset or warm hardware reset.

NOTE: Some MAC devices input pins may drive high/low during power-up or reset. So PHY power on strapping status may be affected by the MAC side. In this case an external 10kΩ pull-down or pull-high resistor is needed to ensure a stable expected status.

NOTE: When using 2.5V RGMII I/O voltage level, RX_CLK can be pull-up or pull-down.

Table 1-5.

MODE[3:0]	Description
1100	RGMII, PLLOFF, INT;
1110	RGMII, PLLON, INT;
Others	Reserved

NOTE: PLLOFF means AR8035 can shut down internal PLL in power saving mode; In PLLOFF mode, when the AR8035 enters power saving mode (hibernation), CLK_25m output drops periodically, which saves more power. In PLLON mode, CLK_25M outputs continuously.

2. Functional Description

The AR8035 is Atheros's low cost GbE PHY. It is a highly integrated analog front end (AFE) and digital signal transceiver, providing high performance combined with substantial cost reduction. The AR8035 provides physical layer functions for half/full -duplex 10 BASE-Te, 100 BASE-Tx and 1000 BASE-T Ethernet to transmit and receive high-speed data over standard category 5 (CAT5) unshielded twisted pair cable.

The AR8035 10/100/1000 PHY is fully 802.3ab compliant, and supports the reduced Gigabit Media-Independent Interface (RGMII) to connect to a Gigabit-capable MAC.

The AR8035 transceiver combines echo canceller, near end cross talk (NEXT) canceller, feed-forward equalizer, joint Viterbi, feedback equalizer, and timing recovery, to enhance signal performance in noisy environments.

The AR8035 is a part of the Arctic family of devices — which includes the AR8031, the AR8033, and the AR8035. A comparison of these is shown below.

Table 2-1 shows a feature comparison across the AR8031, AR8033, and AR8035 family.

Table 2-1. **AR8031, AR8033, AR8035 Comparison**

Feature	AR8031	AR8033	AR8035
RGMII	yes	yes	yes
SGMII	yes	yes	
Cu Ethernet**	yes	yes	yes
EEE (802.3az)	yes	yes	yes
Wake-on-LAN	yes	yes	yes
SERDES/Fiber	yes***	yes***	
1588v2	yes		
Sync-E	yes	yes	
Packaging	48-pin	48-pin	40-pin

NOTE: AR8031, AR8033 is pin-to-pin compatible

NOTE: ** 10BASE-Te, 100BASE-TX, 1000BASE-T will be supported

NOTE: *** 100BASE-FX, and 1000BASE-X will be supported

2.1 Transmit Functions

Table 2-2 describes the transmit function encoder modes.

Table 2-2. **Encoder Mode**

Encoder Mode	Description
1000 BASE-T	In 1000 BASE-T mode, the AR8035 scrambles transmit data bytes from the MAC interfaces to 9-bit symbols and encodes them into 4D five-level PAM signals over the four pairs of CAT5 cable.
100 BASE-TX	In 100 BASE-TX mode, 4-bit data from the MII is 4B/5B serialized, scrambled, and encoded to a three-level MLT3 sequence transmitted by the PMA.
10 BASE-Te	In 10 BASE-Te mode, the AR8035 transmits and receives Manchester-encoded data.

2.2 Receive Functions

2.2.1 Decoder Modes

Table 2-3 describes the receive function decoder modes.

Table 2-3. **Decoder Mode**

Decoder Mode	Description
1000 BASE-T	In 1000 BASE-T mode, the PMA recovers the 4D PAM signals after accounting for the cabling conditions such as skew among the four pairs, the pair swap order, and the polarity of the pairs. The resulting code group is decoded into 8-bit data values. Data stream delimeters are translated appropriately and data is output to the MAC interfaces.
100 BASE-TX	In 100 BASE-TX mode, the receive data stream is recovered and descrambled to align to the symbol boundaries. The aligned data is then parallelized and 5B/4B decoded to 4-bit data. This output runs to the MII receive data pins after data stream delimiters have been translated.
10 BASE-Te	In 10 BASE-Te mode, the recovered 10 BASE-Te signal is decoded from Manchester then aligned.

2.2.2 Analog to Digital Converter

The AR8035 device employs an advanced high speed ADC on each receive channel with high resolution, which results in better SNR and lower error rates.

2.2.3 Echo Canceller

A hybrid circuit is used to transmit and receive simultaneously on each pair. A signal reflects back as an echo if the transmitter is not perfectly matched to the line. Other connector or cable imperfections, such as patch panel discontinuity and variations in cable impedance along the twisted pair cable, also result in drastic SNR degradation on the receive signal. The AR8035 device implements a digital echo canceller to adjust for echo and is adaptive to compensate for the varied channel conditions.

2.2.4 NEXT Canceller

The 1000 BASE-T physical layer uses all four pairs of wires to transmit data. Because the four twisted pairs are bundled together, significant high frequency crosstalk occurs between adjacent pairs in the bundle. The AR8035 device uses three parallel NEXT cancellers on each receive channel to cancel high frequency crosstalk. The AR8035 cancels NEXT by subtracting an estimate of these signals from the equalizer output.

2.2.5 Baseline Wander Canceller

Baseline wander results from Ethernet links that AC-couple to the transceivers and from AC coupling that cannot maintain voltage levels for longer than a short time. As a result, transmitted pulses are distorted, resulting in erroneous sampled values for affected pulses. Baseline wander is more problematic in the 1000 BASE-T environment than in 100 BASE-TX due to the DC baseline shift in the transmit and receive signals. The AR8035 device uses an advanced baseline wander cancellation circuit that continuously monitors and compensates for this effect, minimizing the impact of DC baseline shift on the overall error rate.

2.2.6 Digital Adaptive Equalizer

The digital adaptive equalizer removes inter-symbol interference at the receiver. The digital adaptive equalizer takes unequalized signals from ADC output and uses a combination of feedforward equalizer (FFE) and decision

feedback equalizer (DFE) for the best-optimized signal-to-noise (SNR) ratio.

2.2.7 Auto-Negotiation

The AR8035 device supports 10/100/1000 BASE-T Copper auto-negotiation in accordance with IEEE 802.3 clauses 28 and 40. Auto-negotiation provides a mechanism for transferring information between a pair of link partners to choose the best possible mode of operation in terms of speed, duplex modes, and master/slave preference. Auto-negotiation is initiated upon any of the following scenarios:

- Power-up reset
- Hardware reset
- Software reset
- Auto-negotiation restart
- Transition from power-down to power-up
- The link goes down

If auto-negotiation is disabled, a 10 BASE-Te or 100 BASE-TX can be manually selected using the IEEE MII registers.

2.2.8 Smartspeed Function

The Atheros Smartspeed function is an enhanced feature of auto-negotiation that allows the AR8035 device to fall back in speed based on cabling conditions as well as operate over CAT3 cabling (in 10 BASE-T mode) or two-pair CAT5 cabling (in 100 BASE-TX mode).

By default, the Smartspeed feature is enabled. Refer to the register "Smart Speed" on page 47, which describes how to set the parameters. Set these register bits to control the Smartspeed feature:

- Bit [5]: 1 = Enables Smartspeed (default)
- Bits [4:2]: Sets the number of link attempts before adjusting
- Bit [1]: Timer to determine the stable link condition

2.2.9 Automatic MDI/MDIX Crossover

During auto-negotiation, the AR8035 device automatically determines and sets the required MDI configuration, eliminating the need for external crossover cable. If the remote device also implements automatic MDI crossover, the crossover algorithm as described in IEEE 802.3 clause 40.4.4 ensures that only one device performs the required crossover.

2.2.10 Polarity Correction

If cabling has been incorrectly wired, the AR8035 automatically corrects polarity errors on the receive pairs in 1000 BASE-T, 100 BASE-TX and 10 BASE-Te modes.

2.3 Loopback Modes

2.3.1 Digital Loopback

Digital loopback provides the ability to loop transmitted data back to the receiver using digital circuitry in the AR8035 device. Figure 2-1 shows a block diagram of a digital loopback.

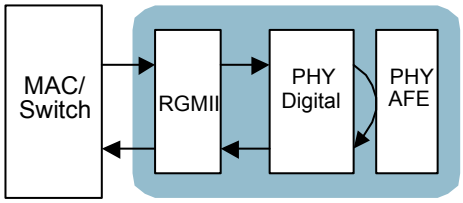


Figure 2-1. **Digital Loopback**

- 1000M loopback: write register 0x0 = 0x4140 to enable 1000M digital loopback.
- 100M loopback: write register 0x0 = 0x6100 to enable 100M digital loopback.
- 10M loopback: write register 0x0 = 0x4100 to enable 10M digital loopback.

2.3.2 External Cable Loopback

External cable loopback loops Tx to Rx through a complete digital and analog path and an external cable, thus testing all the digital data paths and all the analog circuits. Figure 2-2 shows a block diagram of external cable loopback.

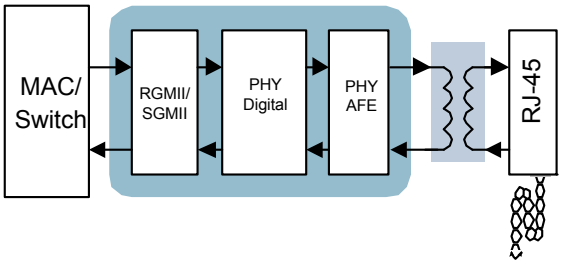


Figure 2-2. **External Cable Loopback**

1. Plug in an external loopback cable (1-3/2-6/4-7/5-8)
2. Write debug register 0xB[15] = 0 to disable hibernate (power-saving mode)
3. Write debug register 0x11[0] = 1 to enable external loopback
4. Select wire speed, as follows:

- 1000M loopback: write register 0x0 = 0x8140 to set 1000M external loopback
- 100M loopback: write register 0x0 = 0xA100 to set 100M external loopback
- 10M loopback: write register 0x0 = 0x0x8100 to set 10M external loopback

5. When the cable in 1000M mode is re-plugged, need to write 0x0 = 0x8140 again to make the PHY link.

2.3.3 Remote PHY Loopback

The Remote loopback connects the MDI receive path to the MDI transmit path, near the RGMII interface, thus the remote link partner can detect the connectivity in the resulting loop. Figure 2-3, below, shows the path of the remote loopback.

Figure 2-3 shows a block diagram of external cable loopback.

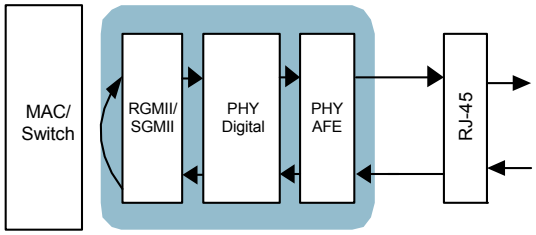


Figure 2-3. **Remote PHY Loopback**

- Write MMD3 register 0x805A[0]= 1 to enable remote PHY loopback.

Please note: The packets from link partner will still appear at RGMII interface when remote loopback is enabled.

Also, remote loopback is independent of PHY auto-negotiation.

2.4 Cable Diagnostic Test

The Cable Diagnostic Test (CDT) feature in the AR8035 device uses Time Domain Reflectometry (TDR) to identify remote and local PHY malfunctions, bad/marginal cable or patch cord segments, or connectors. Some of the possible problems that can be diagnosed include opens, shorts, cable impedance mismatch, bad connectors, termination mismatch, and bad magnetics. The CDT can be performed when there is no link partner or when the link partner is auto-negotiating.

1. Set register 0x16[9:8] to select MDI pair under test
2. Write register 0x16[0]=1 to enable CDT
3. Check register 0x1C[9:8] for fail status
4. Check register 0x1C[7:0] to get delta time. The distance between the fail point and PHY is delta time *0.842

2.5 LED Interface

The LED interface can either be controlled by the PHY or controlled manually, independent of the state of the PHY. Three status LEDs are available. These can be used to indicate operation speed, duplex mode, and link status. The LEDs can be programmed to different status functions from their default value. They can also be controlled directly from the MII register interface.

The reference design schematics for the AR8035's LEDs are shown

Figure 2-4 Reference Design Schematic — Active Low

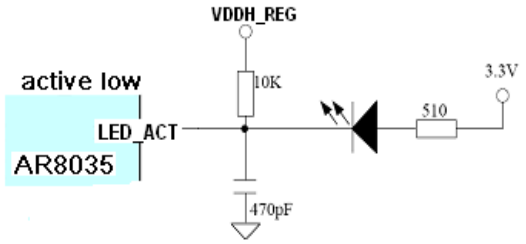


Figure 2-4. **Reference Design Schematic — Active Low**

Figure 2-5 Reference Design Schematic — Active High

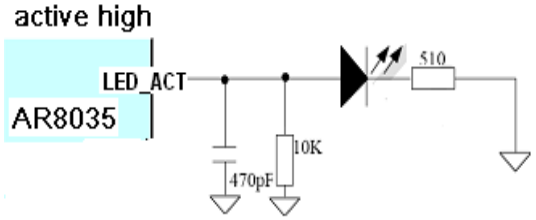


Figure 2-5. **Reference Design Schematic — Active High**

LED_ACT/LED_1000 active states depend on power on strapping mode.

When strapped high, active low. When strapped low, active high.

LED_10_100 depends on LED_1000 power on strapping mode.

So LED_10_100 and LED_1000 should have the same LED design.

Table 2-4. **LED Status**

Symbol	10M Link	10M Active	100M Link	100M Active	1000M Link	1000M Active
LED_10_100	OFF	OFF	ON	ON	OFF	OFF
LED_1000	OFF	OFF	OFF	OFF	ON	ON
LED_ACT	ON	BLINK	ON	BLINK	ON	BLINK

NOTE: Notes: on = active; off = inactive

2.6 Power Supplies

The AR8035 device requires only one external power supply: 3.3 V.

Inside the chip there is a 3.3V rail, 2.5V rail, 1.1V rail and a 1.8V/1.5V rail.

AR8035 integrates a switch regulator which converts 3.3V to 1.1V at a high-efficiency for core power rail. (It is optional for an external regulator to provide this core voltage).

The AR8035 integrates two on chip LDOs which can support 2.5V; 1.5V/1.8V RGMII I/O voltage. Also with 2.5V RGMII I/O voltage configuration AR8035 can work with a 3.3V MAC RGMII interface — because the input can bear 3.3V logic signal, and the output logic VoH and VoL can satisfy the 3.3V LVCMOS/LVTTL requirement. The parameter details are in the Electrical Characteristics chapter.

Reference design for 2.5V RGMII voltage level is shown below:

Figure 2-6 shows the AR8035 reference design for a 2.5V RGMII voltage level.

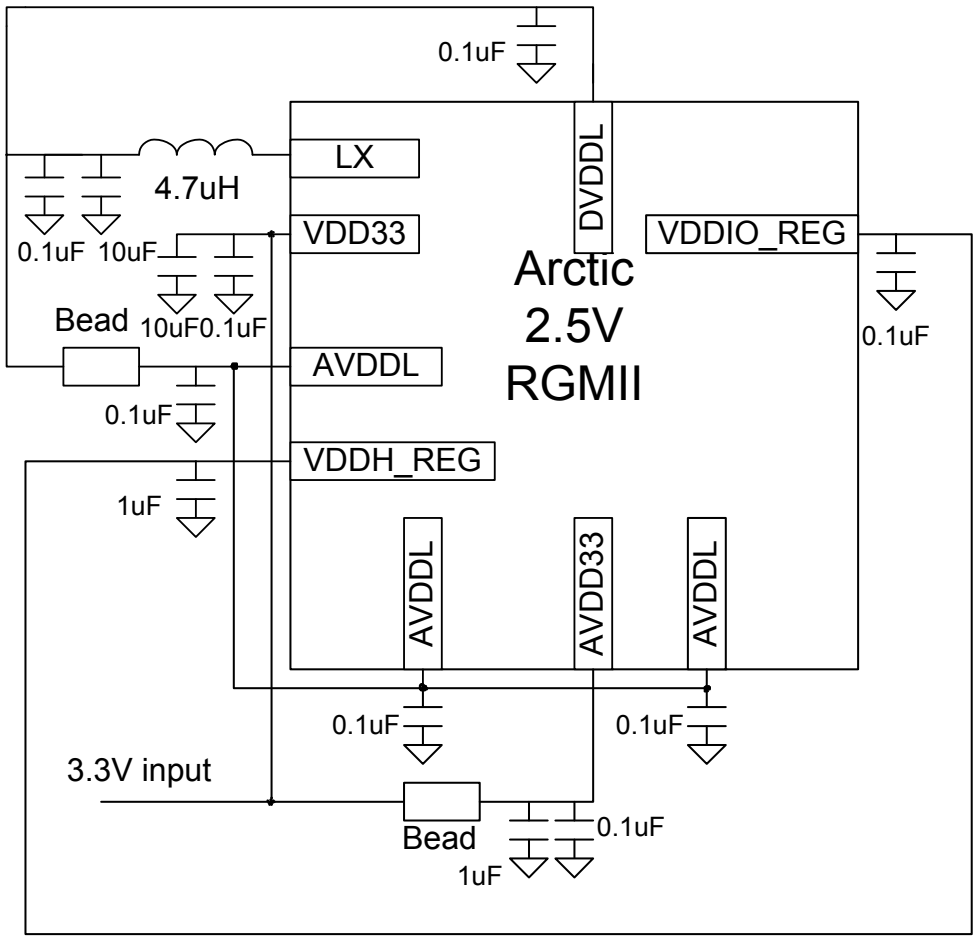


Figure 2-6. **AR8035 reference design for a 2.5V RGMII voltage level**

Reference design for 1.5/1.8V RGMII voltage level is shown below:

Figure 2-7 shows the AR8035 reference design for a 1.5/1.8V RGMII voltage level.

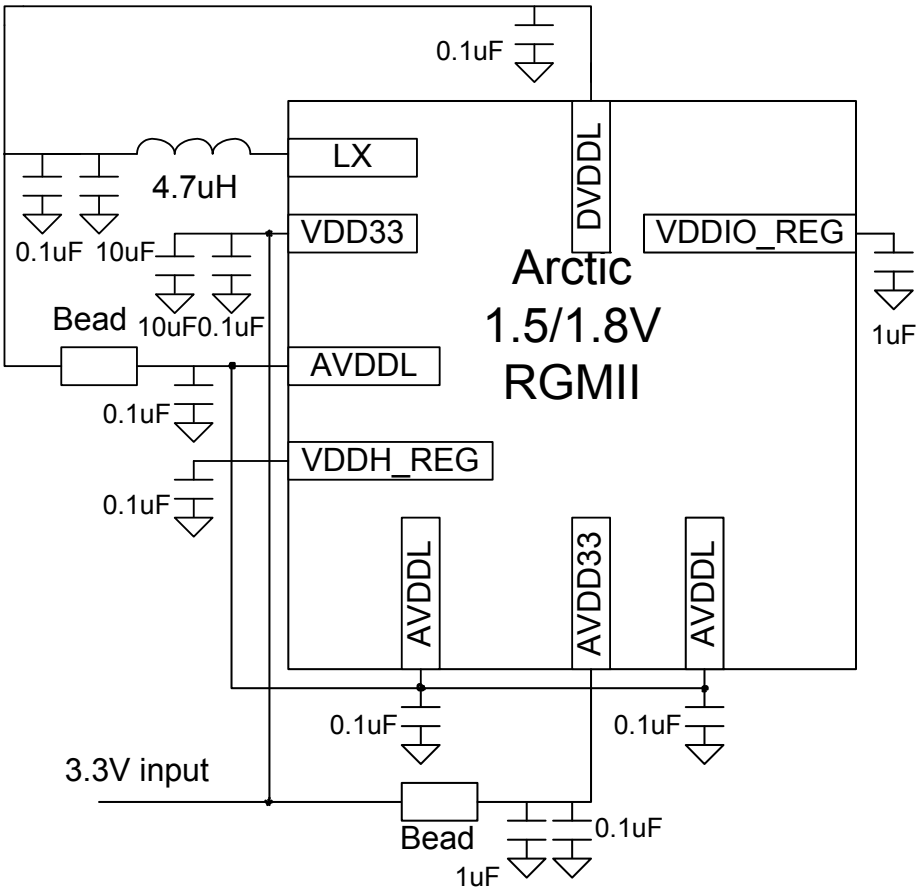


Figure 2-7. **AR8035 reference design for a 1.5/1.8V RGMII voltage level**

2.7 Management Interface

The AR8035 integrates an MDC/MDIO management interface which is compliant with IEEE802.3u clause 22.

MDC is an input clock reference provided by the MAC.

MDIO is the management data input/output bi-directional signal that runs synchronously to MDC.

MDIO is an OD-gate, needs an external 1.5k pull-up resistor.

Definition of the management frame is shown below.

Figure 2-8 shows the AR8035 Management frame fields.

	Management frame fields							
	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
READ	1...1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
WRITE	1...1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

Figure 2-8. **AR8035 Management Frame Fields**

1. PRE is a sequence of 32 contiguous logic one bits on MDIO with 32 corresponding cycles on MDC to provide the PHY with a pattern that it can use to establish synchronization.
2. ST is start of frame
3. OP is the operation code. The operation code for a read transaction is <10>, while the operation code for a write transaction is <01>.
4. PHYAD is 5 bits PHY address. PHY address of AR8035 is configured by power on strapping. There are three address bits can be configured in AR8035 which means 8 PHYs can be connected to the same management interface. Each PHY connected to the same bus line should have a unique PHY address. The first PHY address bit transmitted and received is the MSB of the address.
5. The Register Address is five bits, allowing 32 individual registers to be addressed within each PHY. The first Register Address bit transmitted and received is the MSB of the address.
6. TA is 2 bits to avoid contention during a read operation. For a read operation, both the MAC and PHY shall remain in a high-impedance state for the first bit time. The PHY shall drive a zero during the second bit time of the turnaround. During a write transaction, the MAC must drive 10.
7. Data is the 16 bits data from accessed register. MSB is transmitted first.
8. Idle is a high-impedance without driving state of the MDIO. At least one clocked idle state is required between frames.

There are three kinds of registers in AR8035. All can be accessed using the management frames.

1. IEEE defined 32 MII registers.
2. Atheros defined Debug registers.
3. IEEE defined MDIO Manageable Device (MMD) register

MII register can be access directly through the frame defined above.

Debug register access:

1. Write the debug offset address to 0x1D
2. Read/ Write the data from/to 0x1E

MMD register access:

See detail in register description

example: Write 0x8000 to Register 0 of MMD3

1. Write 0x3 to register 0xD: 0xD=0x0003; (function= address; set the device address)
2. Write 0x0 to register 0xE: 0xE=0x0; (set the register offset address)
3. Write 0x4003 to register 0xD:0xD=0x4003; (function = data; keep the device address)
4. Read register 0xE:0xE==(data from register 0x0 of MMD3)
5. Write 0x8000 to register 0xE:0xE = 0x8000 (write 0x8000 to register 0x0 of MMD3)

NOTE: Read operation please refers to process 1 ~ 4

2.8 Atheros Green Ethos®

2.8.1 Low Power Modes

The AR8035 device supports the software power-down low power mode. The standard IEEE power-down mode is entered by setting the POWER_DOWN bit (bit [11]) of the register "Control" equal to one. In this mode, the AR8035 ignores all MAC interface signals except the MDC/MDIO. It does not respond to any activity on the CAT 5 cable. The AR8035 cannot wake up on its own. It can only wake up by setting the POWER_DOWN bit of the "Control" register to 0, or a Hardware Reset See Table 4.1.1 on page 32.

2.8.2 Shorter Cable Power Mode

With Atheros latest proprietary Green Ethos® power saving technology, the AR8035 can attain an additional 25% power savings when a cable length is detected that is < 30M vs. standard power consumption for a 100M Cat5 cable. The equals and additional 100mW power savings and less than 350mW total power for 1000BASE-T mode in a typical home application.

2.8.3 Hibernation Mode

The AR8035 supports hibernation mode. When the cable is unplugged, the AR8035 will enter hibernation mode after about 10 seconds. The power consumption in this mode can go as low as 10mW only when compared to the normal mode of operation. When the cable is re-

connected, the AR8035 wakes up and normal functioning is restored.

2.9 IEEE 802.3az and Energy Efficient Ethernet

IEEE 802.3az provides a mechanism to greatly save the power consumption between data packets bursts. The link partners enter Low Power Idle state by sending short refresh signals to maintain the link.

There are two operating states, Active state for normal data transfer, and Low-power state between the data packet bursts.

In the low-power state, PHY shuts off most of the analog and digital blocks to reserve energy. Due to the bursty traffic nature of Ethernet, system will stay in low-power mode in the most of time, thus the power saving can be more than 90%.

At the link start up, both link partners exchange information via auto negotiation to determine if both parties are capable of entering LPI mode.

Legacy Ethernet products are supported, and this is made transparent to the user.

2.9.1 IEEE 802.3az LPI Mode

AR8035 works in the following modes when 802.3 az feature is turned on:

- Active: the regular mode to transfer data
- Sleep: send special signal to inform remote link of entry into low-power state
- Quiet: No signal transmitted on media, most of the analog and digital blocks are turned off to reduce energy.
- Refresh: send periodically special training signal to maintain timing recovery and equalizer coefficients
- Wake: send special wake-up signal to remote link to inform of the entry back into Active.

Figure 2-9 shows the 802.3az operating states for the AR8035.

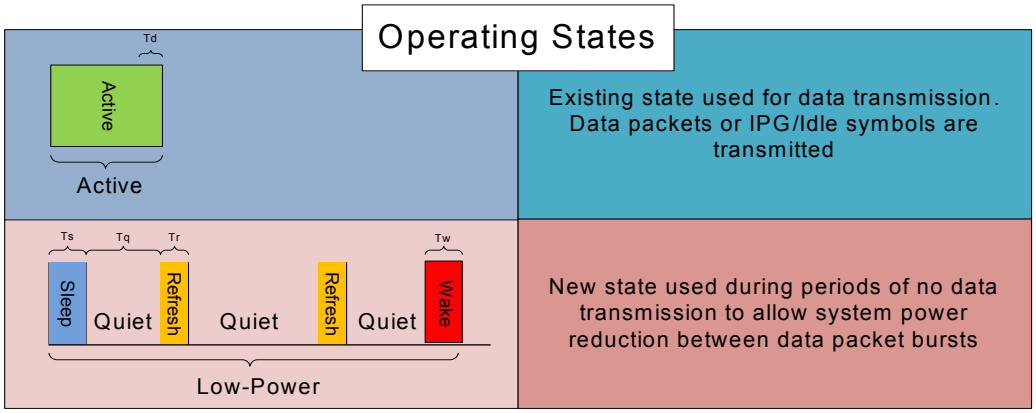


Figure 2-9. **Operating States — 802.3az LPI Mode**

Figure 2-10 shows the 802.3az operating power modes — 802.3az for the AR8035.

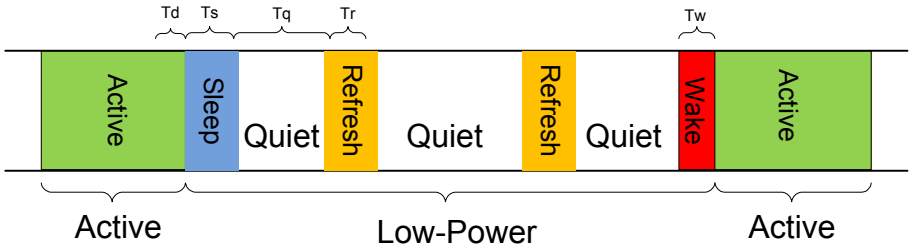


Figure 2-10. **Operating Power Modes — 802.3az LPI Mode**

The AR8035 supports both 100BASE-TX EEE and 1000BASE-T EEE.

100BASE-TX EEE allows asymmetrical operation, which allows each link partner to enter the LPI mode independent of the other partner.

1000BASE-T EEE requires symmetrical operation, which means that both link partners must enter the LPI mode simultaneously.

2.10 Atheros SmartEEE

AR8035 SmartEEE is compatible with normal 802.3az standard. It helps legacy MAC without EEE ability to work as a complete EEE power saving system.

AR8035 SmartEEE will detect egress data flow, if there are no packets to transfer after a defined time which are configurable based on system design, it will enter EEE mode. If there are packets need to transfer, AR8035 will wait typically 16.5us to wake up as 802.3az defined and send out data after the timer configuration in register. It provides a 2048*20bit buffer for egress data before waking up to ensure no packet loss.

AR8035 default mode enables smart EEE after power on or hardware reset.

Working in smartEEE, AR8035 RX side will not generate MDI LPI pattern. So only normal packets and idle packets will appear on the RGMII interface. There is no TX LPI pattern at all if MAC has no EEE capability. LPI is generated inside PHY according to smartEEE mechanism.

If the MAC has EEE capability, can write SmartEEE control register to bypass SmartEEE function.

Please Note:

1. Wait time before entering EEE mode is in register MMD3 0x805c,0x805d[7:0];
2. Adjustable wait time before sending out data is in register MMD3 0x805b, To cooperate with link partner for special requirement.

2.11 Wake On LAN (WoL)

Originally Wake-on-LAN (WoL) was an Ethernet networking standard that allowed a computer to be turned on (or woken up) by a network message for administrator attention, etc. However as part of the latest industry trend towards energy savings, WoL gets wide interest to be adopted across networking systems as a mechanism to help to manage and regulate the total power consumed by the network. The AR8035 supports Wake-on-LAN (WoL):

- Able to enter the sleep/isolate state (PHY's all TX bus (including clock) are in High-Z state, but PHY can still receive packets) by ISOLATE bit in MII register configuration
- Consumes less than 50mW when in sleep/isolate mode
- Supports automatic detection of magic packets (a specific frame containing anywhere within its payload: 6 bytes of ones (resulting in hexadecimal FF FF FF FF FF FF), followed by sixteen repetitions of the target computer's MAC address) and notification via hardware interrupt.
- Supports exit from the sleep state, by register configuration

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1 summarizes the absolute maximum ratings and Table 3-2 lists the recommended operating conditions for the AR8035. Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

Table 3-1. **Absolute Maximum Rating**

Symbol	Parameter	Max Rating	Unit
V_{DD33}	3.3V analog supply voltage	3.8	V
A_{VDD}	1.1V analog supply voltage	1.6	V
D_{VDD}	1.1V digital core supply voltage	1.6	V
T_{store}	Storage temperature	–65 to 150	°C
HBM	Electrostatic discharge tolerance - Human Body Model	±2kV	V
MM	Machine Model	±200V	V
CDM	Charge Device Model	±500V	V

3.2 Recommended Operating Conditions

Table 3-2. **Recommended Operating Conditions**

Symbol	Parameter	Min	Typ	Max	Unit
VDD33/AVDD33	3.3V supply voltage	3.14	3.3	3.47	V
AVDDL/DVDDL	1.1V digital core supply voltage	1.04	1.1	1.17	V
T_A	Ambient temperature for normal operation - Commercial chip version	0	—	70	°C
T_A	Ambient temperature for normal operation - Industrial chip version	-40	—	85	°C
T_J	Junction temperature	-40	—	125	°C
Ψ_{JT}	Thermal Dissipation Coefficient	—	4	—	°C/W

NOTE: External regulators are optional for supplying AVDDL/DVDDL. For industrial version, external AVDDL/DVDDL inputs must be within the range of 1.2 V ±5%. For commercial version, external AVDDL/DVDDL inputs must be within the range of 1.1 V-5% and 1.2 V+5%.

NOTE: The following condition must be satisfied:

$$T_{Jmax} > T_{Cmax} + \Psi_{JT} \times P_{Typical}$$

Where:

T_{Jmax} = maximum allowable temperature of the Junction

T_{Cmax} = Maximum allowable case temperature

Ψ_{JT} = Thermal Dissipation Coefficient
$P_{Typical}$ = Typical power dissipation

3.3 RGMII Characteristics

Table 3-3 shows the RGMII DC characteristics with 2.5/3.3V I/O supply.

Table 3-3. **RGMII Characteristics with 2.5V 3.3V Supply**

Symbol	Parameter	Min	Max	Unit
I_{IH}	Input high current	—	15	µA
I_{IL}	Input low current	–15	—	µA
V_{IH}	Input high voltage	1.7	3.5	V
V_{IL}	Input low voltage	—	0.7	V
V_{OH}	Output high voltage	2.4	2.8	V
V_{OL}	Output low voltage	GND – 0.3	0.4	V

Table 3-4 shows the RGMII DC characteristics with 1.8V I/O supply.

Table 3-4. **RGMII Characteristics with 1.8V Supply**

Symbol	Parameter	Min	Max	Unit
V_{IH}	Input high voltage	1.4	—	V
V_{IL}	Input low voltage	—	0.4	V
V_{OH}	Output high voltage	1.5	—	V
V_{OL}	Output low voltage	—	0.3	V

Table 3-5 shows the RGMII DC characteristics with 1.5V I/O supply.

Table 3-5. **RGMII Characteristics with 1.5V Supply**

Symbol	Parameter	Min	Max	Unit
V_{IH}	Input high voltage	1.2	—	V
V_{IL}	Input low voltage	—	0.3	V
V_{OH}	Output high voltage	1.3	—	V
V_{OL}	Output low voltage	—	0.2	V

Figure 3-1 shows the RGMII AC timing diagram — no internal delay.

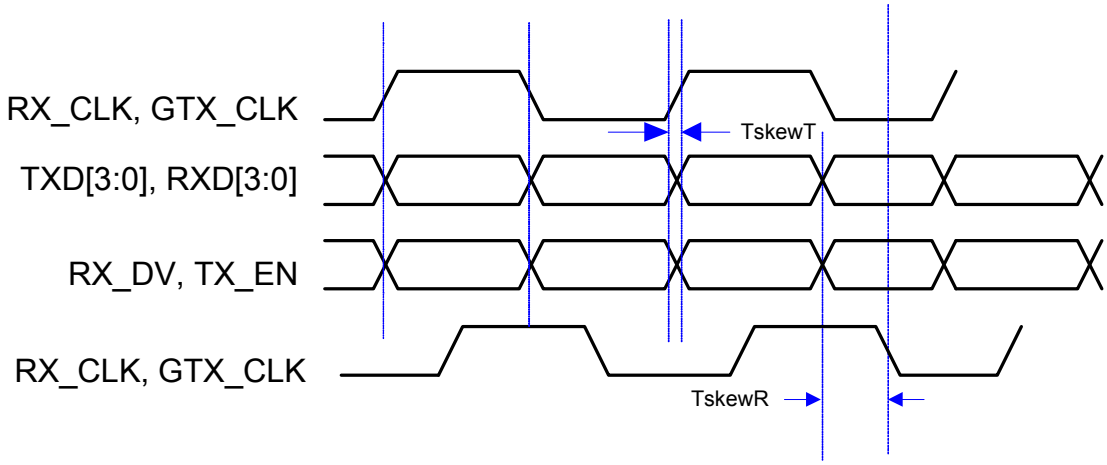


Figure 3-1. **RGMII AC Timing Diagram — no Internal Delay**

Table 3-6 shows the RGMII AC characteristics.

Table 3-6. **RGMII AC Characteristics**

Symbol	Parameter	Min	Typ	Max	Unit
T_{skewT}	Data to clock output skew (at Transmitter)	-500	0	500	ps
T_{skewR}	Data to clock output skew (at Receiver)	1	—	—	ns
T_{cyc}	Clock cycle duration	7.2	8.0	8.8	ns
Duty_G	Duty cycle for Gigabit	45	50	55	%
Duty_T	Duty cycle for 10/100T	40	50	60	%
T_r/T_f	Rise/Fall time (20 - 80%)	—	—	0.75	ns

Figure 3-2 shows the RGMII AC timing diagram with internal delay added (default RGMII timing).

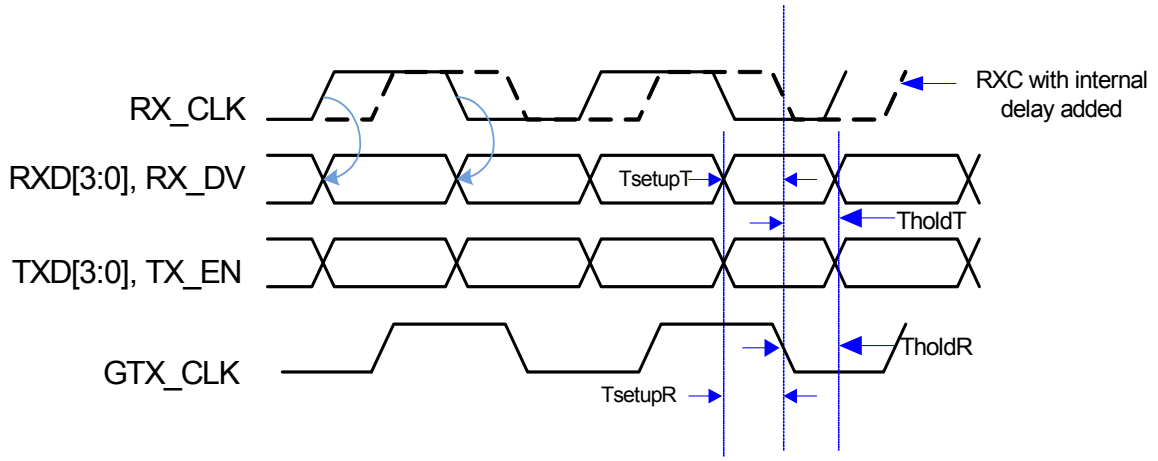


Figure 3-2. **RGMII AC Timing Diagram — With Internal Delay Added (Default)**

Table 3-7 shows the RGMII AC characteristics with delay added.

Table 3-7. **RGMII AC Characteristics with Delay**

Symbol	Parameter	Min	Typ	Max	Unit
TsetupT	Data to Clock output Setup (at Transmitter — integrated delay)	1.65	2.0	2.2	ns
TholdT	Clock to Data output Hold (at Transmitter — integrated delay)	1.65	2.0	2.2	ns
TsetupR	Data to Clock input setup Setup (at Receiver — integrated delay)	1.0	2.0		ns
TholdR	Data to Clock output setup Setup (at Receiver — integrated delay)	1.0	2.0		ns

3.4 MDIO Characteristics

MDIO is OD-gate, and can be pulled-up to 2.5/3.3V.

Table 3-8 shows the MDIO DC characteristics.

Table 3-8. **MDIO Characteristics**

Symbol	Parameter	Min	Max	Unit
I_{IH}	Input high current	—	0.4	mA
I_{IL}	Input low current	0.4	—	mA
V_{OH}	Output high voltage	2.4	—	V
V_{OL}	Output low voltage	—	0.4	V
V_{IH}	Input high voltage	2.0	—	V
V_{IL}	Input low voltage	—	0.8	V

Table 3-9 shows the MDIO AC Characteristics.

Table 3-9. **MDIO AC Characteristics**

Symbol	Parameter	Min	Typ	Max	Unit
tmdc	MDC Period	40			ns
tmdcl	MDC Low Period	16			ns
tmdch	MDC High Period	16			ns
tmdsu	MDIO to MDC rising setup time	10			ns
tmdhold	MDIO to MDC rising hold time	10			ns
tmdelay	MDC to MDIO output delay	0	4		ns

3.5 XTAL/OSC Characteristics

Table 3-10. **XTAL/OSC Characteristics**

Symbol	Parameter	Min	Typ	Max	Unit
T_XI_PER	XI/OSCI Clock Period	40.0 - 50ppm	40.0	40.0 + 50ppm	ns
T_XI_HI	XI/OSCI Clock High	14	20.0		ns
T_XI_LO	XI/OSCI Clock Low	14	20.0		ns
T_XI_RISE	XI/OSCI Clock Rise Time, VIL (max) to VIH (min)			4	ns
T_XI_FALL	XI/OSCI Clock Fall time, VIL (max) TO VIH (min)			4	ns
V_IH_XI	The XI input high level	0.8	1.2	1.5	V
V_IL_XI	The XI input low level voltage	- 0.3	0	0.15	V
Cin	Load capacitance		1	2	pF
Jitter_rms	Period broadband rms jitter			15	ps
Jitter_pk-pk	Period broadband PK-PK jitter			200	ps

Table 3-11. **XTAL/OSC Selection**

Symbol	Min	Typ	Max	Unit
Frequency	-50ppm	20, 50, 62.5, 125	+50ppm	MHz
Output high voltage	2.3	2.62	2.8	V
Output low voltage	GND-0.3	0	0.4	V
JitterRMS			15	ps
JitterPK-PK			125	ps

NOTE: CLK_25M default outputs 25MHz, can be configured to 50MHz, 62.5MHz, or 125MHz by register MMD7 8016[4:3].

NOTE: The jitter result is broadband period jitter with 100000 samples.

3.6 Power Pin Consumption

Table 3-12. **Power Pin Consumptions**

Symbol	Voltage Range	Current
AVDDL	1.1V ±5%	50.8 mA
DVDDL	1.1V ±5%	113.7 mA
AVDD33	3.3V ±5%	63.8 mA
VDDIO_REG	Connect VDDH_REG 2.5V	20.9 mA

NOTE: Data for components selection and layout guide

3.7 Typical Power Consumption Parameters

The following conditions apply to the typical characteristics unless otherwise specified:
VCC = 3.3V (1.1V switching regulator integrated. 1.8V RGMII power included).

Table 3-13. **Typical Power Consumptions**

Symbol	Condition	Total Current (mA)	LED Consumption (mA)	Total Power Consumption w/o LED (mW)
P_{LDPS}	Link Down, Power Saving Mode	3.0	0	9.9
P_{PWD}	Power Down Mode	2.5	0	8.25
P_{1000F}	1000BASE Full Duplex	119	2.7	392.7
P_{1000F}	1000BASE Idle	109	4	359.5
P_{100F}	100BASE Full Duplex	33.9	3.5	111.9
P_{100F}	100BASE Idle	32.6	4	107.6
P_{10F}	10BASE-Te Full Duplex	31.5	1	104.0
P_{10IDLE}	10BASE-Te Idle	9.4	1.5	31.0
802.3az Enabled				
P_{LPI}	1000M Idle	20.0	4.0	66.0
P_{LPI}	100M Idle	14.7	4.0	48.5
Atheros Proprietary Green Ethos®Power Savigns Per Cable Length				
P_{1000F} 20m	1000BASE Full Duplex 20m cable	92.0	2.7	303.6
P_{1000F} 20m	1000BASE Idle 20m cable	85.0	4	280.5
P_{1000F} 100m	1000BASE Full Duplex 100m cable	119.0	2.7	392.7
P_{1000F} 100m	1000BASE Idle 100m cable	109	4	359.7
P_{1000F} 140m	1000BASE Full Duplex 140m cable	137.0	2.7	452.1
P_{1000F} 140m	1000BASE Idle 140m cable	128.0	4	422.4

NOTE: power consumption test results are based on Atheros demo board.

3.8 Power-on Sequence, Reset and Clock

3.8.1 Power-on Sequence

The AR8035 only needs a single 3.3V power supply input. The 1.1V core and 2.5V, 1.8V/1.5V voltages are generated by AR8035's internal regulators. So the AR8035's power-on sequence to establish the power rails stability is met internally.

3.8.2 Reset and Clock Timing

The AR8035 hardware reset needs the clock to take effect. Input clock including the crystal and external input clock should be stable for at least 1ms before RESET can be deasserted. For chip reliability, an external clock must be input after the power-on sequence.

Figure 3-3 shows the Reset Timing diagram.

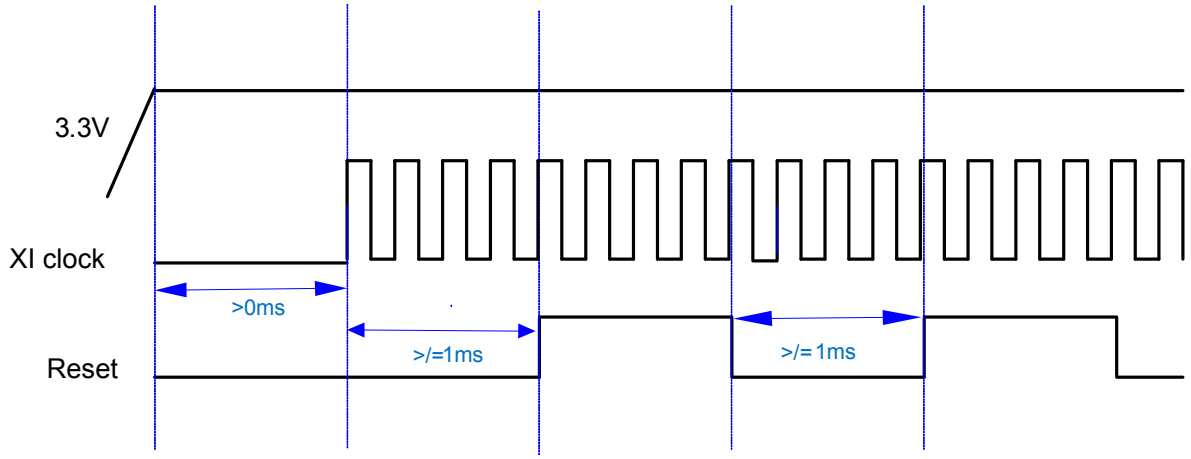


Figure 3-3. **Reset Timing Diagram**

When using crystal, the clock is generated internally after power is stable. For a reliable power on reset, suggest to keep asserting the reset low long enough (10ms) to ensure the clock is stable and clock-to-reset 1ms requirement is satisfied.

4. Register Descriptions

Table 4-1 shows the reset types used in this document.

Table 4-1. **Reset Types**

Type	Description
LH	Register field with latching high function. If status is high, then the register is set to one and remains set until a read operation is performed through the management interface or a reset occurs.
LL	Register field with latching low function. If status is low, then the register is cleared to a zero and remains cleared until a read operation is performed through the management interface or a reset occurs.

Table 4-1. **Reset Types**

Type	Description
Retain	Value written to a register field takes effect without a software reset.
SC	Self-Clear. Writing a one to this register causes the desired function to execute immediately, and the register field clears to zero when the function is complete.
Update	The value written to the register field does not take effect until a software reset is executed. The value can still be read after it is written.

4.1 Register Summary

Table 4-2 summarizes the registers for the AR8035.

Table 4-2. **Register Summary**

Offset	Register
0x00	Control
0x01	Status
0x02	PHY identifier [18:3]
0x03	PHY identifier [19:24]
0x04	Auto-negotiation advertisement
0x05	Link partner ability (base page)
0x06	Auto-negotiation expansion
0x07	Next page transmit
0x08	Link partner next page
0x09	1000 Base-T control
0x0A	1000 Base-T status
0x0B	Reserved
0x0C	Reserved
0x0D	MMD Access Control
0x0E	MMD Access Control Data
0x0F	Extended status
0x10	Function control
0x11	PHY-specific status
0x12	Interrupt enable
0x13	Interrupt status
0x14	Smart Speed
0x15	Reserved

Table 4-2. **Register Summary**

Offset	Register
0x16	Cable defect tester control
0x17	Reserved
0x18	LED control
0x19	Reserved
0x1A	Reserved
0x1B	Reserved
0x1C	Cable defect tester status
0x1D	Debug port address offset
0x1E	Debug port data
0x1F	Reserved

4.1.1 Control

Offset: 0x00
Mode: Read/Write
Hardware Reset: 0x3100
Software Reset: See field descriptions

Bit	Name	SW Reset	Description	
15	RESET	SC	PHY software reset	
			0	Normal operation
			1	PHY reset Writing a 1 to this bit causes immediate PHY reset. Once the operation is done, this bit clears to 0 automatically.
14	LOOPBACK	0	When loopback is active, the transmitter data on TXD loops back to RXD internally. The link breaks when loopback is enabled.	
			0	Disable loopback
			1	Enable loopback
13	SPEED_SELECTION (LSB)	Retain	Force_speed = {register 0.6, this bit}: 2'b00 = 10Mbps 2'b01 = 100Mbps 2'b10 = 1000Mbps 2'b11 = Reserved	
12	AUTO_ NEGOTIATION	Retain		
			0	Disable auto-negotiation process
			1	Enable auto-negotiation process
11	POWER_DOWN	0	When the port is switched from power down to normal operation, software reset and restart Auto-Negotiation are performed even when bit Reset (0.15)and Restart Auto-Negotiation (0.9) are not set by the user. IEEE power down shuts down the chip except for the MAC interface if 16.3 is set to 1. If 16.3 is set to 0, then the MAC interface also shuts down. Power-down has no effect on the 125clk output if 16.4 is set to 0.	
			0	Normal operation
			1	Power-down

Bit	Name	SW Reset	Description	
10	ISOLATE	0	The RGMII/RMIIoutput pins are tri-statedwhen thei bit is set to 1. The RGMII/RMII inputs are ignored. 1 = Isolate 0 = Normal operation	
9	RESTART_AUTO_ NEGOTIATION	SC	Auto-Negotiation automatically restarts after hardware or software reset regardless of whether or not this bit is set.	
			0	Normal operation
			1	Restart auto-negotiation process
8	DUPLEX MODE	Retain	.	
			0	Half-duplex
			1	Full-duplex
7	COLLISION TEST	0		
			0	Disable COL signal test
			1	Enable COL signal test
6	SPEED SELECTION (MSB)	Retain	See description in bit ["13"]	
5:0	RES	00000	Reserved. Always set to 00000.	

4.1.2 Status

Offset: 0x01
Mode: Read-Only
Hardware Reset: 0x7949
Software Reset: See field descriptions

Bit	Name	SW Reset	Description	
15	100BASE-T4	0	100 BASE-T4 This protocol is not available	
			0	PHY not able to perform 100 BASE-T4
14	100BASE-X FULL-DUPLEX	1	Capable of 100-Tx Full Duplex operation	
13	100BASE-X HALF-DUPLEX	1	Capable of 100-Tx Half Duplex operation	
12	10 MBPS FULL-DUPLEX	1	Capable of 10 BASE-T full duplex operation	
11	10 MBS HALF-DUPLEX	1	Capable of 10 BASE-T half duplex operation	
10	100BASE-T2 FULL-DUPLEX	0	Not able to perform 100 BASE-T2	
9	100BASE-T2 HALF-DUPLEX	0	Not able to perform 100 BASE-T2	
8	EXTENDED STATUS	1	Extended status information in the register "Extended Status" on page 43	
7	RESERVED	0	Always 0	
6	MF PREAMBLE SUPPRESSION	1	PHY accepts management frames with preamble suppressed	
5	AUTO-NEGOTIATION COMPLETE	0	0	Auto negotiation process not complete
			1	Auto negotiation process complete
4	REMOTE FAULT	0	This bit clears after read "SC".	
			0	Remote fault condition not detected.
			1	Remote fault condition detected
3	AUTO-NEGOTIATION ABILITY	1	PHY able to perform auto negotiation	
2	LINK STATUS	0	Indicates whether the link was lost since the last read. For the current link status, read LINK_REAL_TIME (bit [10]) of the register "PHY-Specific Status" on page 44. Latching low function.	
			0	Link is down
			1	Link is up
1	JABBER DETECT	0	This bit clears after read "SC".	
			0	Jabber condition not detected
			1	Jabber condition detected
0	EXTENDED CAPABILITY	1	Extended register capabilities	

4.1.3 PHY Identifier [18:3]

Offset: 0x02
Mode: Read-Only
Hardware Reset: 0x004D
Software Reset: 0x004D

Bit	Name	Description
15:0	Unique Identifier Bit	Organizationally unique identifier bits [18:3]. Always 16'h004D

4.1.4 PHY Identifier [19:24]

Offset: 0x03
Mode: Read-Only
Hardware Reset: 0xD072
Software Reset: 0xD072

Bit	Name	Description
15:0	OUI LSB Model Revision	Organizationally unique identifier bits [19:24]. Always 16'hD072

4.1.5 Auto-Negotiation Advertisement

Offset: 0x04
Mode: Read/Write
Hardware Reset: 0x1DE1
Software Reset: See field descriptions

Bit	Name	SW Reset	Description	
15	NEXT_PAGE	Retain	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down If 1000BASE-T is advertised then the required next pages are automatically transmitted. Register 4.15 should be set to 0 if no additional next pages are needed.	
			0	Not advertised
			1	Advertise
14	ACK	0	Must be set to 0	
13	REMOTE FAULT	Retain	Write a 1 to set remote fault	
12	xnp_able	1	Extended next page enable control bi: 1 = Local device supports transmission of extended next pages; 0 = Local device does not support transmission of extended next pages.	
11	ASYMMETRIC PAUSE	Retain	Upon hardware reset , this bit depends on ASYM_PAUSE_PAD. The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down 1 = Asymmetric Pause 0 = No asymmetric Pause	

Bit	Name	SW Reset	Description
10	PAUSE	Retain	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down 1 = MAC PAUSE implemented 0 = MAC PAUSE not implemented
9	100BASE-T4	0	Not able to perform 100 BASE-T4
8	100BASE-TX FULL DUPLEX	Retain	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down 1 = Advertise 0 = Not advertised
7	100BASE-TX HALF DUPLEX	Retain	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down 1 = Advertise 0 = Not advertised
6	10BASE-TX FULL DUPLEX	Retain	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down 1 = Advertise 0 = Not advertised
5	10BASE-TX HALF DUPLEX	Retain	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down 1 = Advertise 0 = Not advertised
4:0	SELECTOR FIELD	00001	Selector field mode 00001 802.3

4.1.6 Link Partner Ability (Base Page)

Offset: 0x05
Mode: Read-Only
Hardware Reset: 0
Software Reset: 0

Bit	Name	Description	
15	NEXT PAGE	Received code word bit [15]	
		0	Link partner not capable of next page
		1	Link partner capable of next page
14	ACK	Acknowledge; received code word bit [14]	
		0	Link partner does not have next page ability
		1	Link partner received link code word
13	REMOTE FAULT	Received code word bit [13]	
		0	Link partner has not detected remote fault
		1	Link partner detected remote fault
12	RESERVED	Technology Ability Field Received Code Word Bit [12]	
11	ASYMMETRIC PAUSE	Received code word bit [11]	
		0	Link partner does not request asymmetric pause
		1	Link partner requests asymmetric pause
10	PAUSE	Received code word bit [10]	
		0	Link partner is not capable of pause operation
		1	Link partner is capable of pause operation
9	100BASE-T4	Received code word bit [9]	
		0	Link partner is not 100 BASE-T4 capable
		1	Link partner is 100 BASE-T4 capable
8	100BASE-TX FULL DUPLEX	Received code word bit [8]	
		0	Link partner is not 100 BASE-TX full-duplex capable
		1	Link partner is 100 BASE-TX full-duplex capable
7	100BASE-TX HALF DUPLEX	Received code word bit [7]	
		0	Link partner is not 100 BASE-TX half-duplex capable
		1	Link partner is 100 BASE-TX half-duplex capable
6	10BASE-TX FULL DUPLEX	Received code word bit [6]	
		0	Link partner is not 10 BASE-T full-duplex capable
		1	Link partner is 10 BASE-T full-duplex capable
5	10BASE-TX HALF DUPLEX	Received code word bit [5]	
		0	Link partner is not 10 BASE-T half-duplex capable
		1	Link partner is 10 BASE-T half-duplex capable
4:0	SELECTOR FIELD	Received code word bit [4:0]	

4.1.7 Auto-Negotiation Expansion

Offset: 0x06
Mode: Read-Only
Hardware Reset: 0x0004
Software Reset: Decided by the PHY inner state

Bit	Name	Description	
15:5	RES	Reserved. Must be set to 0.	
4	PARALLEL DETECTION FAULT	Software resets this bit to 0; clear after read	
		0	No fault has been detected
		1	A fault has been detected
3	LINK PARTNER NEXT PAGE ABLE	Software resets this bit to 0; clear after read	
		0	Link partner is not next page capable
		1	Link partner is next page capable
2	LOCAL NEXT PAGE ABLE		
		0	Local device is not next page capable
		1	Local device is next page able
1	PAGE RECEIVED	On software reset, this bit value is reserved; LH; cleared after a read.	
		0	No new page has been received
		1	A new page has been received
0	LINK PARTNER AUTO-NEGOTIATION ABLE	Software reset to 0.	
		0	Link partner is not auto-negotiation capable
		1	Link partner is auto-negotiation capable

4.1.8 Next Page Transmit

Offset: 0x07
Mode: Read/Write
Reset: See field descriptions

Bit	Name	Reset	Description
15	NEXT PAGE	0	Transmit code word bit [15]
14	RES	0	Transmit code word bit [14]
13	MESSAGE PAGE MODE	1	Transmit code word bit [13]
12	ACK2	0	Transmit code word bit [12]
11	TOGGLE	1	Transmit code word bit [11]
10:0	MESSAGE/ UNFORMATTED FIELD	0x001	Transmit code word bits [10:0]

4.1.9 Link Partner Next Page

Offset: 0x08
Mode: Read-Only
Hardware Reset: 0
Software Reset: 0

Bit	Name	Description
15	NEXT PAGE	Receive code word bit [15]
14	ACK	Receive code word bit [14]
13	MESSAGE PAGE MODE	Receive code word bit [13]
12	ACK2	Receive code word bit [12]
11	TOGGLE	Receive code word bit [11]
10:0	MESSAGE/ UNFORMATTED FIELD	Receive code word bits [10:0]

4.1.10 1000 BASE-T Control

Offset: 0x09
Mode: Read/Write
Hardware Reset: 0x0200
Software Reset: See field descriptions

Bit	Name	SW Reset	Description	
15:13	TEST MODE	Retain	Hardware reset or software reset (see RESET (bit [15]) of the register "Function Control" on page 43) should be issued to ensure normal operation after exiting the test mode.	
			000	Normal Mode
			001	Test mode 1: Transmit waveform test
			010	Test mode 2: Transmit jitter test (MASTER mode)
			011	Test mode 3: Transmit jitter test (SLAVE mode)
			100	Test mode 4: Transmit distortion test
			101, 110, 111	Reserved
12	MASTER/SLAVE MANUAL CONFIGURATION ENABLE	Retain	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down 1 = Manual MASTER/SLAVE configuration 0 = Automatic MASTER/SLAVE configuration	
			0	Automatic MASTER/SLAVE configuration
			1	Manual MASTER/SLAVE configuration

Bit	Name	SW Reset	Description	
11	MASTER/SLAVE CONFIGURATION	Retain	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down Register 9.11 is ignored if register 9.12 is equal to 0. 1 = Manual configure as MASTER 0 = Manual configure as SLAVE	
			0	Manual configure as SLAVE
			1	Manual configure as MASTER
10	PORT TYPE	Retain	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down Register 9.10 is ignored if register 9.12 is equal to 1.	
			0	Prefer single port device (SLAVE)
			1	Prefer multi-port device (MASTER)
9	1000BASE-T FULL DUPLEX	Retain	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down 1 = Advertise 0 = Not advertised When giga_dis_qual(register20.8) is high, this bit is forced to be low.	
8	1000BASE-T HALF-DUPLEX	Retain	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down 1 = Advertise 0 = Not advertised Note: the default setting is no 1000 baset/half duplex advertised When giga_dis_qual(register20.8) is high, this bit is forced to be low.	
7:0	RES	0	Reserved	

4.1.11 1000 BASE-T Status

Offset: 0x0A
Mode: Read-Only
Hardware Reset: 0
Software Reset: 0

Note: Contents of this register clear after a read operation has occurred.

Bit	Name	Description	
15	MASTER/SLAVE CONFIGURATION FAULT	This register bit will clear on read	
		0	No fault detected
		1	Master/slave configuration fault detected
14	MASTER/SLAVE CONFIGURATION RESOLUTION	This register bit is not valid until PAGE_RECEIVED (bit [1]) of the register "Auto-Negotiation Expansion" on page 38 is 1	
		0	Local PHY configuration resolved to Slave
		1	Local PHY configuration resolved to Master
13	LOCAL RECEIVER STATUS	0	Local Receiver Not OK
		1	Local Receiver OK
12	REMOTE RECEIVER STATUS	0	Remote Receiver Not OK
		1	Remote Receiver OK
11	LINK PARTNER 1000BASE-T FULL DUPLEX CAPABILITY	This register bit is not valid until PAGE_RECEIVED (bit [1]) of the register "Auto-Negotiation Expansion" on page 38 is 1	
		0	Link Partner is not capable of 1000 BASE-T half duplex
		1	Link Partner is capable of 1000 BASE-T half duplex
10	LINK PARTNER 1000BASE-T HALF DUPLEX CAPABILITY	This register bit is not valid until PAGE_RECEIVED (bit [1]) of the register "Auto-Negotiation Expansion" on page 38 is 1	
		0	Link Partner is not capable of 1000 BASE-T full duplex
		1	Link Partner is capable of 1000 BASE-T full duplex
9:8	RES	Reserved.	
7:0	IDLE ERROR COUNT	Reports the idle error count since the last time this register was read. The counter stops at 11111111 and does not roll over. These bits clear on a read.	

4.1.12 MMD Access Address Register

Offset: 0x0E
Mode: Read-Only
Hardware Reset: 0
Software Reset: 0

Bit	Name	Type		Description
15:0	Address Data	Mode	R/W	If register13.15:14=00, MMD DEVAD's address register. Otherwise, MMD DEVAD's data register as indicated by the contents of its address register
		HW Rst	00	
		SW Rst	Retain	

4.1.13 MMD Access Control Register

Offset: 0x0D
Mode: Read-Only

NOTE: Contents of this register clear after a read operation has occurred.

Bit	Name	Type		Description
15:14	Function	Mode	R/W	00=address 01=data,no post increment 10=data,post increment on reads and writes 11=data,post increment on writes only;
		HW Rst	00	
		SW Rst	Retain	
13:5	Reserved	Mode	RO	
		HW Rst	0	
		SW Rst	0	
4:0	DEVAD	Mode	R/W	Device address
		HW Rst	00	
		SW Rst	Update	

4.1.14 Extended Status

Offset: 0x0F
Mode: Read-Only
Hardware Reset: 0x2000
Software Reset: 0

Bit	Name	Description
15	1000BASE-X FULL DUPLEX	PHY not able to perform 1000 BASE-X Full Duplex
14	1000BASE-X HALF DUPLEX	PHY not able to perform 1000 BASE-X Half Duplex
13	1000BASE-T FULL-DUPLEX	PHY able to perform 1000 BASE-T Full Duplex
12	1000BASE-T HALF-DUPLEX	PHY not able to perform 1000 BASE-T Half Duplex
11:0	RES	Reserved

4.1.15 Function Control

Offset: 0x10
Mode: Read/Write
Hardware Reset: 0x0862
Software Reset: See field descriptions

Bit	Name	SW Reset	Description	
15:12	RESERVED			
11	ASSERT_CRS_ON_ TRANSMIT	Retain	This bit has effect in 10BT half-duplex mode and 100BT mode:	
			0	Never assert on transmit
			1	Assert on transmit
10	RESERVED			
9:7	RESERVED			
6:5	MDI_CROSSOVER_ MODE	Update	Changes to these bits are disruptive to the normal operation; therefore any changes to this register must be followed by a software reset to take effect.	
			00	Manual MDI configuration
			01	Manual MDIX configuration
			10	Reserved
			11	Enable automatic crossover for all modes

Bit	Name	SW Reset	Description	
4:3	RES	0	Reserved	
2	SQE_TEST	Retain	SQE Test is automatically disabled in full-duplex mode regardless of the state of this bit	
			0	SQE test disabled
			1	SQE test enabled
1	POLARITY_ REVERSAL	Retain	If polarity is disabled, then the polarity is forced to be normal in 10 BASE-T	
			0	Polarity reversal enabled
			1	Polarity reversal disabled
0	DISABLE_JABBER	Retain	0	Enable jabber function
			1	Disable jabber function

4.1.16 PHY-Specific Status

Offset: 0x11
Mode: Read-Only
Hardware Reset: 0x0010
Software Reset: 0

Bit	Name	Description	
15:14	SPEED	Valid only after resolved bit [11] of this register = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled.	
		00	10 Mbps
		01	100 Mbps
		10	1000 Mbps
		11	Reserved
13	DUPLEX	Valid only after resolved bit [11] of this register = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled.	
		0	Half-duplex
		1	Full-duplex
12	PAGE_RECEIVED (real-time)	0	Page not received
		1	Page received
11	SPEED_DUPLEX_ RESOLVED	When Auto-Negotiation is not enabled, this bit = 1 for force speed	
		0	Not resolved
		1	Resolved
10	LINK (real-time)	0	Link down
		1	Link up
9:7	RES	Reserved. Always set to 0.	
6	MDI_CROSSOVER_ STATUS	Valid only after resolved bit [11] of this register = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. This bit is 0 or 1 depending on what is written to bits [6:5] of the register "Function Control" on page 43 in manual configuration mode. "Function Control" bits [6:5] are updated with software reset.	
		0	MDI
		1	MDIX
5	SMARTSPEED_ DOWNGRADE	0	Smartspeed downgrade does not occur
		1	Smartspeed downgrade occurs

Bit	Name	Description	
4	RESERVED		
3	TRANSMIT_PAUSE_ENABLED	Valid only after resolved bit [11] of this register = 1. The resolved bit is set when auto-negotiation is completed or disabled. A reflection of the MAC pause resolution.	
		0	Transmit pause disabled
		1	Transmit pause enabled
2	RECEIVE_ PAUSE_ENABLED	A reflection of the MAC pause resolution. This status bit is valid only after resolved bit [11] of this register = 1. The resolved bit is set when auto-negotiation is completed or disabled.	
		0	Receive pause disabled
		1	Receive pause enabled
1	POLARITY (real-time)	0	Normal
		1	Reversed
0	JABBER (real-time)	0	No jabber
		1	Jabber

4.1.17 Interrupt Enable

Offset: 0x12
Mode: Read/Write
Hardware Reset: 0
Software Reset: See field descriptions

Bit	Name	SW Reset	Description	
15	Auto-Negotiation Error Interrupt Enable	Retain	0	Interrupt disable
			1	Interrupt enable
14	Speed Changed Interrupt Enable	Retain	0	Interrupt disable
			1	Interrupt enable
13	Duplex Changed Interrupt Enable	Retain	0	Interrupt disable
			1	Interrupt enable
12	Page Received Interrupt Enable	Retain	0	Interrupt disable
			1	Interrupt enable
11	Link fail interrupt	Retain	0	Interrupt disable
			1	Interrupt enable
10	Link success interrupt	Retain	0	Interrupt disable
			1	Interrupt enable
9	Reserved			
8	Reserved			
7	Reserved			

Bit	Name	SW Reset	Description	
6	Reserved			
5	Wirespeed-downgrade Interrupt	Retain	0	Interrupt disable
			1	Interrupt enable
4	Reserved			
3:2	RES	0	Reserved. Always set to 00.	
1	Polarity Changed Interrupt Enable	Retain	0	Interrupt disable
			1	Interrupt enable
0	Wake on LAN interrupt enable	0	0	Interrupt disable
			1	Interrupt enable

4.1.18 Interrupt Status

Offset: 0x13
Mode: Read-Only
Hardware Reset: 0

Note: All bits clear on read.

Bit	Name	Description	
15	AUTO _NEGOTIATION_ ERROR	An error is said to occur if MASTER/SLAVE does not resolve, parallel detect fault, no common HCD, or link does not come up after negotiation is completed.	
		0	No Auto-Negotiation Error
		1	Auto-Negotiation Error
14	SPEED_CHANGED	0	Speed not changed
		1	Speed changed
13	DUPLEX_ CHANGED	0	Duplex not changed
		1	Duplex changed
12	PAGE_RECEIVED	0	Page not received
		1	Page received
11	LINK_FAIL _INTERUPT	0	1 = Link down happened.
		1	0 = Link down not happened
10	LINK_SUCESS_INT ERUPT	0	1 = Link up happened.
		1	0 = Link up not happened
9:6	RESERVED	0	No symbol error
		1	Symbol error
5	WIRESPEED_DOW NGRADE _INTERRUPT	0	No Smartspeed interrupt detected
		1	Smartspeed interrupt detected

Bit	Name	Description	
4:2	RESERVED	0	
		1	
1	POLARITY_ CHANGED	0	Polarity not changed
		1	Polarity changed
0	INT_WOL_PTP	0	No Wake-on-LAN packet is received
		1	Wake-on-LAN packet is received

4.1.19 Smart Speed

Offset: 0x14
Mode: Read/Write
Hardware Reset: 0x82C
Software Reset: See field descriptions

Bit	Name	Reset	Description	
15:6	RES	0	Reserved. Must be set to 00001000.	
5	SMARTSPEED_EN	1	The default value is one; if this bit is set to one and cable inhibits completion of the training phase, then after a few failed attempts, the device automatically adjusts the highest ability to the next lower speed: from 1000 to 100 to 10.	
4:2	SMARTSPEED_RETRY_LIMIT	011	The default value is three; if set to three, then the device attempts five times before adjusting; the number of attempts can be changed through setting these bits.	
			000	2 retries
			001	3 retries
			010	4 retries
			011	5 retries (default)
			100	6 retries
			101	7 retries
			110	8 retries
			111	9 retries
1	BYPASS_SMARTSPEED_TIMER	0	0	The stable link condition is determined 2.5 seconds after the link is established (default)
			1	The stable link condition is determined as soon as the link is established
0	RESERVED	0	Reserved. Must be set to 0.	

4.1.20 Cable Diagnostic Tester Control

Offset: 0x16
Mode: Read/Write
Hardware Reset: 04E8
Software Reset: Retain

Bit	Name	Description	
15:10	RES	Reserved	
9:8	MDI_PAIR_ SELECT	Cable Diagnostic Tester (CDT) control registers Use the cable defect tester control registers to select which MDI pair is shown in the register "Cable Defect Tester Status" on page 49.	
		00	MDI[0] pair
		01	MDI[1] pair
		10	MDI[2] pair
		11	MDI[3] pair
7:1	RES	Reserved	
0	ENABLE_TEST	When set, hardware automatically disable this bit when CDT is done	
		0	Disable CDT Test
		1	Enable CDT Test

4.1.21 LED Control

Offset: 0x018

Bit	Name	Type		Description
15	Reserved	Mode	R/W	
		HW Rst.	0	
		SW Rst	Retain	
14:12	Led on time	Mode	R/W	000 = 5 ms 001 = 10ms 010 = 21 ms 011 = 42ms 100 = 84 ms 101 = 168ms 110 to 111 = 42ms
		HW Rst.	011	
		SW Rst	Retain	
11	Reserved	Mode	R/W	Always 0
		HW Rst.	0	
		SW Rst	Retain	
10:8	Led off time	Mode	R/W	000 = 21 ms 001 = 42 ms 010 = 84 ms 011 =168 ms 100 =330 ms 101 = 670 ms 110 to 111 = 168ms
		HW Rst.	010	
		SW Rst	Retain	
7:0	Reserved	Mode	R/W	
		HW Rst.	0	
		SW Rst	Retain	

4.1.22 Cable Defect Tester Status

Offset: 0x1C
Mode: Read-Only
Hardware Reset: 0200
Software Reset: Retain

Bit	Name	Description	
15:10	RES	Reserved	
9:8	STATUS	The content of this register applies to the cable pair selected in the register "Cable Diagnostic Tester Control" on page 47.	
		00	Valid test, normal cable (no short or open in cable)
		01	Valid test, short in cable (Impedance < 33 Ω)
		10	Valid test, open in cable (Impedance > 333 Ω)
		11	Test fail
7:0	DELTA_TIME	Delta time to indicate distance	

4.1.23 Debug Port Address Offset

Offset: 0x1D
Mode: Read/Write
Hardware Reset: 0
Software Reset: 0

Bit	Name	Description
15:6	RES	Reserved
5:0	ADDRESS_OFFSET	Address index to access the debug registers

4.1.24 Debug Port Data

Offset: 0x1E
Mode: Read/Write
Hardware Reset: 0x82EE
Software Reset: 0x82EE

Bit	Name	Description
15:0	DATA	Data contents of the debug registers as addressed by the "Debug Port Address Offset" register

4.2 Debug Register Descriptions

Table 4-3 summarizes the debug registers for the AR8035.

Table 4-3.

Offset	Register
0x00	Debug register 0
0x05	Debug register 5
0x10	100 BASE-TX test mode select
0x11	Debug register 11
0x12	Test configuration for 10 BASE-T

4.2.1 RGMII RX Clock Delay Control

Offset: 0x00

Bit	Name	Type		Description
15	Sel_clk125m_dsp	Mode	R/W	Control bit for rgmii interface rx clock delay: 1 = rgmii rx clock delay enable 0 = rgmii rx clock delay disable
		HW Rst.	1	
		SW Rst.	1	
14:0	Reserved	Mode	RO	
		HW Rst.	2EE	
		SW Rst.	2EE	

4.2.2 RGMII TX Clock Delay Control

Offset: 0x05

Bit	Name	Type		Description
15:9	Reserved	Mode	R/W	
		HW Rst.	1	
		SW Rst.	1	
8	rgmii_tx_clk_dly	Mode	R/W	Rgmii tx clock delay control bit: 1 = rgmii tx clock delay enable 0 = rgmii tx clock delay disable.
		HW Rst.	0	
		SW Rst.	Retain	
7:0	Reserved	Mode	RO	
		HW Rst.	2EE	
		SW Rst.	2EE	

4.2.3 Hibernation Control and RGMII GTX Clock Delay Register

Offset: 0x0B

Bit	Name	Type		Description
15	Ps_hib_en	Mode	R/W	Power hibernate control bit; 1: hibernate enable 0: hibernate disable
		HW Rst.	1	
		SW Rst.	Retain	
14:13	Reseved	Mode	RO	
		HW Rst.	01	
		SW Rst.	01	
12	Hib_pulse_sw	Mode	R/W	1: when hibernate, PHY sends NLP pulse and detects signal from cables. 0: when hibernate, PHY doesn't send NLP pulse ,just detects signal from cables.
		HW Rst.	1	
		SW Rst.	Retain	
11:7	Reseved	Mode	RO	
		HW Rst.	11000	
		SW Rst.	11000	
6:5	Gtx_dly_val	Mode	R/W	Select the delay of gtx_clk. 00:0.25ns 01:1.3ns 10:2.4ns 11:3.4ns
		HW Rst.	2'b10	
		SW Rst.	Retain	
4:0	Reseved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	

4.2.4 100BASE-TX Test Mode Select

Offset: 0x10

Bit	Name	Type		Description
15:8	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	
7	Jitter_test	Mode	R/W	100BT jitter test
		HW Rst.	0	
		SW Rst.	Retain	
6	Os_test	Mode	RO	100BT over shoot test
		HW Rst.	0	
		SW Rst.	0	
5	Dcd_test	Mode	R/W	100BT DCD test
		HW Rst.	0	
		SW Rst.	Retain	
4:0	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	

4.2.5 1000BT external loopback configure

Offset: 0x11

Bit	Name	Type		Description
15:1	Reserved	Mode	RO	
		HW Rst.	3AA9	
		SW Rst.	3AA9	
0	Ext_lpbk	Mode	RO	1: enable the PHY's external loopback, namely channel 0<-> channel 1, channel 2 <-> channel 3.
		HW Rst.	0	
		SW Rst.	0	

4.2.6 Rgmii_mode; Test configuration for 10BT

Offset: 0x12

Bit	Name	Type		Description
15:6	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
5	Test_mode[2]	Mode	RO	The bit2 of test_mode
		HW Rst.	0	
		SW Rst.	0	
4	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
3	Reserved	Mode	RO	
		HW Rst.	1	
		SW Rst.	1	
2	Reserved	Mode	RO	
		HW Rst.	1	
		SW Rst.	1	
1:0	Test_mode[1:0]	Mode	RO	[001]: packet with all ones, 10MHz sine wave, For harmonic test. [010]: pseudo random, for TP_IDLE/Jitter/Differential Voltage test. [011]: normal link pulse only, [100]: 5MHz sin wave. Others: normal mode.
		HW Rst.	0	
		SW Rst.	0	

4.2.7 MMD3 (MDIO Manageable Device Address 3 for PCS)

Offset	Register	Description	
0	PCS Control Register		
1	PCS Status Register		

Offset	Register	Description	
20	EEE capability		
22	EEE wake error counter		

4.2.8 MMD7 (MDIO Manageable Device Address 7 for Auto-Negotiation)

Offset	Register	Description	
0	AN control		
1	AN status		
22	AN XNP transmit		
23	AN XNP transmit1		
24	AN XNP transmit2		
25	AN XNP ability		
26	AN XNP ability1		
27	AN XNP ability2		
60	EEE advertisement		
61	EEE LP advertisement		
32768	EEE ability auto-negotiation result		

4.3 MDIO Interface Register

4.3.1 PCS Control 1

Device Address = 3

Offset: 0x0 (Hex)

Bit	Name			Description
15	Pcs_rst	Mode	R/W	Reset bit, self clear. When write this bit 1 : 1, reset the registers(not vender specific) in MMD3/ MMD7. 2, cause software reset in mii register0 bit15.
		HW Rst.	0	
		SW Rst.	0	
14:11	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	
10	Clock_stoppable	Mode	R/W	Not implemented.
		HW Rst.	0	
		SW Rst.	Retain	
9.0	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	

4.3.2 PCS Status 1

Device Address = 3

Offset: 0x1 (Hex)

Bit	Name			Description
15:12	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	
11	Tx lp idle received	Mode	R/W	When read as 1, it indicates that the transmit PCS has received low power idle signaling one or more times since the register was last read. Latch High.
		HW Rst.	0	
		SW Rst.	0	
10	Rx lp idle received	Mode	R/W	When read as 1, it indicates that the recive PCS has received low power idle signaling one or more times since the register was last read. Lach High.
		HW Rst.	0	
		SW Rst.	0	
9	Tx lp idle indication	Mode	R/W	When read as 1, it indicates that the transmit PCS is currently receiving low power idle signals.
		HW Rst.	0	
		SW Rst.	0	
8	Rx lp idle indication	Mode	R/W	When read as 1, it indicates that the receive PCS is currently receiving low power idle signals.
		HW Rst.	0	
		SW Rst.	0	
7:0	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	

4.3.3 EEE Capability

Device Address = 3

Offset: 0x14 (Hex)

Bit	Name			Description
15:3	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	
2	1000BT EEE	Mode	RO	EEE is supported for 1000BASE-T.
		HW Rst.	1	
		SW Rst.	1	
1	100BT EEE	Mode	RO	EEE is supported for 100BASE-T.
		HW Rst.	1	
		SW Rst.	1	
0	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	

4.3.4 EEE Wake Error Counter

Device Address = 3

Offset: 0x16 (Hex)

Bit	Name			Description
15:	EEE wake error counter	Mode	RO	Count wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type. This counter is clear after read, and hold at all ones in the case of overflow.
		HW Rst.	0	
		SW Rst.	0	

4.3.5 Wake-on-Lan loc_mac_addr_o

Device Address = 3

Offset: 0x804A (Hex)

Bit	Name			Description
15:0	Loc_mac_ Addr_o[47:32]	Mode	R/W	Bits [47:32] of local MAC address, used in Wake-on-Lan.
		HW Rst.	0	
		SW Rst.	Retain	

4.3.6 Wake-on-Lan loc_mac_addr_o

Device Address = 3

Offset: 0x804B (Hex)

Bit	Name			Description
15:0	Loc_mac_ Addr_o[31:16]	Mode	R/W	Bits [31:16] of local MAC address, used in Wake-on-Lan.
		HW Rst.	0	
		SW Rst.	Retain	

4.3.7 Wake-on-Lan loc_mac_addr_o

Device Address = 3

Offset: 0x804C (Hex)

Bit	Name			Description
15:0	Loc_mac_ Addr_o[15:0]	Mode	R/W	Bits [15:0] of local MAC address, used in Wake-on-Lan.
		HW Rst.	0	
		SW Rst.	Retain	

4.3.8 Rem_phy_lpkb

Device Address = 3

Offset: 0x805A (Hex)

Bit	Name			Description
15:1	Reserved	Mode	R/W	
		HW Rst.	0	
		SW Rst.	Retain	
0	Rem_phy_lpbk	Mode	R/W	Loopback received data packets to link partner
		HW Rst.	0	
		SW Rst.	Retain	

4.3.9 Smart_eee control1

Device Address = 3

Offset: 0x805B (Hex)

Bit	Name			Description
15:8	Lpi_wt	Mode	R/W	1000BT Tw timer. After timer done, buffered data will be send. LSB vs time : 1us Default value: 17us.
		HW Rst.	8'h11	
		SW Rst.	Retain	
7:0	Lpi_wt	Mode	R/W	100BT Tw timer. After timer done, buffered data will be send. LSB vs time : 1us Default value: 23us.
		HW Rst.	8'h17	
		SW Rst.	Retain	

4.3.10 Smart_eee control2

Device Address = 3

Offset: 0x805C (Hex)

Bit	Name			Description
15:0	Lpi_time[15:0]	Mode	R/W	Lpi_timer will count when no data for transmission. After lpi_timer done, PHY will enter LPI mode. LSB vs time : 163.84us Default value: 335.544ms.
		HW Rst.	16'h800	
		SW Rst.	Retain	

4.3.11 Smart_eee control3

Device Address = 3

Offset: 0x805D (Hex)

Bit	Name			Description
15:14	Reserved	Mode	R/W	
		HW Rst.	0	
		SW Rst.	0	
13:12	Lpi_tx_delay_sel	Mode	R/W	Select IPG length inserted between packets. It's for debug.
		HW Rst.	2'b01	
		SW Rst.	Retain	
11:9	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
8	Lpi_en	Mode	R/W	Enable smart EEE. 1 = enable, 0 = disable.
		HW Rst.	1'b01	
		SW Rst.	Retain	
7:0	lpi_timer[23:16]	Mode	R/W	Lpi_timer will count when no data for transmission. After lpi_timer done, PHY will enter LPI mode.
		HW Rst.	0	
		SW Rst.	Retain	

Device address = 7, address ofset = 0x8016 (Hex)

4:3	Select_clk125m	Mode	R/W	CLK_25M output clock select 00=25M 01=50M 10=62.5M 11=125M
		HW Rst.	00	
		SW Rst.	Retain	

Device Address = 7

Offset: 0x1 (Hex)

Bit	Name			Description
15:8	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	

Bit	Name			Description
7	Xnp_status	Mode	RO	1 = both Local device and link partner have indicated support for extended next page; 0 = extended next page shall not be used.
		HW Rst.	0	
		SW Rst.	0	
6:0	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	

4.3.12 AN status

Device Address = 7

Offset: 0x16 (Hex)

Bit	Name			Description
15:0	Xnp_22	Mode	R/W	A write to this register set mr_next_page_loaded.
		HW Rst.	15'h0	
		SW Rst.	Retain	

4.3.13 AN XNP transmit1

Device Address = 7

Offset: 0x17 (Hex)

Bit	Name			Description
15:0	Xnp_23	Mode	R/W	
		HW Rst.	15'h0	
		SW Rst.	Retain	

4.3.14 AN XNP transmit2

Device Address = 7

Offset: 0x18 (Hex)

Bit	Name			Description
15:0	Xnp_24	Mode	R/W	
		HW Rst.	15'h0	
		SW Rst.	Retain	

4.3.15 EEE advertisement

Device Address = 7

Offset: 0x3C (Hex)

Bit	Name			Description
15:3	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	
2	EEE_1000BT	Mode	R/W	If Local device supports EEE operation for 1000BT, and EEE operation is desired, this bit shall be set to 1.
		HW Rst.	1'b1	
		SW Rst.	Retain	
1	EEE_100BT	Mode	R/W	If Local device supports EEE operation for 100BT, and EEE operation is desired, this bit shall be set to 1.
		HW Rst.	1'b1	
		SW Rst.	Retain	
0	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	

4.3.16 EEE LP advertisement

Device Address = 7

Offset: 0x3D (Hex)

Bit	Name			Description
15:3	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	
2	EEE_1000BT	Mode	RO	1 = link partner supports EEE operation for 1000BT, and EEE operation is desired; 0 = link partner does not support EEE operation for 1000BT, or EEE operation is not desired.
		HW Rst.	0	
		SW Rst.	0	
1	EEE_100BT	Mode	RO	1 = link partner supports EEE operation for 100BT, and EEE operation is desired; 0 = link partner does not support EEE operation for 100BT, or EEE operation is not desired.
		HW Rst.	0	
		SW Rst.	0	
0	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	

5. Package Dimensions

The AR8035 is packaged in a 40 pin QFN. The body size is 5 mm x 5 mm. The package drawings and dimensions are provided in Figure 5-1 and the following table.

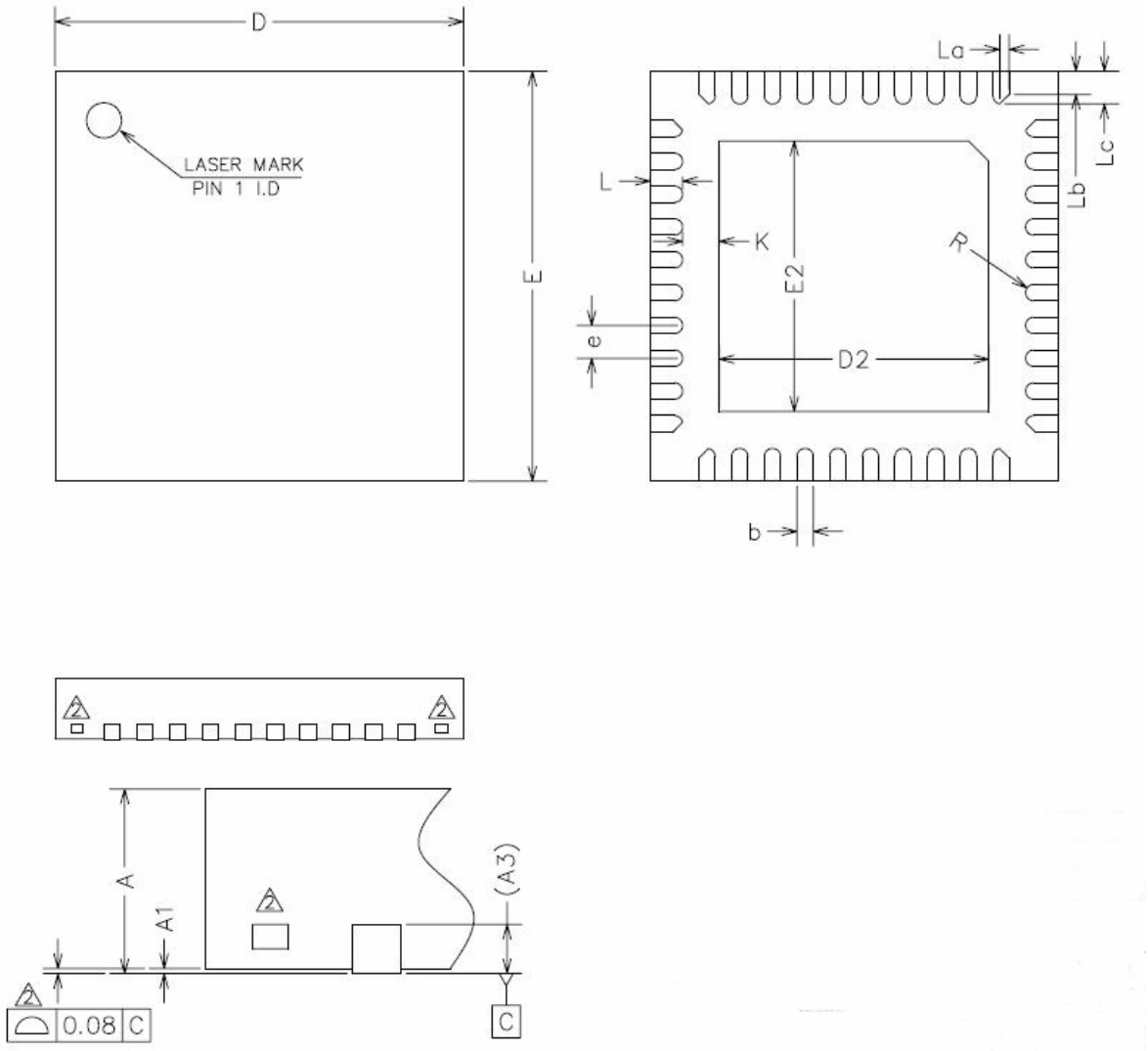


Figure 5-1. **Package Views**

Table 5-1. **Package Dimensions**

Dimension Label	Min	Nom	Max	Unit
A	0.70	0.75	0.80	mm
A1	0.00	0.02	0.05	mm
A3		0.20 REF		
b	0.15	0.20	0.25	mm
D	4.90	5.00	5.10	mm
E	4.90	5.00	5.10	mm
D2	3.15	3.30	3.50	mm
E2	3.15	3.30	3.50	mm
e	0.35	0.40	0.45	mm
K	0.20	--	--	mm
L	0.30	0.40	0.50	mm
R	0.09	--	--	mm
La	0.12	0.15	0.18	mm
Lb	0.23	0.26	0.29	mm
Lc	0.30	0.39	0.50	mm

Notes:
1. All Dimensions refer to JEDEC Standard MO-220 VHHE-1

6. Ordering Information

Table 6-1. **AR8035 Ordering Information**

Ordering Number	Version	Default Ordering Unit
AR8035-AL1A	Commercial	Tray pack
AR8035-AL1A-R	Commercial	Tape and reel
AR8035-AL1B-R	Industrial	Tape and reel

7. Top-side Marking

Table 7-1. **AR8035 Marking**

Ordering Number	Marking
AR8035-AL1A AR8035-AL1A-R	AR8035-A
AR8035-AL1B-R	8035-AL1B

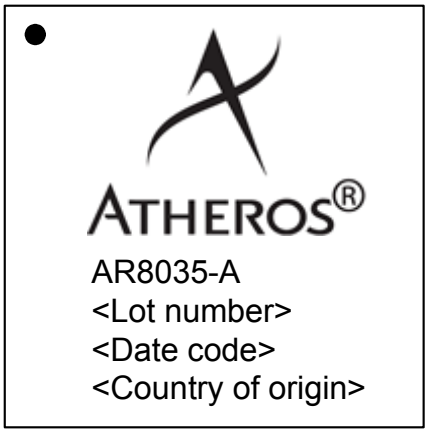


Figure 7-1. **AR8035 Top-Side Marking (Commercial)**

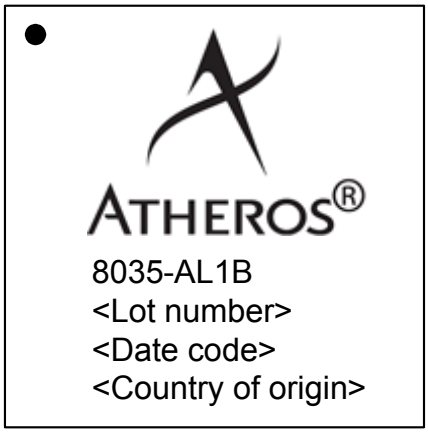


Figure 7-2. **AR8035 Top-Side Marking (Industrial)**

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