APW9105

6A, 18V, 600kHz Synchronous Step-Down Converter

Features

- **Input Voltage range : 4.5V to 18V.**
- **6A Output Current**
- **ANPEC System Phase Shift (ASP) function Reduces System Noise by Daisy Chaining Converter with Phase Shift**
- **Typical 0.6V ±1% Internal Reference Voltage.**
- **Optimized Upper and Lower MOSFETs R_{DS_on} for max Efficiency:**
  - **N-CH MOSFET: 40mΩ for High Side.**
  - **N-CH MOSFET: 20mΩ for Low Side.**
- **VDD Bypass Function allows for External 5V supply**
- **Mode Pin allows for Forced PWM or Automatic PSM/PWM mode**
- **Built in OVP, UVP, Current Limit and OTP.**
- **Low Cost TQFN3x2-14 package.**
- **Lead Free and Green Devices Available (RoHS Compliant).**
- **DyncBandwidth™ Technology**
- **SpeedTrans™ Technology**

Applications

- **Digital Subscriber Line**
- **Set-Top-Box**
- **DDR4, LPDDR4, LPDDR4X**
- **Passive Optical Network**
- **G.fast**
- **General DC to DC converter Applications**

General Description

The APW9105 is a high efficiency synchronous buck converter with integrated 40m/20mΩ of upper/lower power MOSFET and offers 6A continuous current capability.

This part is part of the family of converters with a proprietary **ANPEC System Phase Shift** (ASP) method that allows multiple converters to be daisy chained together while being able to synchronize to an external clock, allowing for a much reduced system noise performance. The ASP pin of the APW9105 can output a synchronized clock to the external clock with a slight phase delay to the next converter such that next converter will not turn on at the same time.

Another feature of this part is its ability to automatically optimize its BW (DyncBandwidth) to allow better dynamic response once it is synchronized to a higher external clock.

The APW9105 uses a peak current mode control scheme to regulate the output voltage. The internal switching frequency is set at 600kHz while the EN/SYNC pin supports external clock synchronization.

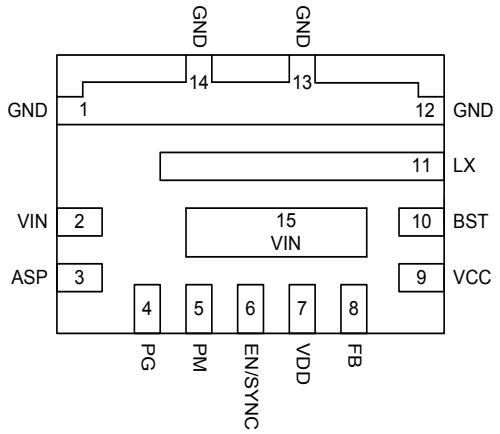
The APW9105 also equips a technique: SpeedTrans™, which allows improving transient response without complex external compensation circuits design.

VDD bypass pin allows for an external 5V supply to power the internal control circuitry thereby reducing overall system power consumption for better efficiency especially at light load conditions. And PM selection, It can improve the efficiency when the load is light.

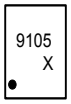
The APW9105 is also equipped with Power-on-reset, soft start, and complete protections, over-temperature, over-voltage, under-voltage and over-current of the converter

The APW9105 is offered in a TQFN3x2-14 package allowing small size while having an excellent thermal capability for power dissipation.

Pin Configuration (Top View)



Ordering and Marking Information

APW9105 □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QB: TQFN3x2-14 Operating Ambient Temperature Range I : -40 to 85° C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW9105 QB : 	X - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{VIN}	VIN to PGND	-0.3 ~ 20	V
V_{BS}	BST to LX	-0.3 ~ 5.5	V
V_{LX}	LX to PGND	-1 ~ 20	V
$V_{I/O}$	VCC, VDD, PG, ASP, PM, EN/SYNC, FB to GND	-0.3 ~ 6	V
PD	Power Dissipation	Internally Limited	W
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature(10 Seconds)	260	°C

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)	68	°C/W
θ_{JA}	Junction-to-Ambient Resistance (Note 3)	31.2	°C/W

Note 2: θ_{JA} is measured on 4 layers test board following the EIA/JESD51-7.
Note 3: θ_{JA} is measured on Anpec evaluation board in free air.

Recommended Operation Conditions (Note 4)

Symbol	Parameter	Range	Unit
V_{IN}	VIN supply voltage	4.5 ~ 18	V
$V_{EN/SYNC}$	EN/SYNC input voltage	0 ~ 5	V
V_{OUT}	Converter output voltage	0.6 ~ 5	V
V_{PM}	PM input voltage	0 ~ 5	V
V_{DD}	VDD input voltage	0 ~ 5	V
I_{OUT}	Converter output current	0 ~ 6	A
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 4: Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over VIN=12V, T_A=25°C

Symbol	Parameter	Test condition	Specification			Unit
			Min.	Typ.	Max.	
SUPPLY						
V_{UVLO_R}	UVLO Upper Threshold	VIN Rising	-	4.2	-	V
V_{UVLO_HYS}	UVLO Hysteresis Voltage	VIN Falling	-	0.4	-	V
I_{VIN_SHDN}	VIN Shutdown Current	EN/SYNC=GND	-	3	-	μA
EN/SYNC Threshold						
V_{EN_H}	EN/SYNC Input Threshold High Voltage	For Enable Chip	-	1	1.15	V
V_{EN_Hys}	EN/SYNC Input Hysteresis Voltage	For Disable Chip	-	0.25	-	V
$T_{DB\_EN\_OFF}$	EN/SYNC Turn Off Debounce Time		-	20	-	μs
T_{D_EN}	EN/SYNC Turn On Delay Time	When EN/SYNC High to LX Switching	-	600	-	μs
I_{EN}	EN/SYNC Input Current	VEN/SYNC=2V	-	2	-	μA
R_{DIS}	Discharge Resistor	When EN/SYNC goes Low	-	15	-	Ω
	EN/SYNC Input High Threshold	For SYNC Function	1.8	-	-	V
	EN/SYNC Input Low Threshold	For SYNC Function	-	-	0.25	V
F_{SYNC}	SYNC Frequency Range		400	-	2000	kHz
REGULATOR AND VCC						
V_{REF}	Reference Voltage	T_J=25°C	594	600	606	mV
V_{POR}	VCC POR Threshold Voltage	VCC Rising	-	4	-	V
V_{POR_Hys}	VCC POR Hysteresis Voltage	VCC Falling	-	0.4	-	V
V_{VCC}	VCC Regulator Output Voltage	I_{VCC}=0A	-	5	-	V
	VCC Load Regulation	I_{VCC}=10mA	-	3	-	%
t_{SS}	Output Soft Start Time		-	1.15	-	ms
OSCILLATOR FREQUENCY						
F_{OSC}	Oscillator Frequency		-	600	-	kHz
	Frequency Accuracy	T_J=-40~125°C	-20	-	+20	%
	Minimum Controllable on Time		-	55	-	ns
	Maximum Duty	Fsw=600kHz	-	90	-	%
POWER MOSFET						
	High Side MOSFET Resistance		-	40	-	mΩ
	Low Side MOSFET Resistance		-	20	-	mΩ
	High Side MOSFET Leakage Current	$V_{EN/SYNC}$=0V, V_{LX}=GND	-	1	-	μA
	Low Side MOSFET Leakage Current	$V_{EN/SYNC}$=5V, V_{LX}=VIN, FB=0.7V	-	1	-	μA
BOOTSTRAP POWER						
R_{BST}	BST Switch On Resistance	VEN/SYNC=5V, LX=-0.1V, BST Source 0.1A	-	10	-	Ω
	BST Leakage Current	V_{BST-LX}=5V	-	-	1	μA

Electrical Characteristics (Cont.)

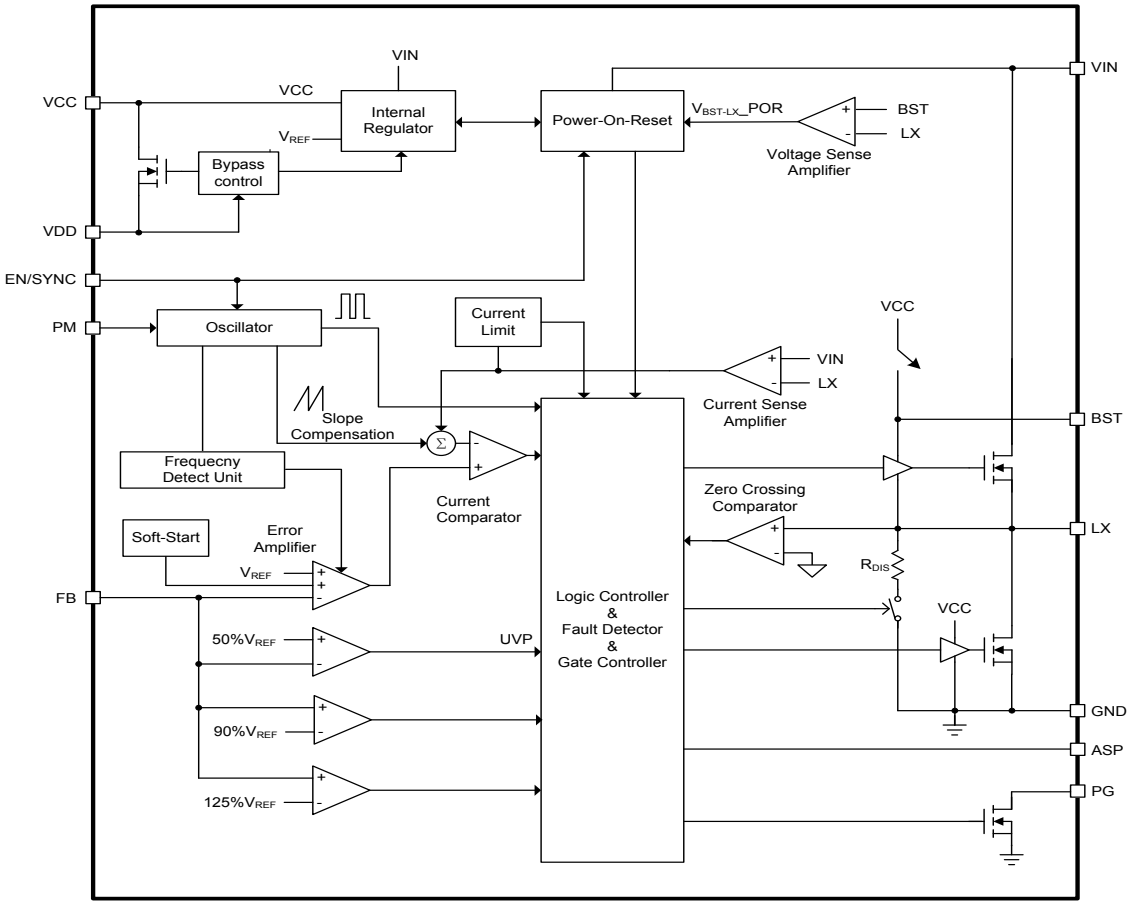
Unless otherwise specified, these specifications apply over VIN=12V, T_A=25°C

Symbol	Parameter	Test condition	Specification			Unit
			Min.	Typ.	Max.	
PROTECTIONS						
I_{LIM}	High Side MOSFET current-limit		-	9.5	-	A
	Over-temperature Trip Point	Guarantee by design	-	150	-	°C
	Over-temperature Hysteresis	Guarantee by design	-	30	-	°C
	Under Voltage Protection		-	50	-	$\%V_{REF}$
	Hiccup Count Ratio		-	9.5	-	
	Over Voltage Protection		-	125	-	$\%V_{REF}$
	Over Voltage Protection Hysteresis		-	7	-	$\%V_{REF}$
VDD						
V_{BYP}	VDD Bypass Threshold	Rising	-	4.65	-	V
		Hysteresis	-	0.25	-	V
R_{BYP}	Bypass Switch On Resistance		-	1.6	-	Ω
Power Mode (PM) Pin						
V_{PM_H}	PM Input Voltage High	PM from Low to High	3	-	-	V
V_{PM_L}	PM Input Voltage Low	PM from High to Low	-	-	0.7	V
R_{PM}	PM Pull Low Resistance	V_{PM}=VCC	-	1	-	MΩ
Power Good						
V_{PG_H}	PG In (PG goes high)	VOUT rising	-	0.9	-	VOUT
V_{PM_HYS}	PG Out (PG goes low)	VOUT falling	-	0.7	-	VOUT
ASP						
	ASP High Side Leakage	EN/SYNC=0	-	-	1	μA
	ASP High Side Leakage	EN/SYNC=0	-	-	1	μA

Pin Descriptions

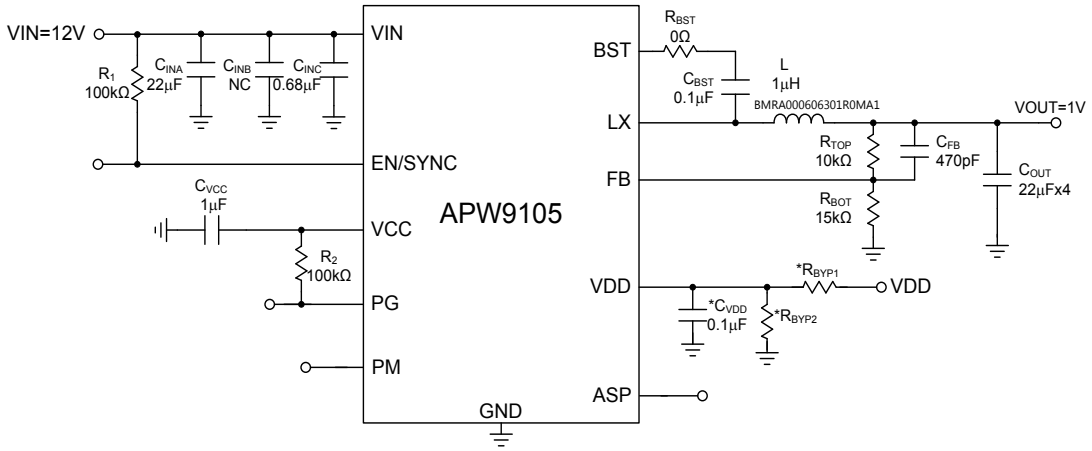
PIN		FUNCTION
NO.	NAME	
1,12, 13,14	GND	Power Ground. This pin must be connected directly to the GND plane of the PCB using low inductance vias.
2,15	VIN	Power Input Pin. VIN supplies the power to the buck converter.
3	ASP	Synchronous Clock Output Pin. If the EN/SYNC pin receives a synchronization signal, the ASP outputs a clock with the same frequency as EN/SYNC and shifts phase 45 degree; the ASP will maintain high-Z state when no external clock is received.
4	PG	Output Power Good Indicator Pin. This pin is an open-drain device; connect a pull-up resistor to an external supply voltage for the PG function.
5	PM	Force PWM Mode Enable Pin. If this pin is pulled low, the IC will operate in automatic PSM/PWM mode. If this pin is pulled high, the IC will operate in forced PWM mode. The PM pin cannot be left floating.
6	EN/SYNC	Enable_Synchronous Clock Input Pin. Drive EN/SYNC high to turn the converter on and drive EN/SYNC low to turn it off. And Input an external clock signal to this pin for synchronization function. EN/SYNC pin can configure SpeedTrans™, If EN/SYNC voltage is between 1V-1.3V, the SpeedTrans™ mode ON; If EN/SYNC voltage is >1.8V, the SpeedTrans™ mode OFF. The voltage is only being detected during power on, the synchronization function wouldn't be affected after soft-start.
7	VDD	External 5V supply. In order to reduce the power consumption of the internal LDO, an external 5V to VDD can be connected to replace the internal control circuit supply voltage. If the VDD bypass function is not used, be sure to connect VDD pin to GND. If this function is to be used, the VIN voltage must be greater than 5.5V.
8	FB	Output Feedback Pin. FB senses the output voltage and regulates it. Connect the resistor divider from the output through FB to the ground to set the output voltage.
9	VCC	Internal Regulator Output Pin. The APW9105 provides an internal 5V VCC regulator for the internal control circuitry. It is recommended to connect a 1μF X5R capacitor from the VCC pin to ground to ensure stability and regulation. Do not apply an external load to VCC.
10	BST	High-Side Gate Driver Supply Voltage Input Pin. A 0.1μF X5R ceramic capacitor is connected from this pin to the LX pin to provide a bootstrap voltage for the gate driver to drive the upper MOSFET.
11	LX	Power Switching Output. This pin is the junction of the high side power MOSFET and the low side power MOSFET. Connect this pin to the output inductor.

Block Diagram



Typical Application Circuit

1.SpeedTrans™ OFF (EN/SYNC=5V)

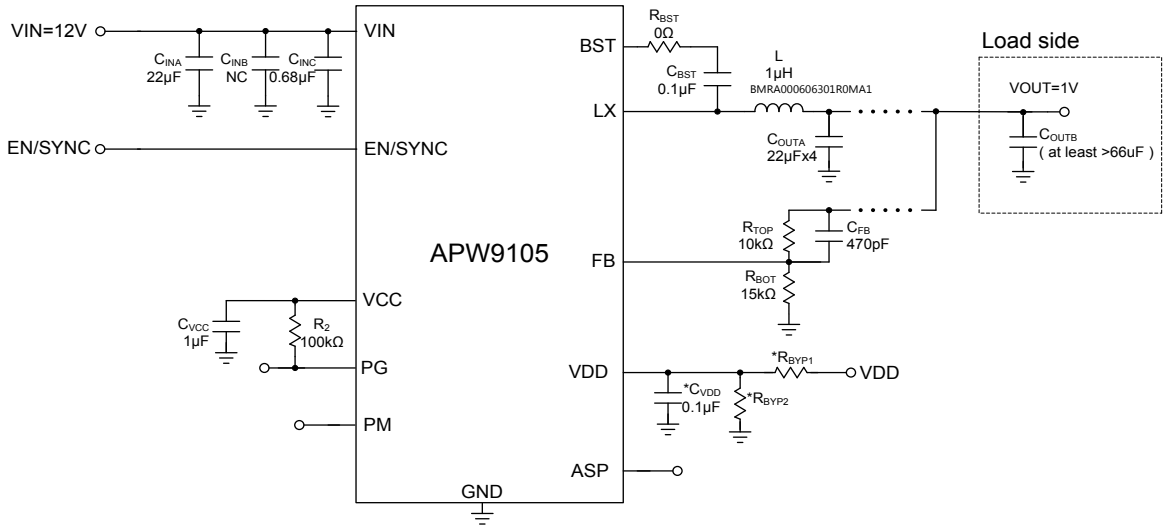


*Note 5: If the VDD bypass function is not used, be sure to connect VDD pin to GND by RBYP2, CVDD and RBYP1 are open. For better efficiency, please connect VDD pin to external 5V through RBYP1 and CVDD must be placed close this pin.

Components Selection for Different Output Voltage

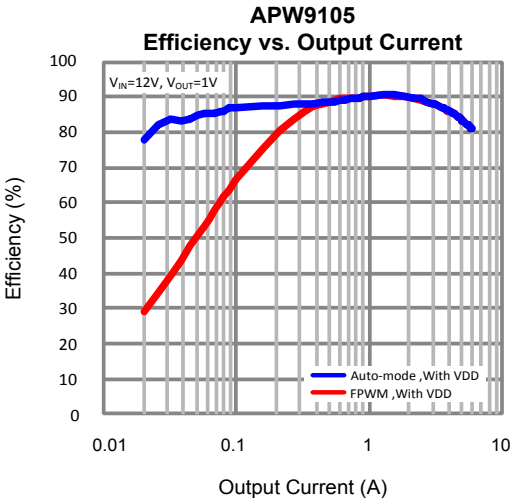
VIN (V)	VOUT (V)	IOUT (A)	C_{IN} (F)	L (H)	C_{OUT} (F)	R_{TOP} (Ω)	R_{BOT} (Ω)	C_{FB} (F)
12	1	0 ~ 6A	22µ × 1	1µ	22µ × 4	10k (1%)	15k (1%)	470p
12	1.8	0 ~ 6A	22µ × 1	1.5µ	22µ × 4	30k (1%)	15k (1%)	220p
12	3.3	0 ~ 6A	22µ × 1	2.2µ	22µ × 4	68k (1%)	15k (1%)	130p
12	5	0 ~ 6A	22µ × 1	3.3µ	22µ × 4	110k (1%)	15k (1%)	75p

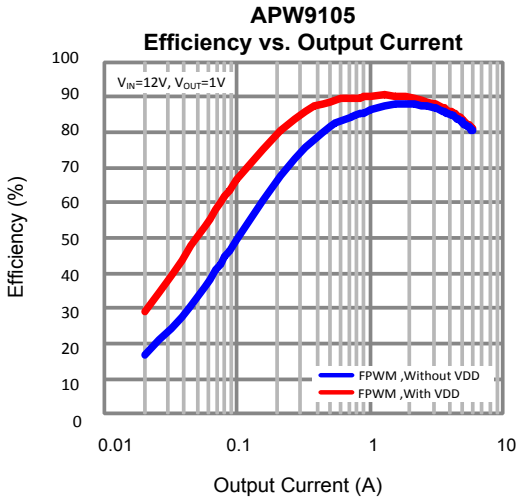
2.SpeedTrans™ ON (EN/SYNC=1.2V)

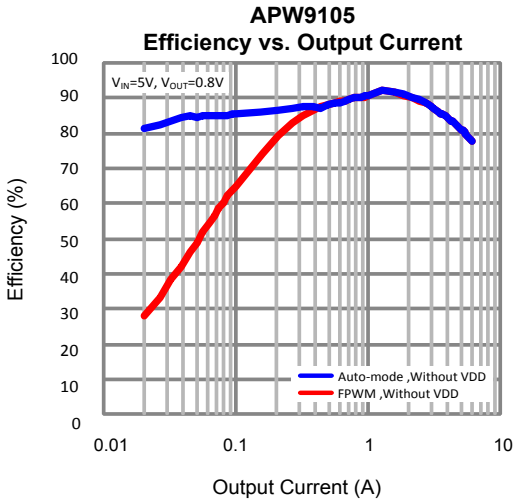


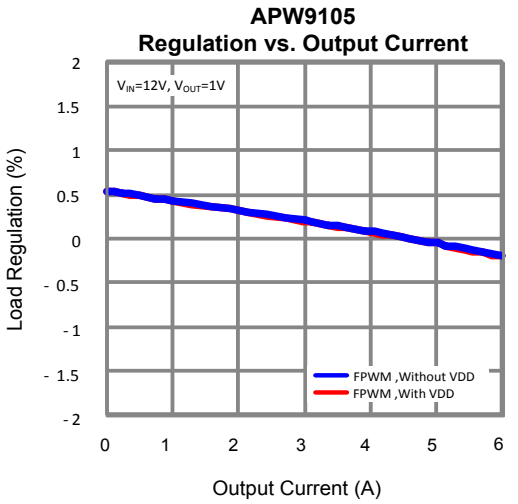
Typical Operating Characteristics

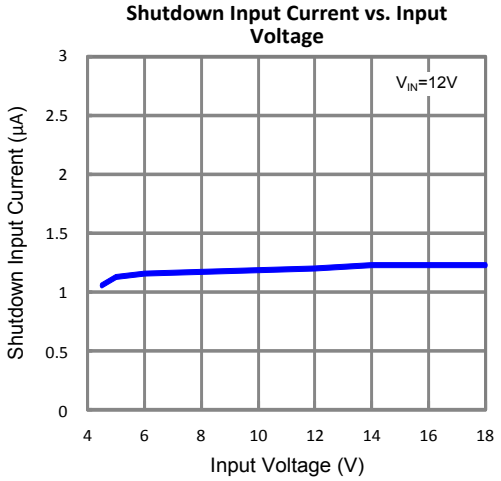
Refer to the typical application circuit. The test condition is V_{IN}=12V, C_{OUT}=22µF*2, T_A= 25°C unless otherwise specified.

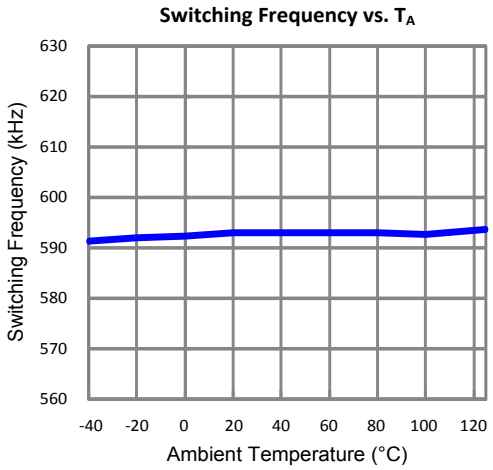






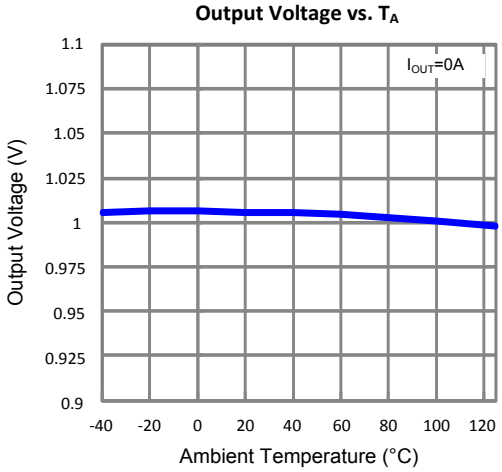






Typical Operating Characteristics (Cont.)

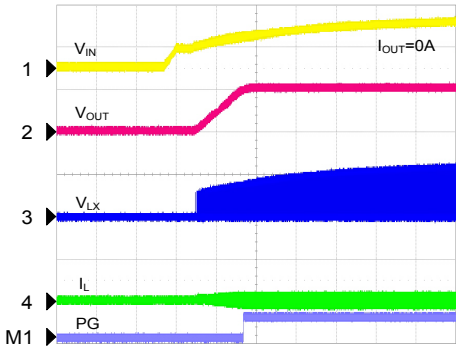
Refer to the typical application circuit. The test condition is V_{IN}=12V, C_{OUT}=22µF*2, T_A= 25°C unless otherwise specified.



Operating Waveforms

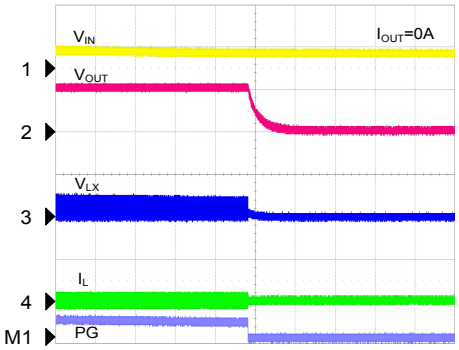
Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.

Start-Up by VIN



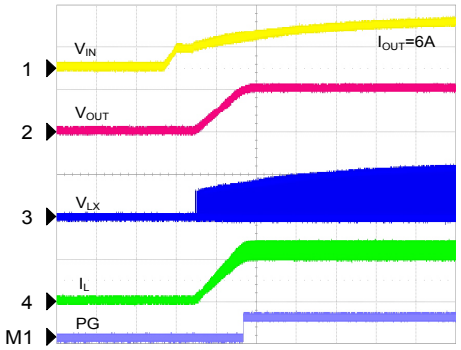
CH1: V_{IN}, 10V/Div
CH2: V_{OUT}, 1V/Div
CH3: V_{LX}, 10V/Div
CH4: I_L, 5A/Div
M1: PG, 10V/DIV
Time: 1ms/Div

Shutdown by VIN



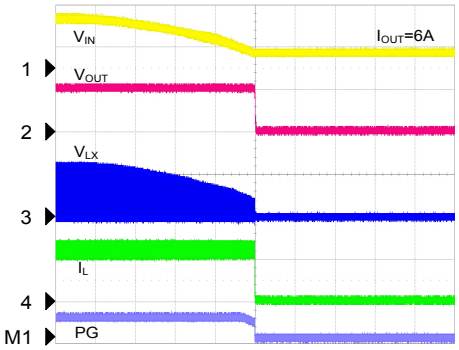
CH1: V_{IN}, 10V/Div
CH2: V_{OUT}, 1V/Div
CH3: V_{LX}, 10V/Div
CH4: I_L, 5A/Div
M1: PG, 10V/DIV
Time: 5ms/Div

CH1 Start-Up by VIN



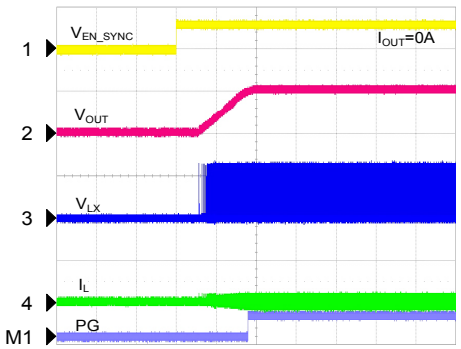
CH1: V_{IN}, 10V/Div
CH2: V_{OUT}, 1V/Div
CH3: V_{LX}, 10V/Div
CH4: I_L, 5A/Div
M1: PG, 10V/DIV
Time: 1ms/Div

CH1 Shutdown by VIN



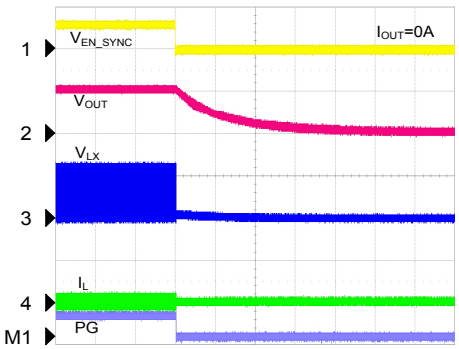
CH1: V_{IN}, 10V/Div
CH2: V_{OUT}, 1V/Div
CH3: V_{LX}, 10V/Div
CH4: I_L, 5A/Div
M1: PG, 10V/DIV
Time: 1ms/Div

Start-Up by Enable



CH1: $V_{EN/SYNC}$, 5V/Div
CH2: V_{OUT}, 1V/Div
CH3: V_{LX}, 10V/Div
CH4: I_L, 5A/Div
M1: PG, 10V/DIV
Time: 1ms/Div

Shutdown by Enable

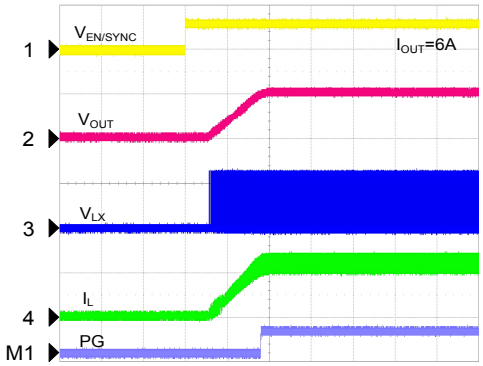


CH1: $V_{EN/SYNC}$, 5V/Div
CH2: V_{OUT}, 1V/Div
CH3: V_{LX}, 10V/Div
CH4: I_L, 5A/Div
M1: PG, 10V/DIV
Time: 1ms/Div

Operating Waveforms (Cont.)

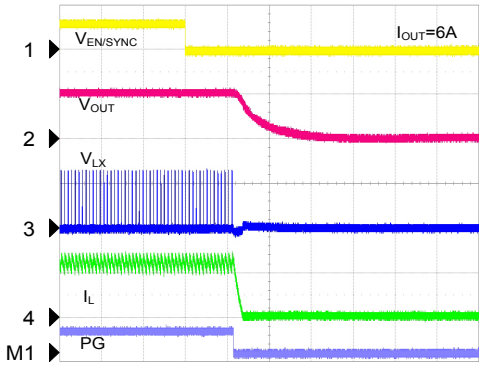
Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.

Start-Up by Enable



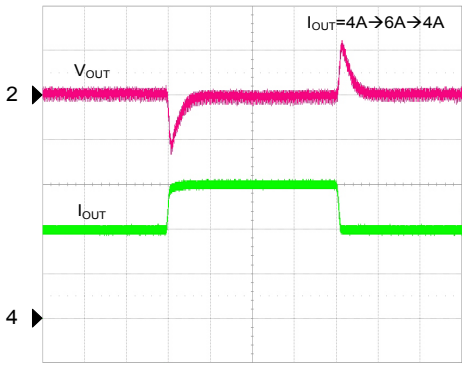
CH1: $V_{EN/SYNC}$, 5V/Div
CH2: V_{OUT}, 1V/Div
CH3: V_{LX}, 10V/Div
CH4: I_L, 5A/Div
M1: PG, 10V/DIV
Time: 1ms/Div

Shutdown by Enable



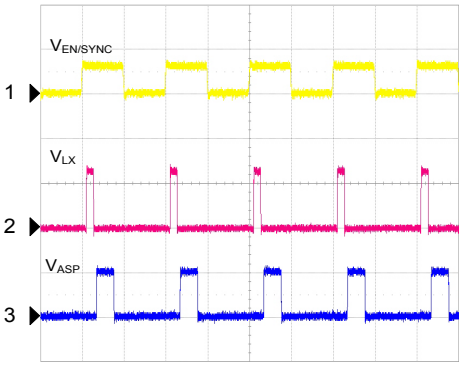
CH1: $V_{EN/SYNC}$, 5V/Div
CH2: V_{OUT}, 1V/Div
CH3: V_{LX}, 10V/Div
CH4: I_L, 5A/Div
M1: PG, 10V/DIV
Time: 20µs/Div

Load Transient



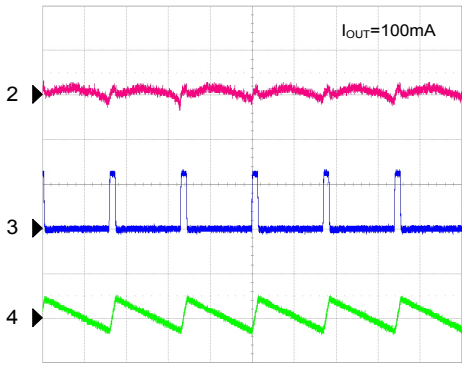
CH2: V_{OUT}, 50mV/Div, AC
CH4: I_{OUT}, 2A/Div
Time: 50µs/Div

ASP Output



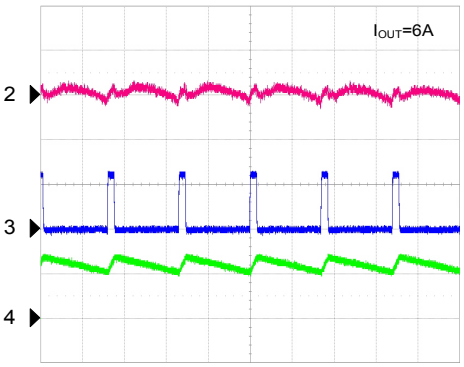
CH1: $V_{EN/SYNC}$, 5V/Div
CH2: V_{LX}, 10V/Div
CH3: V_{ASP}, 5V/Div
Time: 500ns/Div

Output Ripple



CH2: V_{OUT}, 20mV/Div, AC
CH3: V_{LX}, 10V/Div
CH4: I_L, 2A/Div
Time: 1µs/Div

Output Ripple

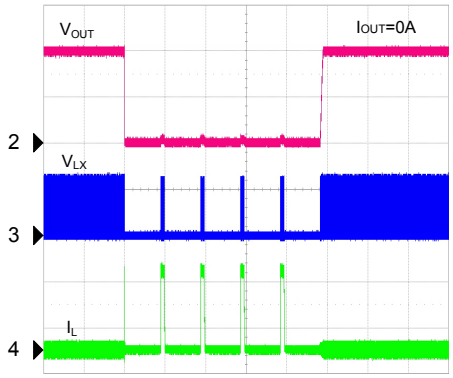


CH2: V_{OUT}, 20mV/Div, AC
CH3: V_{LX}, 10V/Div
CH4: I_L, 5A/Div
Time: 1µs/Div

Operating Waveforms (Cont.)

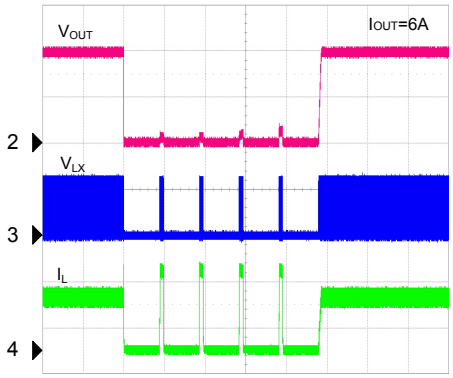
Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.

Short Circuit Protection



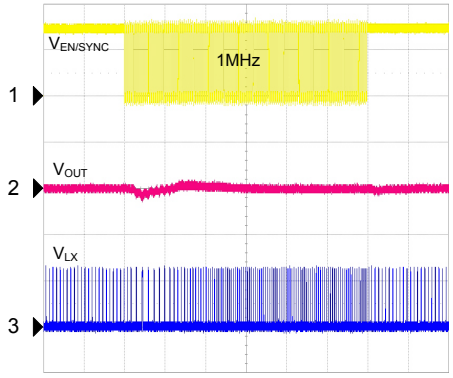
CH2: V_{OUT}, 500mV/Div
CH3: V_{LX}, 10V/Div
CH4: I_L, 5A/Div
Time: 20ms/Div

Short Circuit Protection



CH2: V_{OUT}, 500mV/Div
CH3: V_{LX}, 10V/Div
CH4: I_L, 5A/Div
Time: 20ms/Div

SYNC Transient



CH1: $V_{EN/SYNC}$, 2V/Div
CH2: V_{OUT}, 200mV/Div, AC
CH3: V_{LX}, 10V/Div
Time: 20µs/Div

Function Descriptions

Main Control Loop

The IC uses current mode control to regulate the output voltage. The output voltage is measured at FB through a resistor divider and amplified by an internal transconductance error amplifier. The output of the transconductance error amplifier is compared to the switching current to adjust the duty cycle to control the output voltage.
The benefit of current mode control is the ability to quickly adjust the duty cycle as the output current increases rapidly for fast load transient response.

VIN Under Voltage Lock Out

When the IC is powered up, the internal circuitry except VCC remains inactive until the VIN voltage exceeds the VIN UVLO high threshold voltage. When VIN is below the VIN UVLO low threshold voltage, the IC is turned off and the output discharge is triggered.

VCC Power-On-Reset (POR)

VCC is an internal voltage regulator that is activated when the IC is powered by VIN and EN goes high. The IC continuously monitors the voltage on the VCC pin. The soft start is activated, when the VCC voltage is higher than the POR threshold and the VIN voltage is higher than the UVLO threshold and the EN voltage is higher than the enable threshold.
VCC POR is used to protect the IC from erroneous operation with insufficient VCC voltage. VCC POR also has hysteresis to resist ripple on the VCC voltage.

Soft-Start

The IC has a built-in soft-start function that controls the rise time of the output voltage during start-up to reduce input current surges and prevent output overshoot.
The soft start function will be enabled when any condition that can initiate an output start-up, such as VIN power to the IC or toggle the EN pin, and when the converter is restarted from the OTP and hiccup mode.

Over-Temperature Protection (OTP)

The IC features over-temperature protection by monitoring its junction temperature and prevent damage to the chip when operating at extremely high temperatures. When the junction temperature exceeds the OTP threshold, the IC will be turned off to lower the junction temperature. The OTP circuit has hysteresis that allows the IC to restart when the junction temperature is below the OTP low threshold temperature.

Enable/Shutdown and Frequency synchronization

The IC provides the EN/SYNC pin, which is a digital input that turns the converter on or off. Drive EN/SYNC high to turn the converter on and drive it low to turn it off.
To synchronize the internal operating frequency of the IC with the external clock, connect the EN/SYNC pin to an external 50% duty cycle clock. The rising edge of the internal clock is synchronized with the rising edge of the external clock.

VDD Bypass Function

The APW9105 allows an external 5V to be supplied to the VDD pin where it automaticly disconnects internal LDO and switches the internal biasing of the regulator to the VDD supply. This function eliminates the LDO loss and improves the overall efficiency specially in the lighter load operation.

Current Limit and Hiccup

The IC monitors the current through the high-side power MOSFET to limits the peak inductor current to prevent IC from being damaged in the event of an overload or short circuit.
When the current limit protection is activated, the output current will be limited and the output voltage will drop. When the output voltage drops below the UVP threshold, UVP is triggered and the converter enters hiccup mode.
In hiccup mode, the converter will restart periodically. This protection mode is especially useful when the output is shorted to ground. The average short-circuit current is greatly reduced to alleviate thermal issues and protect the IC. Once the over-current condition is removed, the IC will exit the hiccup mode.

Fast Discharge

When the EN signal goes low or the VIN voltage falls below the UVLO threshold, the IC is turned off and the output fast discharge is triggered.
The discharge MOSFET between the LX of the converter and ground is turned on, allowing the output capacitor to be quickly discharged through this MOSFET.

ASP

The APW9105 is part of the family of converters with a proprietary **ANPEC System Phase Shift** (ASP) method that allows multiple converters to be daisy chained together while being able to synchronize to an external clock, allowing for a much reduced system noise performance.
When using external frequency synchronization, the ASP pin generates a clock signal of the same frequency and 45 degree phase shift. This signal is then used to synchronize another device allowing it to turn on at a delay time which reduces the net EMI of the system.

Power Good (PG)

The IC has an open-drain PG pin that indicates the output regulation state. During soft start, when the output voltage reaches 90% of its target value this pin will switch HI after a de-bounce time. If the output voltage is below 70% of its regulated voltage, PG signal will be pulled low. Since PG is an open-drain output device, it requires an external pull-up resistor; however, if the pin is not used, no resistor is needed.

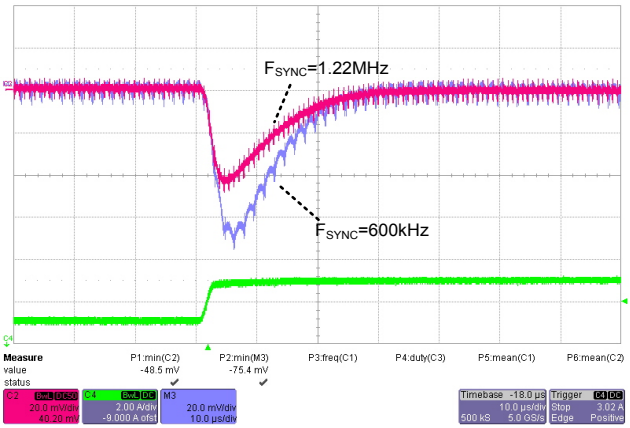
PM Pin

The PM pin allows the converter to either operate in fixed frequency PWM mode or in an automatic PSM/PWM mode. If the PM pin is left open or pulled HI, the IC will always be a in a fixed frequency mode regardless of the load current. This frequency will be either fixed internal frequency of 600kHz. If the PM pin is connected to GND, the IC is in the automatic PSM/PWM mode.

Function Descriptions (Cont.)

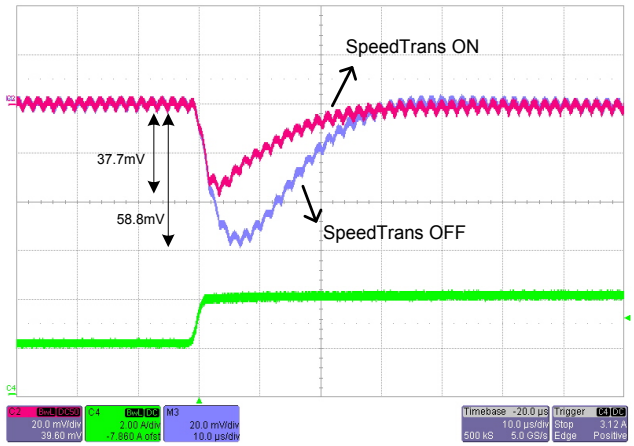
DyncBandwidth™ Technology

DyncBandwidth, dynamic bandwidth compensation, is a technique to allow the converter running with the best transient response over a wide range of switching frequencies. When receiving an external clock, the converter will automatically adjust the internal compensation through the internal Frequency Detection Unit.



SpeedTrans™ Technology

SpeedTrans™, speed up transient mode, is a technique to improve transient response for strict undershoot/overshoot specification as well as reduce the quantity of output capacitors. When the EN/SYNC voltage is between 1V to 1.3V, the converter will automatically adjust the internal loop compensation through the Voltage Detection Unit. The voltage detection unit is operated only during power on; therefore, it wouldn't affect synchronization function. When enable SpeedTrans™, please ensure adding extra capacitors at load side (at least >66uF).



Application Information

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, select the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage.
Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended highly because of their low ESR and small temperature coefficients.
Since the input capacitor (CIN) absorbs the input-switching current, it requires an adequate ripple-current rating. The RMS current in the input capacitor can be estimated by:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at VIN = 2VOUT, where:

$$I_{CIN} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor with a RMS current rating greater than half of the maximum load current.
The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high-quality ceramic capacitor (e.g. 0.1μF) should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge in order to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{OSC} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Output Capacitor Selection

The output capacitor is required to filter the output and provide load transient current. The higher capacitance value will provide the smaller output ripple and better load transient.
Ceramic electrolytic capacitors with X5R or X7R dielectrics and low ESR are recommended to keep the output voltage ripple low. The output voltage ripple caused by the capacitance can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{OSC} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times F_{OSC} \times C_{OUT}}\right)$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

Output Inductor Selection

The inductance value will determine the inductor ripple current and affects the load transient response and output ripple voltage.
The larger inductance value will result in a smaller ripple current, which will result in a lower output ripple voltage but a slower transient response, while a smaller inductance value will have opposite result.
A good rule is to choose the inductor ripple current that is about 30% of the maximum output current. Use the following equation to derive the inductance value for most designs:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times F_{OSC}}$$

Where, ΔI_L is the inductor-ripple current.

To avoid inductor saturation, the inductor current rating should be at least the converter's maximum output current plus the inductor ripple current. The maximum inductor peak current can be estimated by:

$$I_{L(MAX)} = I_{OUT} + \frac{\Delta I_L}{2}$$

In addition, choosing an inductor with a smaller DCR will provide better efficiency, and it is recommended that the inductor's DCR should be less than 15m ohms.

Output Voltage Setting

The output voltage is set by a resistor voltage divider between output terminal and ground. For detailed voltage divider settings, please refer to “Typical Application Circuit”. The output voltage can be calculated as follows:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$$

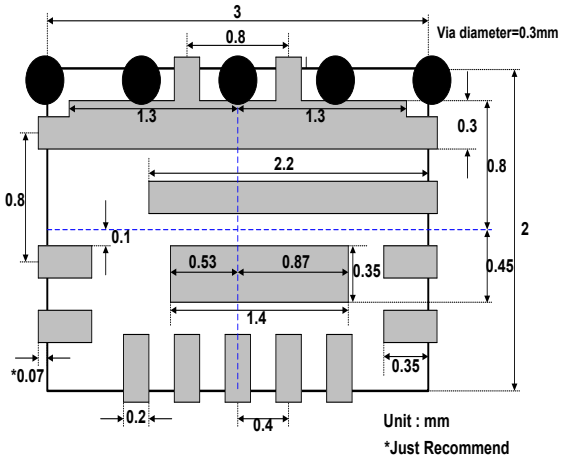
Application Information (Cont.)

Layout Consideration

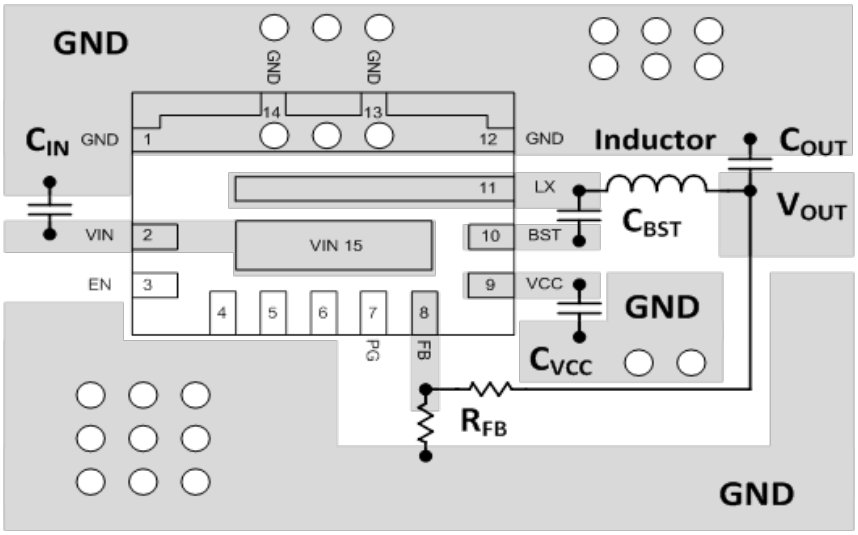
For all switching power supplies, the layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

1. The VIN input capacitor should be placed close to the VIN and PGND pins(<1mm). Connecting the capacitor and VIN/PGND pins with short and wide trace without any via holes for good input voltage filtering. The distance between VIN/PGND to capacitor less than 2mm respectively is recommended.
2. Place the VCC capacitor to VCC pin and GND pin as close as possible.
3. Place the inductor as close as possible to the LX pin to minimize noise coupling into other circuits.
4. The ground of the output capacitor and input capacitor and the PGND of the IC should be as close as possible.
5. Place the feedback resistor divider as close as possible to the FB pin to minimize FB high impedance trace. In addition, the FB pin trace cannot be routed close to the switching signal.
6. For better heat dissipation, it is highly recommended to place a large ground plane under the thermal pad of all PCB layers and place as many vias as possible on the thermal pad from the top layer to the bottom layer.
7. It is recommended to place the input capacitor, output capacitor and inductor on top layer, and use a large power GND plane to connect the ground of the input capacitor, the ground of the output capacitor, and the PGND of the IC.

Recommended Minimum Footprint (Top View)

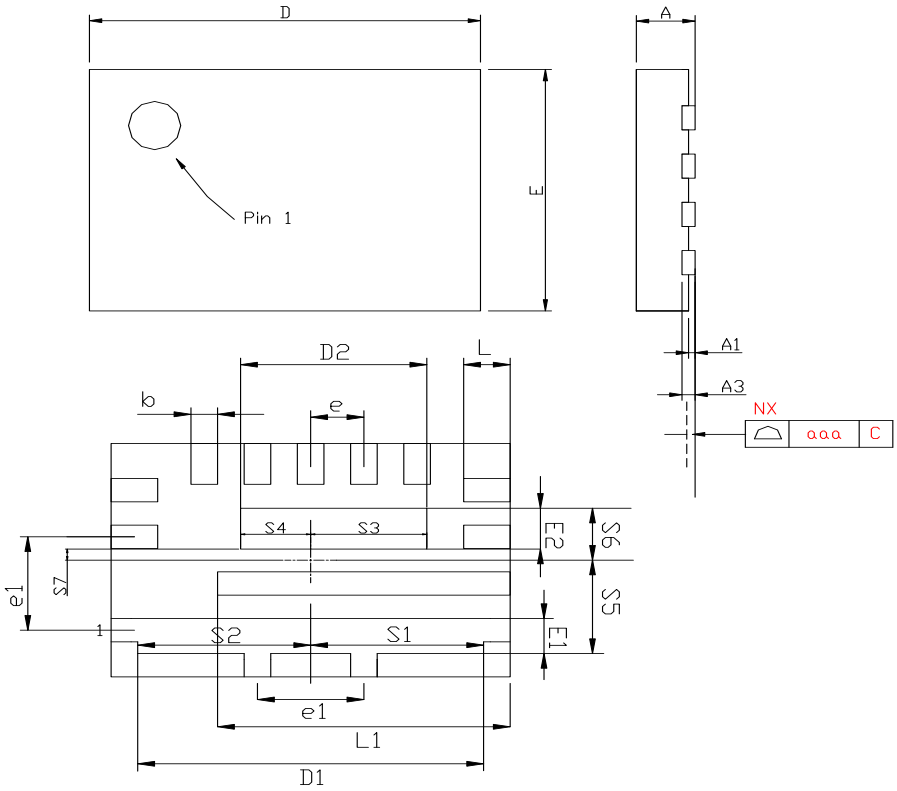


Layout Example



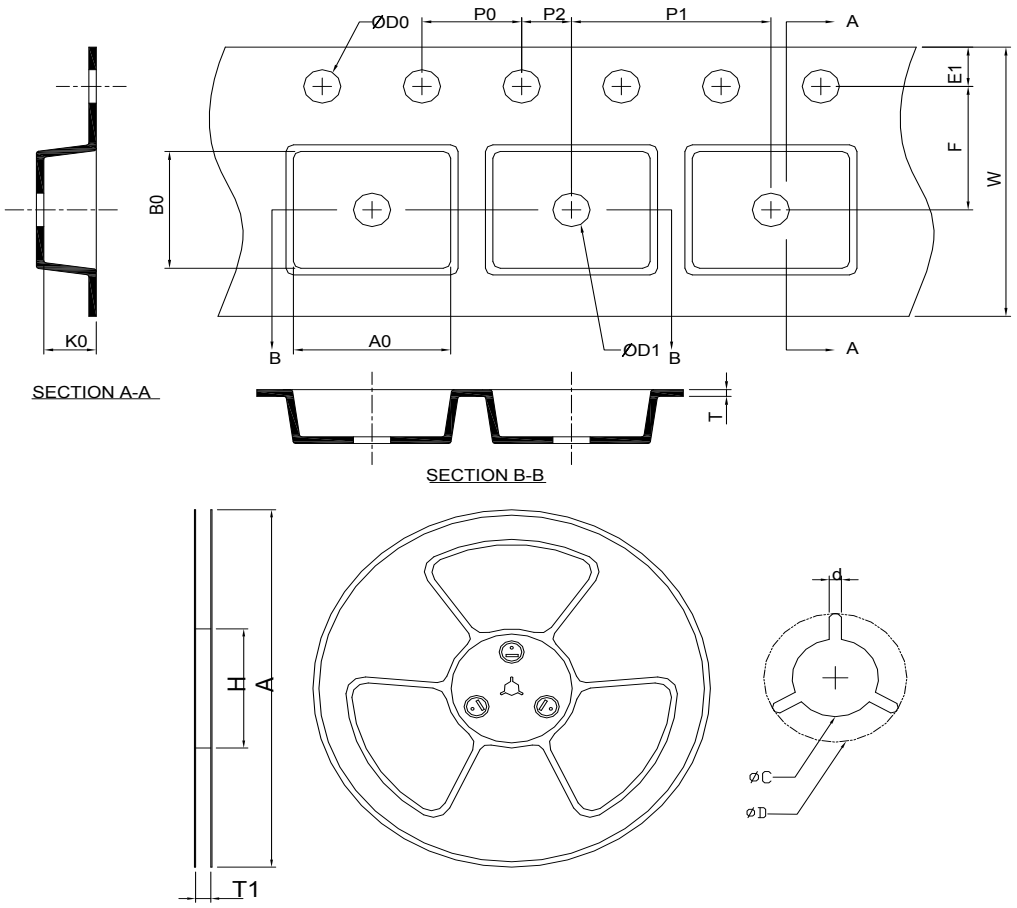
Package Information

TQFN3x2-14



SYMBOL	TQFN3*2-14			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.032
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.15	0.25	0.006	0.010
D	2.90	3.10	0.114	0.122
E	1.90	2.10	0.075	0.083
e	0.40 BSC		0.016 BSC	
e1	0.80 BSC		0.032 BSC	
L	0.30	0.40	0.012	0.016
L1	2.15	2.25	0.085	0.089
D1	2.55	2.75	0.100	0.108
D2	1.35	1.45	0.053	0.057
E1	0.25	0.35	0.010	0.014
E2	0.30	0.40	0.012	0.016
S1	1.30 REF		0.051 REF	
S2	1.30 REF		0.051 REF	
S3	0.87 REF		0.034 REF	
S4	0.53 REF		0.021 REF	
S5	0.80 REF		0.031 REF	
S6	0.45 REF		0.018 REF	
S7	0.10 REF		0.004 REF	
aaa	0.08		0.003	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN3x2-14	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.20	1.75±0.10	3.50±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.25±0.05	2.30±0.20	3.30±0.20	1.00±0.20

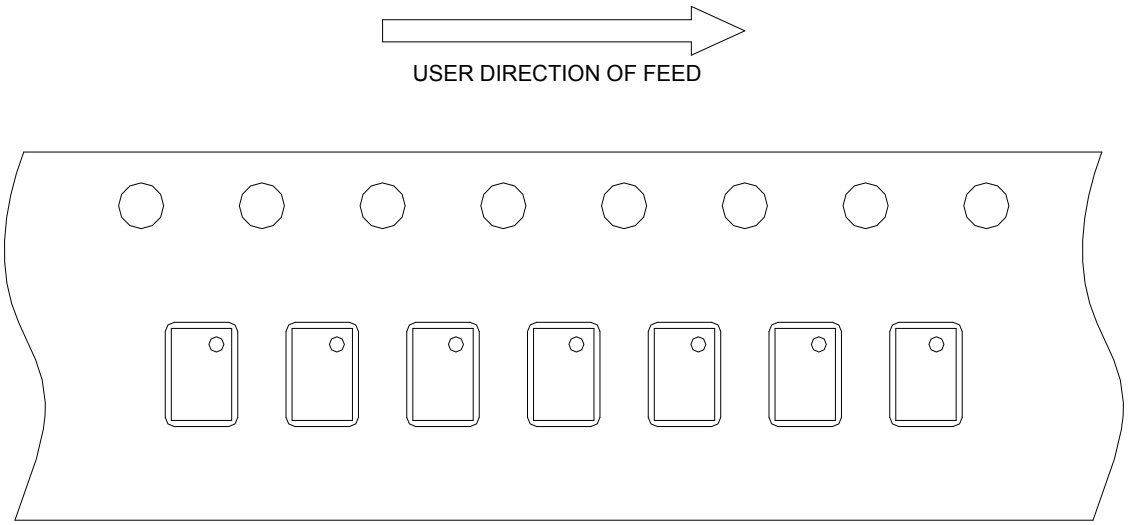
(mm)

Devices Per Unit

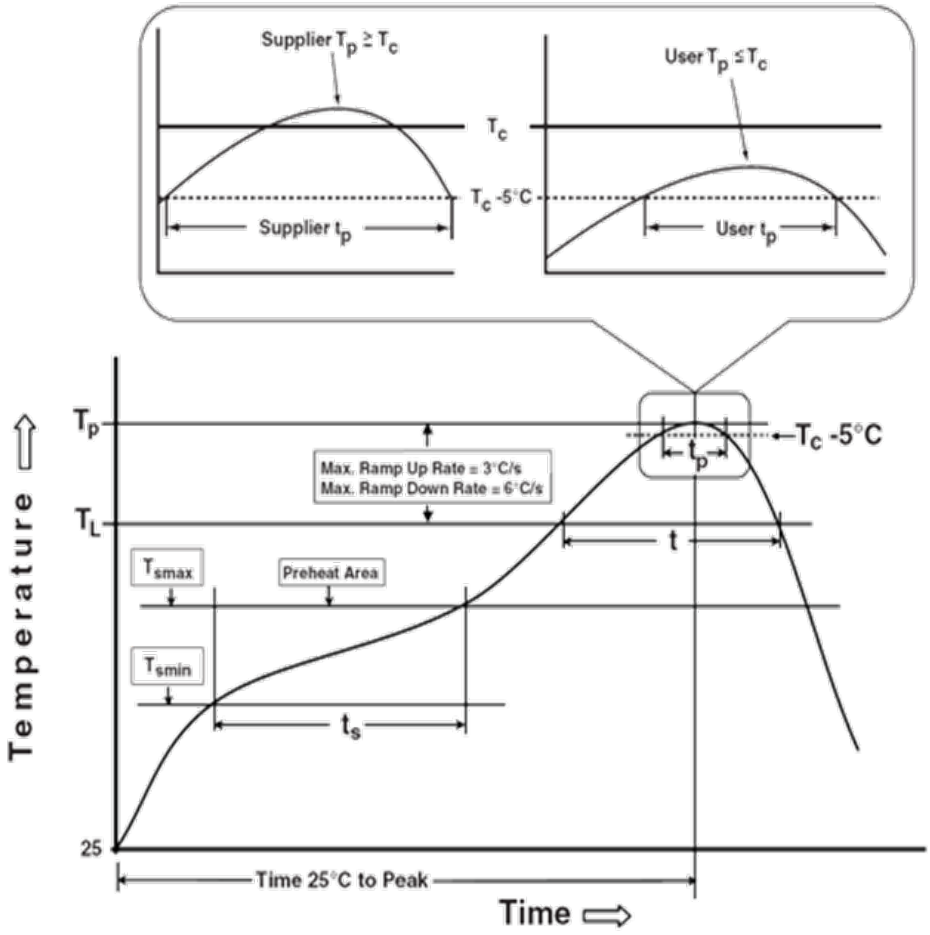
Package type	Packing	Quantity
TQFN3x2-14	Tape & Reel	3000

Taping Direction Information

TQFN3x2-14



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≧ 2KV
MM	JESD-22, A115	VMM ≧ 200V
Latch-Up	JESD 78	10ms, 1_{tr} ≧ 100mA

Customer Service

Anpec Electronics Corp.
Head Office :
No.6, Dusing 1st Road, SBIP,
Hsin-Chu, Taiwan, R.O.C.
Tel : 886-3-5642000
Fax : 886-3-5642050

Taipei Branch :
2F, No. 11, Lane 218, Sec 2 Jhongsing Rd.,
Sindian City, Taipei County 23146, Taiwan
Tel : 886-2-2910-3838
Fax : 886-2-2917-3838