8A Synchronous Buck Converter

Features

- **Wide Input voltage Range from 6V to 28V**
- **Provide PWM Converter with Adjustable 0.6V to 5.5V Output**
  - **0.6V Reference Voltage**
  - **Excellent Line/Load Regulations about ±1.5% over temperature range at PWM Channel**
- **Built in POR Control Scheme Implemented**
- **15mA 5V Voltage Output**
- **Constant On-Time Control Scheme with Frequency Compensation for PWM Mode**
- **Built in Soft Start for PWM Output and Soft Stop for PWM Output and LDO Output**
- **Integrated Bootstrap Forward P-CH MOSFET**
- **High Efficiency over Light to Full Load Range (PWMs)**
- **Built in Power Good Indicators (PWM)**
- **Integrated 24mΩ at VCC=5V N-Channel MOSFET For High Side**
- **Integrated 14mΩ at VCC=5V N-Channel MOSFET For Low Side**
- **60% Under-Voltage and 120% Over-Voltage Protections (PWM)**
- **Fixed Current-Limit Protection at 11A Loading (PWM)**
- **Over-Temperature Protection**
- **3mmx3mm Thin QFN-16A (TQFN3x3-16A) package**
- **Lead Free and Green Device Available (RoHS Compliant)**

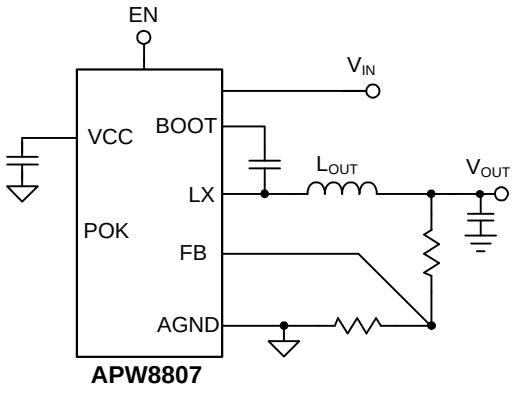
General Description

The APW8807 integrates the step-down, constant on-time, synchronous PWM converter with 24Ω N-channel high side MOSFET and 14Ω N-channel low side MOSFET, as well as various protections into a chip. The PWM converter step down high voltage of a battery to generate low-voltage, for NB applications.

The APW8807 provides excellent transient response and accurate DC output voltage in automatic PFM/PWM Mode. In Pulse-Frequency Mode (PFM), the APW8807 provides very high efficiency over light to heavy loads with loading-modulated switching frequencies. The PWM mode works nearly at constant frequency for low-noise requirements. The APW8807 is equipped with accurate sourcing current-limit, output under-voltage, output over-voltage protections, being perfect for NB applications. A 4.8ms (Typ.) soft-start can reduce the start-up current. A soft-stop function actively discharges the output capacitors by the discharge switch.

The APW8807 has enable control for PWM. Pulling the EN pin low shuts down the PWM output. The APW8807 is available in a TQFN3x3-16A package.

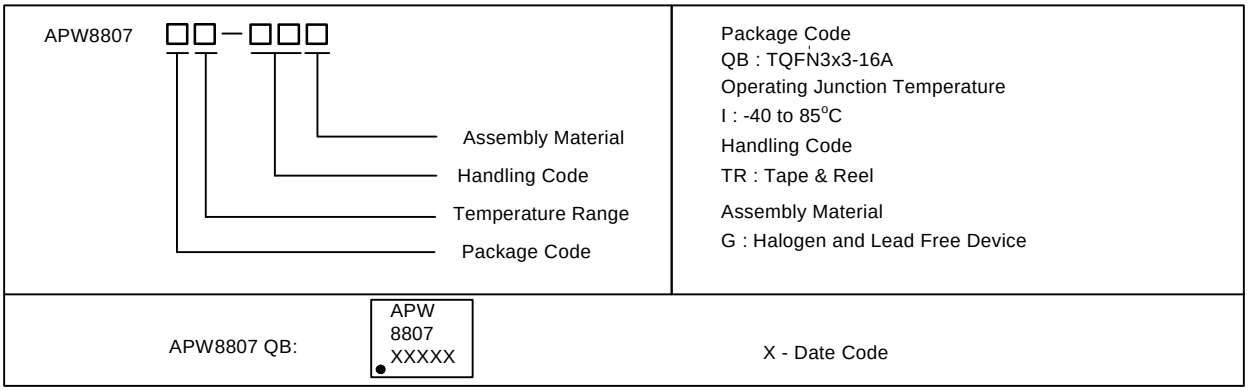
Simplified Application Circuit



Applications

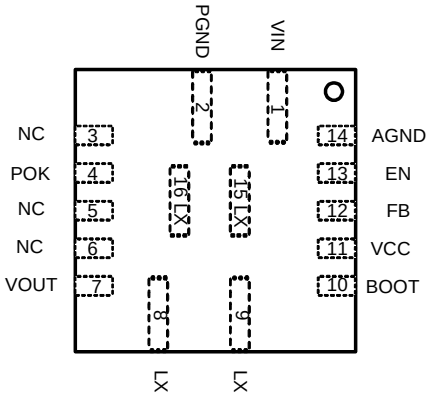
- **Notebook and Sub-Notebook Computers**
- **Portable Devices**
- **DDR1, DDR2, and DDR3 Power Supplies**
- **3-Cell and 4-Cell Li+ Battery-Powered Devices**
- **Graphic Cards**
- **Game Consoles**
- **Telecommunications**

Ordering and Marking Information



Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Pin Configuration



TQFN 3 x 3 -16A
Top View

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{CC}	VCC Supply Voltage (VCC to GND)	-0.3 ~ 7	V
V_{IN}	Input Power Voltage (VIN to GND)	-0.3 ~ 30	V
V_{BOOT}	BOOT Supply Voltage (BOOT to LX)	-0.3 ~ 7	V
$V_{BOOT-GND}$	BOOT Supply Voltage (BOOT to GND)	-0.3 ~ 37	V
V_{LX}	LX Voltage (LX to GND) <20ns pulse width >20ns pulse width	 -5 ~ 37 -0.3 ~ 30	V
	All Other Pins (LDO, VCLK, ENLDO, EN, VOUT, POK to GND)	-0.3 ~ V_{CC}+0.3	V
V_{GND}	AGND to PGND	-0.3 ~ +0.3	V
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature(10 Seconds)	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2) TQFN3x3-16A	95	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{IN}	PWM Converter Input Voltage	6 ~ 28	V
V_{CC}	VCC Supply Voltage	4.5 ~ 5.5	V
V_{OUT_PWM}	PWM Converter Output Voltage	0.6 ~ 5.5	V
I_{OUT_PWM}	PWM Converter Output Current	0~8	A
C_{IN}	PWM Converter Input Capacitor (MLCC)	10 ~	µF
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{CC}=5V, V_{IN}=12V and T_A= -40 to 85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Condition	APW8807			
			Min.	Typ.	Max.	Unit
VOUT PIN AND VOUT VOLTAGE						
V_{OUT}	Output Voltage Setting Range		0.6	-	5.5	V
	REF voltage		-	0.6	-	
	Regulation Accuracy	T_A = 25 °C	-0.5	-	+0.5	%
		T_A = -40 °C ~ 85 °C, Line & Load Regulations	-1.5	-	+1.5	%
R_{DIS}	VOUT Discharge Resistance	EN=0V, V_{OUT}=0.5V		-	80	Ω
SUPPLY CURRENT						
I_{VIN_PWM}	VIN Supply Current at PWM Mode	VOUT=5.5V, EN=5V, I_{OUT}=3A			1.53	A
I_{VIN_PFM}	VIN Supply Current at PFM Mode	VOUT=5.5V, EN=5V, I_{OUT}=0A	-	80	100	μA
I_{VIN_SD}	VIN Supply Current at Shutdown Mode	EN=0V	-	-	10	μA
ON-TIME TIMER AND INTERNAL SOFT START AND ZERO CROSSING						
F_{SW}	Switching Frequency at PWM	V_{IN}=12V, V_{OUT}=5.05V	450	500	550	kHz
$T_{ON(MIN)}$			-	100	-	ns
$T_{OFF(MIN)}$	Minimum off time	VFB=0.55V, V_{PHASE}=-0.1V	200	300	400	ns
T_{SS}	Internal Soft Start Time	EN High to V_{OUT} Regulation 95%	-	4.8	-	ms
V_{ZC}	Zero Crossing Comparator Offset	V_{GND}-V_{LX}	-5	-	5	mV
INTERNAL POWER MOSFETS AND DEAD TIME						
$R_{DS(ON)\_H}$	High Side N-MOSFET Resistance	VCC=5V	-	24	30	Ω
$R_{DS(ON)\_L}$	Low Side N-MOSFET Resistance	VCC=5V	-	14	18	Ω
BOOTSTRAP SWITCH						
V_F	Ron	V_{VCC} – $V_{BOOT-GND}$, I_F = 10mA	-	0.15	0.25	V
I_R	Reverse Leakage	$V_{BOOT-GND}$ = 30V, V_{LX} = 25V, V_{VCC} = 5V	-	-	0.5	μA
VCC POR THRESHOLD						
V_{POR_VCC}	VCC POR Threshold Voltage		4.25	4.35	4.45	V
	VCC POR Hysteresis		-	100	-	mV
CONTROL INPUTS						
	EN Leakage	EN=0V	-	0.1	1.0	μA
	EN Low Threshold	EN falling	1.05	1.35	1.65	V
	Hys.		-	200	-	mV

Electrical Characteristics(Cont.)

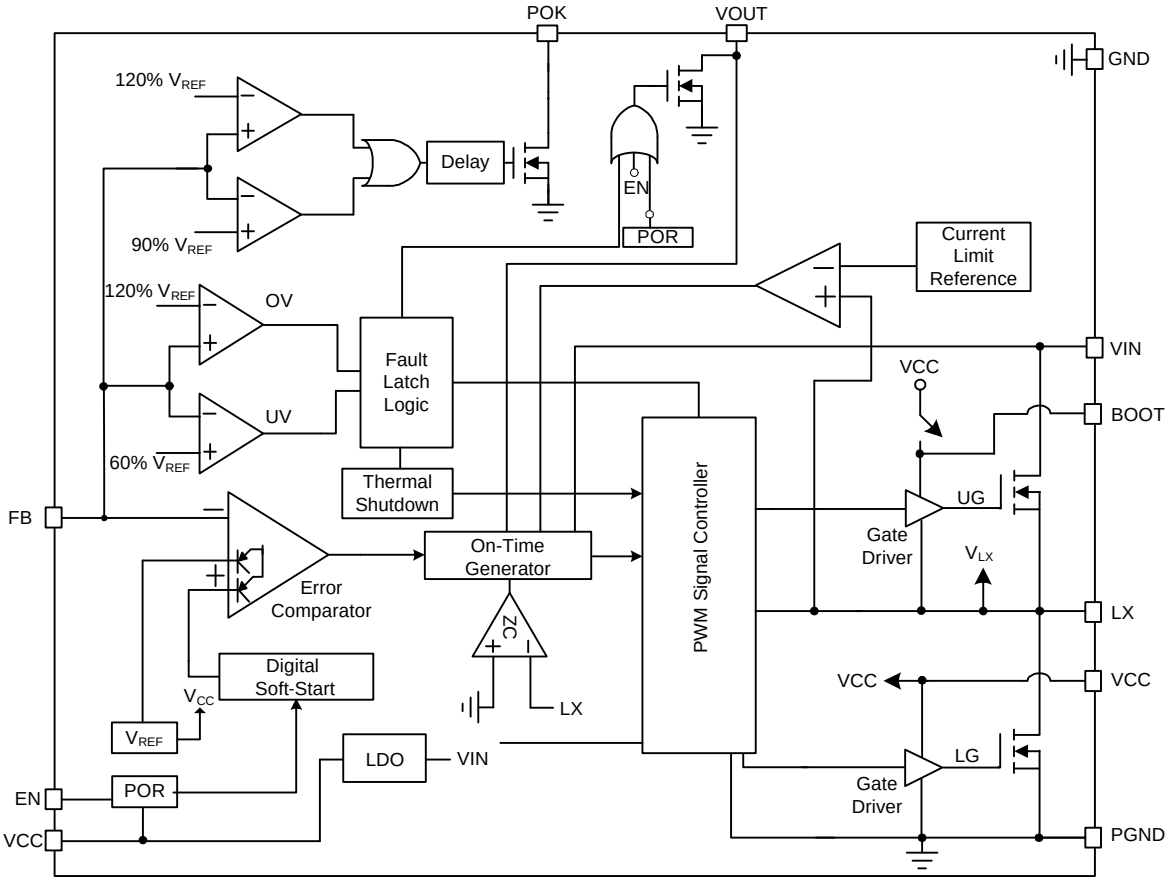
Unless otherwise specified, these specifications apply over V_{CC}=5V, V_{IN}=12V and T_A= -40 to 85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Condition	APW8807			
			Min.	Typ.	Max.	Unit
POWER-OK INDICATOR						
V_{POK}	POK Threshold	POK in from Lower (POK Goes High)	87	90	93	%
		POK Low Hystersis	-	3	-	%
		POK out from Normal high threshold (POK Goes Low)	115	120	125	%
I_{POK}	POK Leakage Current	V_{POK}=5V	-	0.1	1.0	µA
	POK Sink Current	V_{POK}=0.5V	2	4	-	mA
	POK Out Debounce Time1	When enter 120% threshold	-	2	-	µs
	POK Out Debounce Time2	When enter 87% threshold	-	16	-	µs
	POK Enable Delay Time	From EN High to POK High	-	5.3	-	ms
PROTECTION						
I_{CL}	Low Side Current Limit	Valley current	10	11	12	A
V_{UV}	UVP Threshold		55	60	65	%
	UVP Debounce Interval		-	2	-	µs
	UVP Enable Delay	EN high to UVP workable	-	5.3	-	ms
V_{OVP}	OVP Rising Threshold		115	120	125	%
		HYS	-	10	-	%
	OVP Propagation Delay	V_{FB} Rising, Over voltagee=10mV	-	2	-	µs
T_{OTP}	OTP Rising Threshold (Note 5)		-	150	-	°C
	OTP Hysteresis (Note 5)		-	40	-	°C
VCC Regulator						
	VCC Regulator Output Voltage	VIN=6V~28V, no load	4.8	5	5.2	V
	VCC Load Regulation	Icc=15mA	-	5	-	%

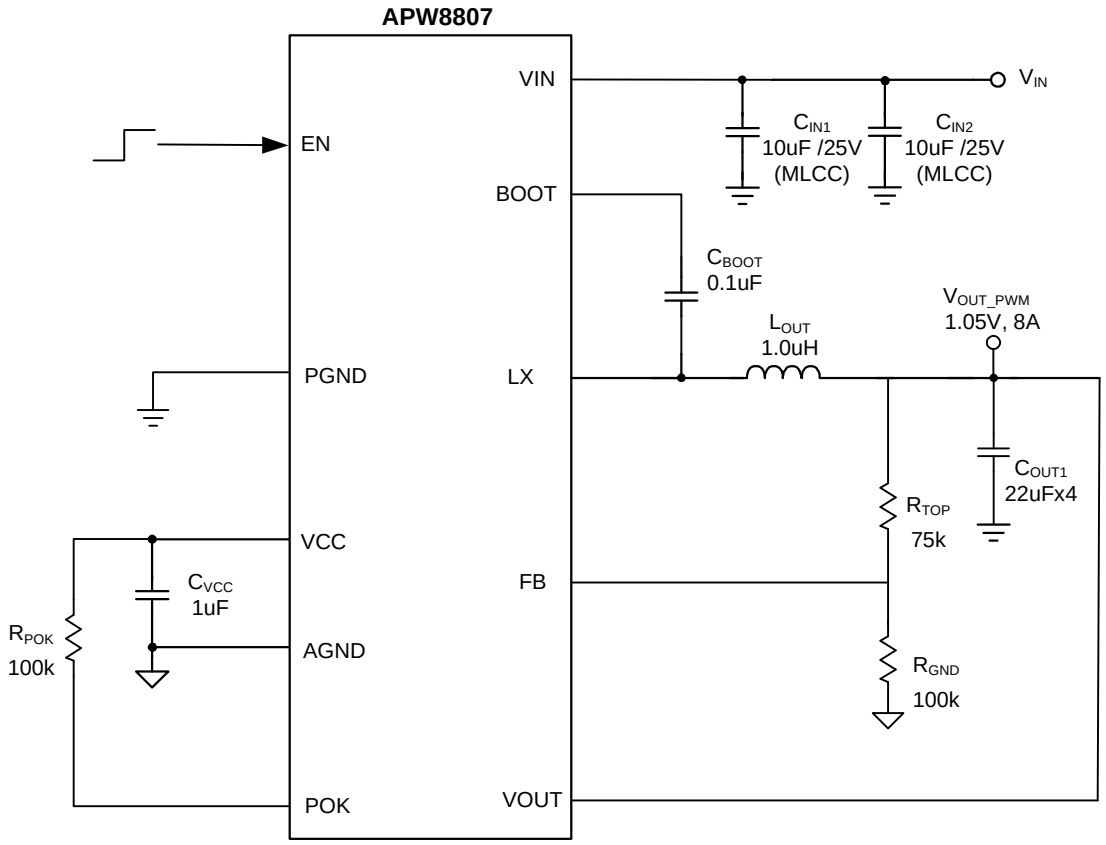
Pin Description

PIN		FUNCTION
NO.	NAME	
1	VIN	Battery voltage input pin. VIN powers linear regulators and is also used for the constant on-time PWM on-time one-shot circuits. Connect VIN to the battery input and bypass with a 1μF capacitor for noise interference.
2	PGND	Power Ground of The LGATE Low-Side MOSFET Drivers.
3, 5, 6	NC	No Connection
4	POK	Power-Good Output Pin of PWM. POK is an open-drain output used to indicate the status of the PWM output voltage. Connect the POK in to +5V through a pull-high resistor.
7	VOUT	PWM Output Voltage-Sense Input. The VOUT pin makes a direct measurement of the PWM output voltage. VOUT is an input to the constant on-time PWM one-time one-shot circuit.
8, 9,15,16	LX	Junction Point of The High-Side MOSFET Source, Output Filter Inductor and The Low-Side MOSFET Drain for PWM. Connect this pin to the Source of the high-side MOSFET. LX serves as the lower supply rail for the UGATE high-side gate driver. LX is the current-sense input for the PWM.
10	BOOT	Supply Input for The UGATE Gate Driver and an internal level-shift circuit. Connect to an external capacitor to create a boosted voltage suitable to drive a logic-level N-channel MOSFET.
11	VCC	Output for internal 5V linear regulator. It can be also connected +5V from external supply voltage for Control Circuitry. Decoupling at least 1μF of a MLCC capacitor from the VCC pin to the GND pin..
12	FB	Output voltage feedback pin (PWM). It can use a resistive divider from VOUT to GND to adjust the output from 0.6V to 5.5V.
13	EN	PWM Enable. PWM is enabled when EN=1. When EN=0, PWM is in shutdown.
14	AGND	Signal Ground for The IC.

Block Diagram



Typical Application Circuit



Function Description

Constant-On-Time PWM Controller with Input Feed-Forward

The constant on-time control architecture is a pseudo-fixed frequency with input voltage feed-forward. This architecture relies on the output filter capacitor's effective series resistance (ESR) to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal. In PFM operation, the high-side switch on-time controlled by the on-time generator is determined solely by a one-shot whose pulse width is inversely proportional to input voltage and directly proportional to output voltage. In PWM operation, the high-side switch on-time is determined by a switching frequency control circuit in the on-time generator block. The switching frequency control circuit senses the switching frequency of the high-side switch and keeps regulating it at a constant frequency in PWM mode. The design improves the frequency variation and is more outstanding than a conventional constant on-time controller, which has large switching frequency variation over input voltage, output current and temperature. Both in PFM and PWM, the on-time generator, which senses input voltage on VIN pin, provides very fast on-time response to input line transients.

Another one-shot sets a minimum off-time (typical: 300ns). The on-time one-shot is triggered if the error comparator is high, the low-side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

Pulse-Frequency Modulation (PFM) Mode

In PFM mode, an automatic switchover to pulse-frequency modulation (PFM) takes place at light loads. This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current zero crossing. This mechanism causes the threshold between PFM and PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the critical conduction point). The on-time of PFM is given by:

$$T_{ON\text{-}PFM} = \frac{1}{F_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

Where F_{SW} is the nominal switching frequency of the converter in PWM mode.

The load current at handoff from PFM to PWM mode is given by:

$$I_{LOAD(PFM\ to\ PWM)} = \frac{1}{2} \times \frac{V_{IN} - V_{OUT}}{L} \times T_{ON\text{-}PFM}$$
$$= \frac{V_{IN} - V_{OUT}}{2L} \times \frac{1}{F_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

Power-On-Reset

A Power-On-Reset (POR) function is designed to prevent wrong logic controls. The POR function continually monitors the supply voltage on the VCC pins. VCC POR circuitry inhibits wrong switching. When the rising VCC voltage reaches the rising POR threshold (4.35V typical), the PWM output voltages begin to ramp up. When the VCC voltage is lower than 4.25V(typ.), both switch power supplies are shut off. This is non-latch protection. VCC POR threshold could reset the under-voltage, over-voltage protection.

Soft Start

The APW8807 integrates soft-start circuit to ramp up the PWM output voltage of the converter to the programmed regulation set point at a predictable slew rate. The slew rate of PWM output voltage is internally controlled to limit the inrush current through the output capacitors during soft start process. When the EN pin is pulled above the rising threshold voltage, the PWM initiates a soft-start process to ramp up the output voltage. The soft-start interval is 4.8ms(typical) and independent of the switching frequency.

Enable Controls

The APW8807 has the independent enable controls for PWM part. When the EN pin is high at standby mode, the PWM initiates a soft-start process to ramp
up the output voltage. When EN1 is low, the chip is in its low-power standby state. The APW8807 only consumes 50μA of current while in standby mode.

When the EN is high, the clock signal becomes available from VCLK pin. The PWM output is discharged to low voltage by the soft stop method.Driving EN below low threshold clears the over-voltage, and under-voltage fault latches.

Function Description (Cont.)

Soft-Stop (PWM)

In the event of PWM under-voltage or shutdown, the chip enables the soft-stop function. The soft-stop function discharges the PWM output voltages to low voltage by the soft stop method. The reference remains active to provide an accurate threshold and to provide over-voltage protection.

Power Good Indicator (PWMs)

POK is actively held low in shutdown, standby, and soft-start. In the soft-start process, the POK is an open-drain output, and it is released with enable delay after the latest EN goes high (about 5.3ms typ.). In normal operation, the POK window is from 90% to its OVP threshold of the converter reference voltage. V_{OUT} has to stay within this window for POK to be high. In order to prevent false POK drop, capacitors need to parallel at the output to confine the voltage deviation with severe load step transient.

Under-Voltage Protection (PWM)

In the process of operation, if a short circuit occurs, the output voltage will drop quickly. When load current is bigger than current limit threshold value, the output voltage will fall out of the required regulation range. The under-voltage continually monitors the setting output voltage after soft-start is completed. If a load step is strong enough to pull the output voltage lower than the under-voltage threshold for at least 2µs, the PWM controller starts a soft-stop process to shut down the output gradually and latched off when the soft-stop process is completed.

The under-voltage threshold is 60% of the nominal output voltage. Under-voltage protection is ignored for at least 5.3ms (typical) after a rising edge on EN. Re-toggling EN signal will clear the latch and bring the chip back to operation.

Over Voltage Protection (OVP)

Should the output voltage of VOUT increase over 20% of the setting voltage due to the high-side MOSFET failure or for other reasons, the over voltage protection will active. Over voltage protection will force the low-side MOSFET gate driver turns on. This action actively pulls down the output voltage. When the OVP occurs, the POK pin will pull down and latch-off the converter. This OVP scheme only clamps the voltage overshoot, and does not invert the output voltage when otherwise activated with a continuously high output from low-side MOSFET driver. It?s a common problem for OVP schemes with a latch. Once an over-voltage fault condition is set, it can be reset by re-toggling EN signal.

Over-Temperature Protection

When the junction temperature increases above the rising threshold temperature 150°C, the IC will enter the over temperature protection (OTP). When the OTP occurs, PWM controller circuitry shuts down. It is non-latch protection.

Current Limit (PWM)

The current limit circuit employs a "valley" current-sensing algorithm (See Figure 1). The APW8807 uses the low-side MOSFET's $R_{DS(ON)}$ of the synchronous rectifier as a current-sensing element. If the magnitude of the current-sense signal at LX pin is above the current-limit threshold, the PWM is not allowed to initiate a new cycle. The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the sense resistance, inductor value, and input voltage.

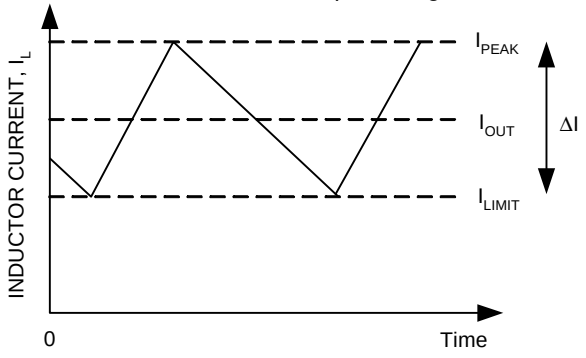


Figure 1. Current-Limit Algorithm

Function Description (Cont.)

PWM controller use the low-side MOSFETs on-resistance $R_{DS(ON)}$ to monitor the current for protection against shorted outputs. The MOSFET's $R_{DS(ON)}$ is varied by temperature and gate to source voltage.

The current Limit threshold of APW8807 is fixed 10A (Minimum).

The PCB layout guidelines should ensure that noise and DC errors do not corrupt the current-sense signals at LX. When combined with the under-voltage protection circuit, this current-limit method is effective in almost every circumstance.

Application Information

Output Voltage Selection

The output voltage of PWM can be adjusted from 0.6V to 5.5V with a resistor-driver at FB between VOUT and GND. Using 1% or better resistors for the resistive divider is recommended. The FB pin is the inverter input of the error amplifier, and the reference voltage is 0.6V. Take the example, the output voltage of PWM is determined by:

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_{TOP}}{R_{GND}}\right)$$

Where R_{TOP} is the resistor connected from V_{OUT} to V_{FB} and R_{GND} is the resistor connected from FB to GND.

Output Inductor Selection

The duty cycle of a buck converter is the function of the input voltage and output voltage. Once an output voltage is fixed, it can be written as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

The inductor value determines the inductor ripple current and affects the load transient reponse. Higher inductor value reduces the inductor's ripple current and induces lower output ripple voltage. The ripple current can be approxminated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{F_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Where F_{SW} is the switching frequency of the regulator. Increasing the inductor value and frequency will reduce the ripple current and voltage. However, there is a tradeoff between the inductor's ripple current and the regulator load transient response time.

A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current. Increasing the switching frequency (F_{SW}) also reduces the ripple current and voltage, but it will increase the switching loss of the MOSFETs and the power dissipation of the converter. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current. Once the inductance value has been chosen, selecting an inductor is capable of carrying the required peak current without going into saturation. This will be result in a larger output ripple voltage.

Output Capacitor Selection

Output voltage ripple and the transient voltage deviation are factors that have to be taken into consideration when selecting an output capacitor. Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore, selecting high performance low ESR capacitors is intended for switching regulator applications. In addition to high frequency noise related MOSFET turn-on and turn-off, the output voltage ripple includes the capacitance voltage drop and ESR voltage drop caused by the AC peak-to-peak current. These two voltages can be represented by:

$$\Delta V_{COUT} = \frac{I_{RIPPLE}}{8 C_{OUT} F_{SW}}$$

$$\Delta V_{ESR} = I_{RIPPLE} \times R_{ESR}$$

These two components constitute a large portion of the total output voltage ripple. In some applications, multiple capacitors have to be paralleled to achieve the desired ESR value. If the output of the converter has to support another load with high pulsating current, more capacitors are needed in order to reduce the equivalent ESR and suppress the voltage ripple to a tolerable level. A small decoupling capacitor in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors must also be considered.

To support a load transient that is faster than the switching frequency, more capacitors have to be used to reduce the voltage excursion during load step change. Another aspect of the capacitor selection is that the total AC current going through the capacitors has to be less than the rated RMS current specified on the capacitors to prevent the capacitor from over-heating.

Application Information (Cont.)

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, select the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage. The maximum RMS current rating requirement is approximately $I_{OUT}/2$, where I_{OUT} is the load current. During power up, the input capacitors have to handle large amount of surge current. In low-duty notebook appliactions, ceramic capacitors are remmended. The capacitors must be connected between the drain of high-side MOSFET and the source of low-side MOSFET with very low-impeadance PCB layout.

Layout Consideration

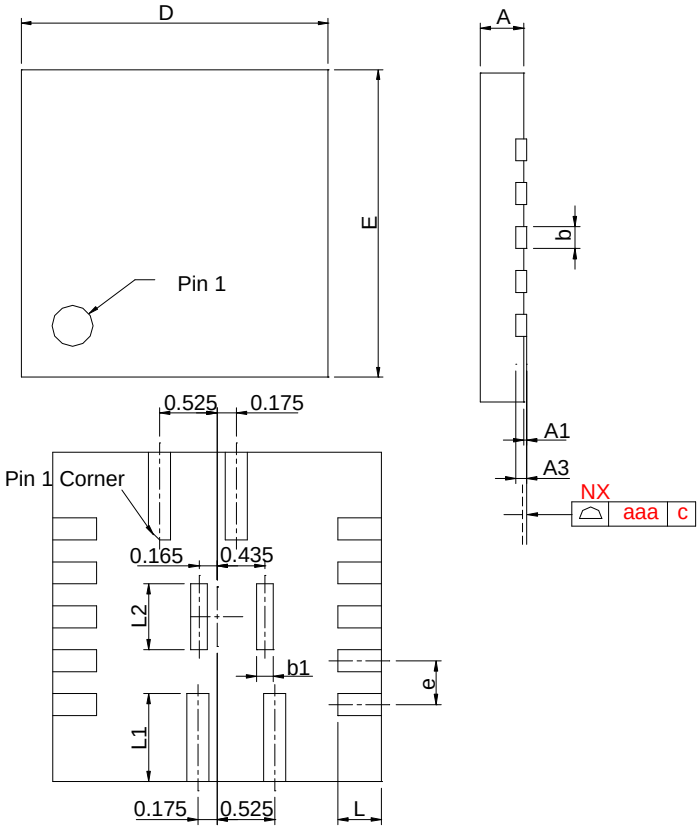
In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator. With power devices switching at higher frequency, the resulting current transient will cause voltage spike across the interconnecting impedance and parasitic circuit elements. As an example, consider the turn-off transition of the PWM MOSFET. Before turn-off condition, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is freewheeling by the lower MOSFET and parasitic diode. Any parasitic inductance of the circuit generates a large voltage spike during the switching interval. In general, using short and wide printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike. And signal and power grounds are to be kept separating and finally combined to use the ground plane construction or single point grounding. The best tie-point between the signal ground and the power ground is at the negative side of the output capacitor on each channel, where there is less noise. Noisy traces beneath the IC are not recommended. Below is a checklist for your layout:

Layout Consideration (Cont.)

- Keep the switching nodes LX and BOOT away from sensitive small signal nodes since these nodes are fast moving signals. Therefore, keep traces to these nodes as short as possible and there should be no other weak signal traces in parallel with theses traces on any layer.
- Decoupling capacitor, boot capacitors, should be close to their pins.
- The input capacitor should be near the VIN pin; the high quality ceramic decoupling capacitor can be put close to the VCC and GND pins; the output capacitor should be near the loads. The input capacitor GND should be close to the output capacitor GND and GND pin.

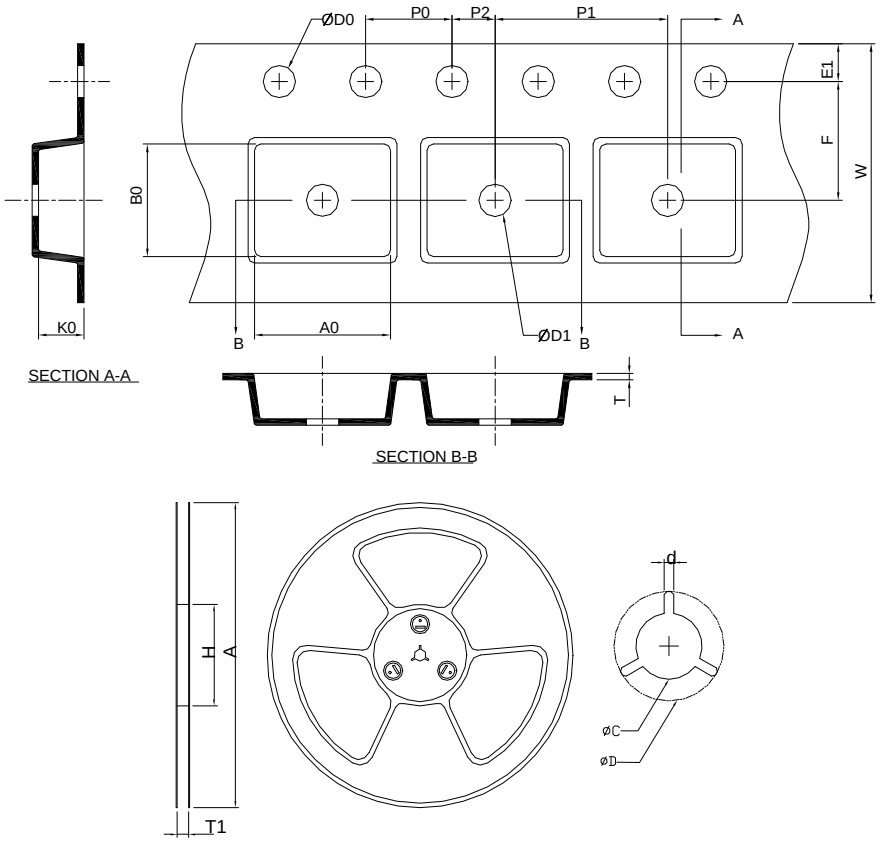
Package Information

TQFN3x3-16A



SYMBOL	TQFN3x3-16A			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.15	0.25	0.006	0.010
b1	0.10	0.20	0.004	0.008
D	2.90	3.10	0.114	0.122
E	2.90	3.10	0.114	0.122
e	0.40 BSC		0.016 BSC	
L	0.35	0.45	0.014	0.018
L1	0.75	0.85	0.030	0.033
L2	0.55	0.65	0.022	0.026
aaa	0.08		0.003	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN3x3-16A	330±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.00±0.20

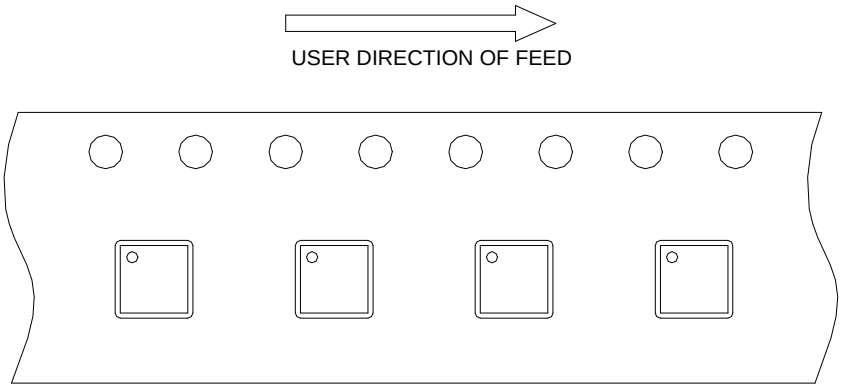
(mm)

Devices Per Unit

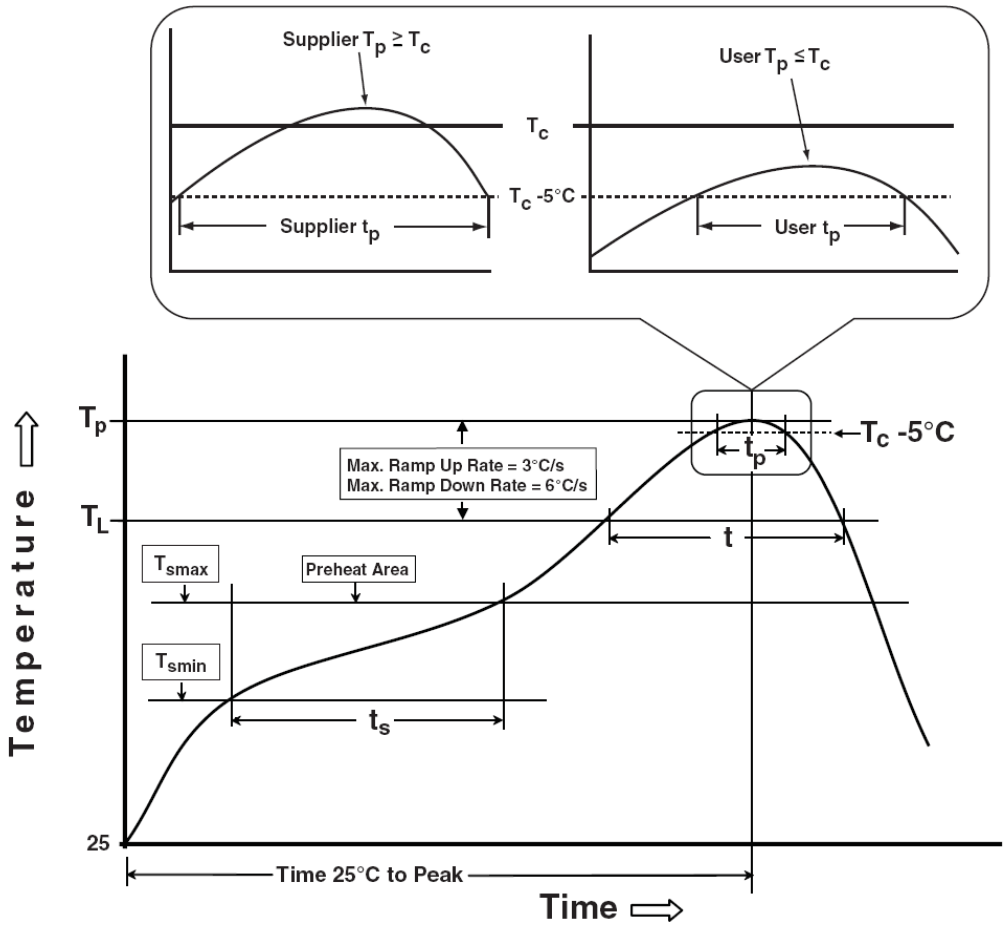
Package Type	Unit	Quantity
TQFN3x3-16A	Tape & Reel	3000

Taping Direction Information

TQFN3x3-16A



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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