300mA ULTRA LOW DROPOUT POSITIVE ADJUSTABLE AND FIXED REGULATORS

FEATURES

- SOT-23 Package
- Stable with 2.2μF Ceramic Capacitor
- 1% Voltage Reference Accuracy
- Only 270mV Dropout at 300mA and 170mV Dropout at 150mA
- 5μA Quiescent Current in Shutdown
- Current Limit and Thermal Shutdown
- Logic Input Enable Pin
- RoHS Compliant

APPLICATIONS

- Laptop, Notebook & Palmtop computers
- Battery Powered Equipments
- PCMCIA Vcc & Vpp Regulator
- Consumer Electronics
- High Efficiency Linear Power Supplies

DESCRIPTION

The APU1205 device is an efficient linear voltage regulator with better than 1% initial voltage accuracy, very low dropout voltage and very low ground current designed especially for hand held, battery powered applications. Other features of the device are: TTL compatible enable/shutdown control input, current limiting and thermal shutdown.

The APU1205 is available in fixed and adjustable output voltage versions in a small SOT-23 5-Pin package.

TYPICAL APPLICATION

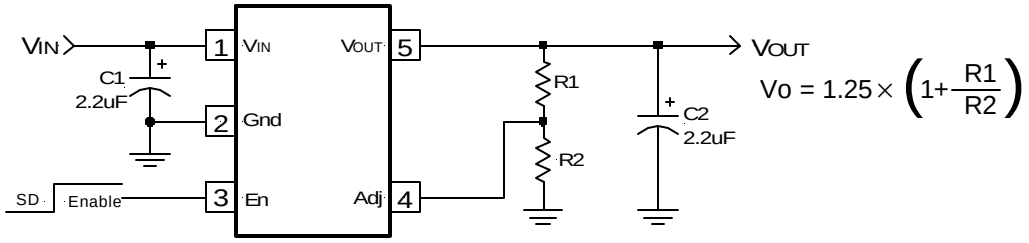


Figure 1 - Typical application of the APU1205 ajustable voltage regulator.

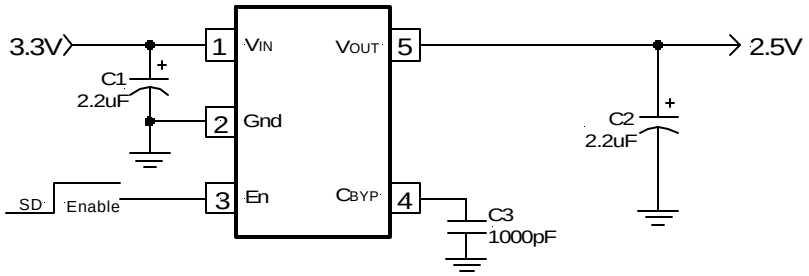


Figure 2 - Typical application of the APU1205-25 fixed voltage regulator.

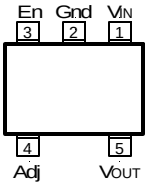
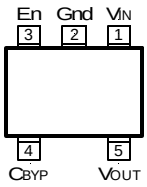
PACKAGE ORDER INFORMATION

TJ (°C)	5-PIN SOT-23	OUTPUT VOLTAGE
0 To 125	APU1205Y5	Adj
0 To 125	APU1205Y5-18	1.8V
0 To 125	APU1205Y5-25	2.5V
0 To 125	APU1205Y5-28	2.8V
0 To 125	APU1205Y5-30	3.0V
0 To 125	APU1205Y5-33	3.3V
0 To 125	APU1205Y5-36	3.6V

ABSOLUTE MAXIMUM RATINGS

Input Voltage (V_{IN}) 10V
Enable Input Voltage 10V
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 150°C

PACKAGE INFORMATION

5-PIN SOT-23 (Y5)	5-PIN SOT-23 (Y5)
 Adjustable θ_{JA}=256°C/W	 Fixed θ_{JA}=256°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over C_{IN}=Co=22µF, Io=100µA, $V_{IN(MIN)}$=2.5V(Adjustable devices) V_{IN}=Vo + 1V(for fixed voltage devices), V_{OUT}=V_{FB}(for adjustable version only), C_{BYP}=470pF(for fixed voltage devices), VENB=2V and T_A=25°C. Typical values refer to T_A=25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Reference Voltage	Vo		-1		1	%
(See Table 1 for typical values)		(Note 4)	-2		2	
Line Regulation	ΔV_I	Vo + 1V<V_{IN}<10V		0.005		%/V
Load Regulation (Note 1)	ΔV_L	1mA<Io<100mA		0.8		%
		100mA<Io<300mA		0.1		
Dropout Voltage (Note 2)	$\Delta V_{I(O)}$	Io=100µA		10	50	mV
		Io=100µA (Note 4)		13	70	
		Io=50mA		85	110	
		Io=50mA (Note 4)		100	140	
		Io=150mA		170	220	
		Io=150mA (Note 4)		204	260	
		Io=300mA		270	350	
		Io=300mA (Note 4)		324	400	
Ground Current (Note 3)	I_Q	V_{EN}=2V, Io=100µA		120	160	µA
		Io=100µA (Note 4)		240		
		Io=50mA		420	600	
		Io=50mA (Note 4)		540		
		Io=150mA		2200	2900	
		Io=150mA (Note 4)		2900		
		Io=300mA		7200	9500	
		Io=300mA (Note 4)		9300		
Ground Current-SD Activated	$I_{Q(SD)}$	V_{EN}=0V to 0.8V or Open		5		µA
Current Limit	I_{CL}	Vo=0V	320	420		mA
Thermal Regulation	ΔV_P	V_{IN}=10V, Io=150mA, 10ms Pulse		0.05		%/W
Adjust Pin Current	I_{ADJ}	V_{IN}=2.5V, Vo=V_{ADJ}		0.1		µA
Enable Pin Input LO Voltage	$V_{EN(L)}$	Regulator OFF			0.8	V
Enable Pin Input HI Voltage	$V_{EN(H)}$	Regulator ON	2			V
Enable Pin Input LO Current		$V_{EN(L)}$=0V to 0.8V		0.01		µA
Enable Pin Input HI Current		$V_{EN(H)}$=2V to V_{IN}		20		µA

Note 1: Low duty cycle pulse testing with Kelvin connections is required in order to maintain accurate data.

Note 2: Dropout voltage is defined as the minimum differential voltage between V_{IN} and V_{OUT} required to maintain regulation at V_{OUT}. It is measured when the output voltage drops 1% below its nominal value.

Note 3: Ground current is the regulator quiescent current plus the pass transistor current. The total current from the supply is the sum of the load current plus the ground pin current.

Note 4: The specification applies for the junction temperature of 0 to +125°C.

PIN DESCRIPTIONS

PIN #	PIN SYMBOL	PIN DESCRIPTION
1	V_{IN}	The input pin of the regulator. Typically a large storage capacitor is connected from this pin to ground to insure that the input voltage does not sag below the minimum drop out voltage during the load transient response. This pin must always be higher than V_{OUT} by at least the amount of the dropout voltage and some margin in order for the device to regulate properly.
2	Gnd	Ground pin. This pin must be connected to the lowest potential in the system and all other pins must be at higher potential with respect to this pin.
3	En	Enable pin. A low signal or left open on this pin shuts down the output. This pin must be tied HI or to V_{IN} for normal operation.
4	Adj (Adjustable Only)	A resistor divider from this pin to the V_{OUT} pin and ground sets the output voltage. To minimize the error due to the error amplifier, select the values of the resistor dividers to be less than 10KΩ.
4	C_{BYP} (Fixed Only)	A 470 to 1000pF bypass capacitor connected to this pin reduces the output noise.
5	V_{OUT}	The output of the regulator. A minimum of 2.2μF with max ESR of 1Ω capacitor must be connected from this pin to ground to insure stability.

5-PIN SOT-23	Output Voltage
APU1205	1.25V
APU1205-18	1.8V
APU1205-25	2.5V
APU1205-28	2.8V
APU1205-30	3.0V
APU1205-33	3.3V
APU1205-36	3.6V

Table 1- Nominal output voltage vs. part number.

The output voltage of the adjustable device can be set using:

$$Vo = 1.25 \times \left(1 + \frac{R1}{R2}\right)$$

Where:
R1 = Resistor connected from output to the Adj pin
R2 = Resistor connected from Adj pin to Gnd

BLOCK DIAGRAM

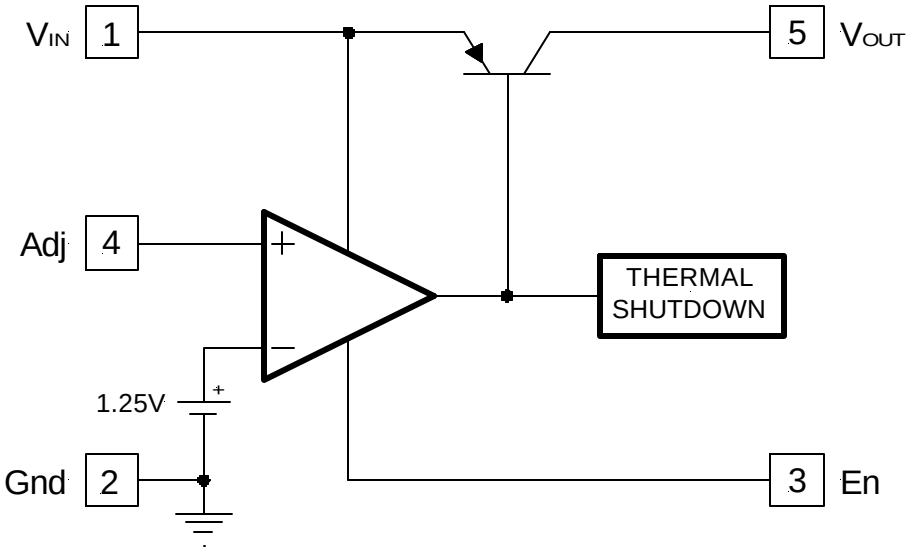


Figure 3 - APU1205 Adjustable output block diagram.

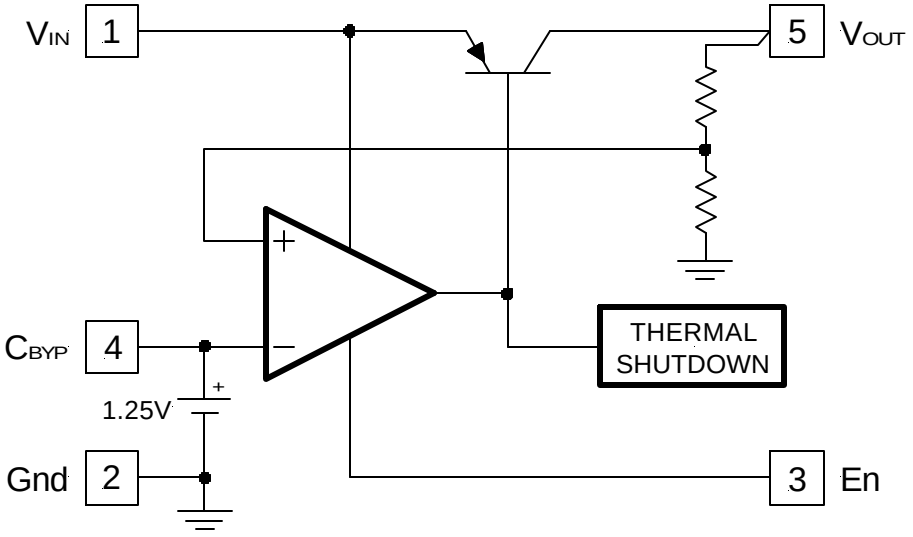


Figure 4 - APU1205-18, APU1205-25, APU1205-28, APU1205-30, APU1205-33 and APU1205-36 Fixed output block diagram.