NEW PRODUCT

Description

The APR347 is a secondary side MOSFET driver for synchronous rectification in DCM operation.

The synchronous rectification can effectively reduce the secondary side rectifier power dissipation and provide high performance solution. By sensing primary MOSFET gate-to-source voltage, the APR347 can output ideal drive signal with less external components. It can provide high performance solution for 3.3V to 15V output voltage application.

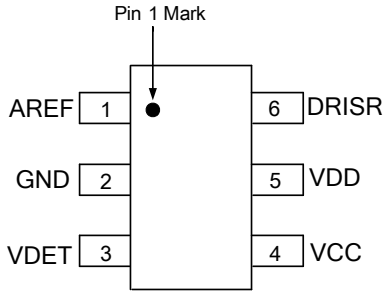
The APR347 is available in SOT26 package.

Features

- Synchronous Rectification for DCM Operation Flyback
- Eliminate Resonant Ring Interference
- Fewest External Components
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Pin Assignments

(Top View)



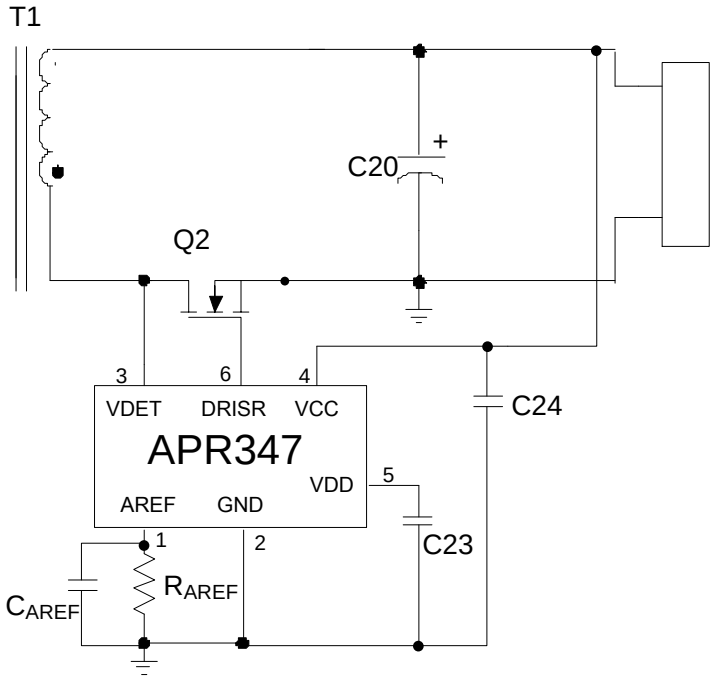
SOT26

Applications

- Adapters/Chargers for Cell/Cordless Phones, ADSL Modems, MP3 and Other Portable Apparatus

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit



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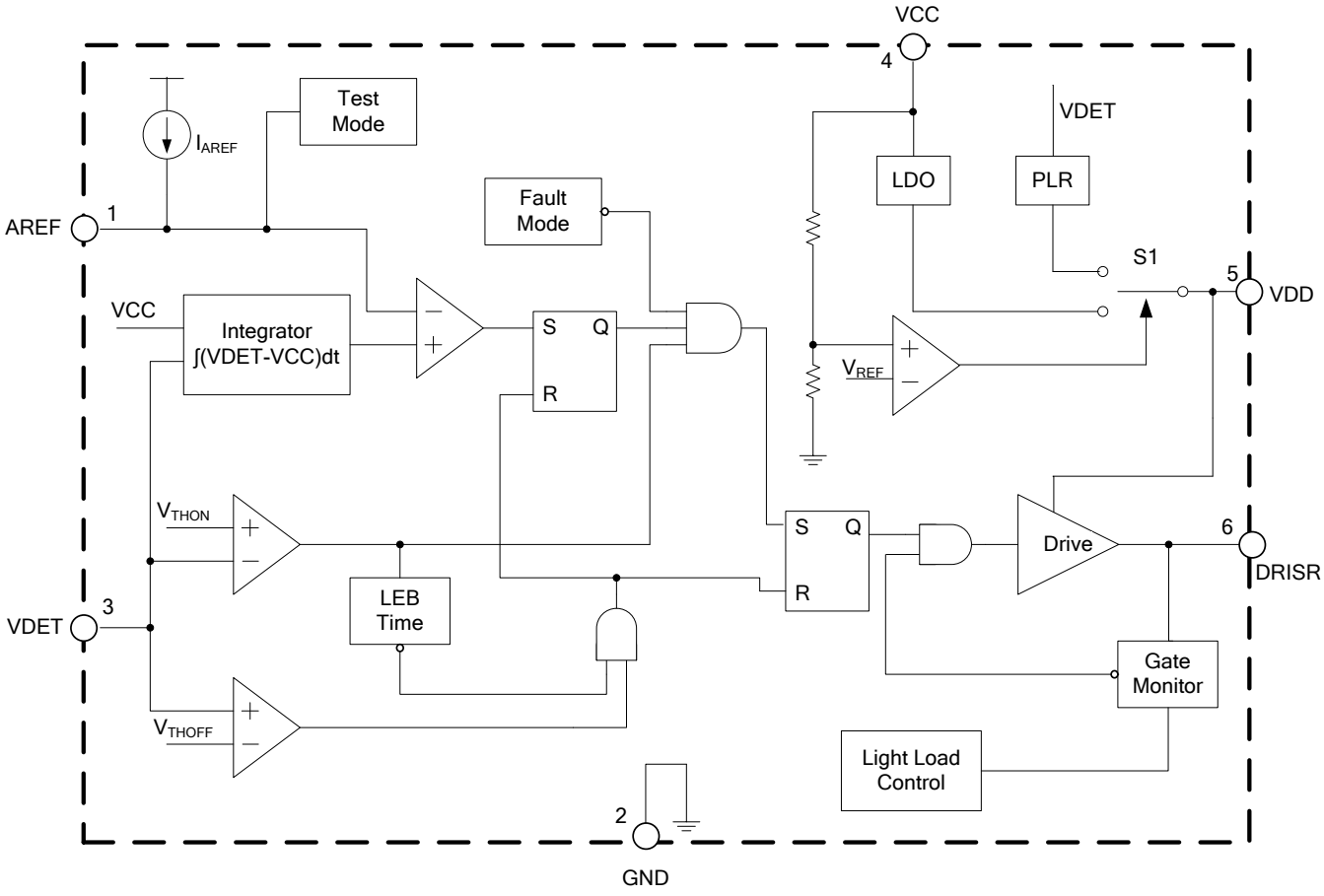
Pin Descriptions

Pin Number	Pin Name	Function
1	AREF	Program a voltage reference with a resistor from AREF to GND, to enable synchronous rectification MOSFET drive signal
2	GND	Ground
3	VDET	SR MOS drain-to-source voltage sense input, connected to drain pin of SR MOSFET through a resistor
4	VCC	Power supply, connected with system output Input of internal LDO and system output voltage sensing circuit.
5	VDD	Internal power supply. It provides bias voltage for the internal logic circuit and the MOSFET driver. Connect this pin to a capacitor.
6	DRISR	Synchronous rectification MOSFET Gate drive

Functional Block Diagram



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Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating	Unit
V_{CC}	Supply Voltage	-0.3 to 28	V
V_{DET}	Voltage at VDET Pin (Note 5)	-0.7 to 150	V
V_{DRISR}	Voltage at DRISR Pin	-0.3 to 7	V
V_{DD}	Internal Power Supply Voltage	-0.3 to 7.5	V
P_D	Power Dissipation at T_A = +25°C	0.6	W
T_J	Operating Junction Temperature	+150	°C
T_{STG}	Storage Temperature	-65 to +150	°C
T_{LEAD}	Lead Temperature (Soldering, 10s)	+300	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	197	°C/W
θ_{JC}	Thermal Resistance (Junction to Case)	76	°C/W

Notes: 4. Stresses greater than those listed under "*Absolute Maximum Ratings*" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "*Recommended Operating Conditions*" is not implied. Exposure to "*Absolute Maximum Ratings*" for extended periods may affect device reliability.

5. VDET pin is ESD sensitive and passes 1000V HBM. The JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	0	16	V
T_A	Ambient Temperature	-40	+85	°C

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Electrical Characteristics (@V_{CC} = 5V, T_A = -40°C <T_A<+85°C, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Supply Voltage (VCC Pin)						
$I_{STARTUP}$	Startup Current	V_{CC} = $V_{STARTUP}$-0.1V	–	150	–	μA
I_{OP}	Operating Current	VDET Pin Floating V_{CC} = 5V	–	150	–	μA
$V_{STARTUP}$	Startup Voltage	–	–	2.4	–	V
–	UVLO	–	–	2.2	–	V
V_{DD_ENABLE}	VDD Enable Falling Threshold at VCC Pin	–	–	4.6	–	V
$V_{DD\_DISABLE}$	VDD Disable Rising Threshold at VCC Pin	–	–	4.75	–	V
V_{DD_HYS}	VDD Disable Hysteresis at VIN Pin	–	–	150	–	mV
VDD Pin						
V_{DD}	Internal Power Supply Voltage	–	–	5.5	–	V
Gate Driver						
V_{THON}	Gate Turn On Threshold	–	0	–	1	V
V_{THOFF}	Gate Turn Off Threshold	–	–	-5	–	mV
t_{DON}	Turn On Delay Time	From V_{THON} to V_{DRISR} = 1V	–	70	180	ns
t_{DOFF}	Turn Off Propagation Delay Time	From V_{THOFF} to V_{DRISR} = 4V	–	100	150	ns
t_{RG}	Turn On Rising Time	From 1V to 4V, V_{CC}=5V, C_L=4.7nF	–	50	100	ns
t_{FG}	Turn Off Falling Time	From 4V to 1V, V_{CC}=5V, C_L=4.7nF	–	20	100	ns
t_{ON_MIN}	Minimum On Time	–	1.2	1.6	2	μs
t_{OFF_MIN}	Minimum Off Time	–	–	2	–	μs
V_{DRISR}	SR Drive Voltage	V_{CC}<4.6V	–	–	V_{DD}-0.1	V
		V_{CC} >4.75V	–	–	V_{CC}-0.1	
K_{QS}	(Note 6)	–	–	0.42	–	mA*μs
V_{S_MIN}	Synchronous Rectification (SR) Minimum Operating Voltage (Note 7)	–	–	–	4.5	V
Green Mode (Note 8)						
t_{LL}	Minimum Off Time to Enter Green Mode	–	–	600	–	μs

Notes: 6. This item is used to specify the value of R_{AREF}.
7. This item specifies the minimum SR operating voltage of V_{IN_DC}, $V_{IN\_DC} \geq N_{PS} * V_{S\_MIN}$.
8. These parameters are guaranteed by design and characterization.

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Synchronous Rectification Principle Description

SR MOSFET Turn on

The APR347 determines the synchronous rectification MOSFET turn-on time by monitoring the MOSFET drain-to-source voltage. When the drain voltage is lower than the turn-on threshold voltage V_{THON}, the IC outputs a positive drive voltage after a turn-on delay time (t_{DON}). The MOSFET will turn on and the current will transfer from the body diode into the MOSFET's channel. Since of parasitic parameter, the voltage on MOSFET drain pin has moderate voltage ringing at this moment, which maybe impact on the sense of VDET voltage and resulting in the turning-off fault. To avoid fault situation happening, a Minimum On-Time (t_{ONMIN}) blanking period is used to maintain the power MOSFET on for a minimum amount of time.

In Figure 1, the turn on blanking time t_{ONMIN} is to prevent the MOSFET drain-to-source voltage ringing affect.

Turn off Operation

The DCM operation of the SR is described with timing diagram shown in Figure 1.

In the process of drain current decreasing linearly toward zero, the drain-source voltage rises synchronically. When it rises over the turn off threshold voltage V_{THOFF}, the APR347 pulls the drive signal down after a turn-off delay (t_{DOFF}).

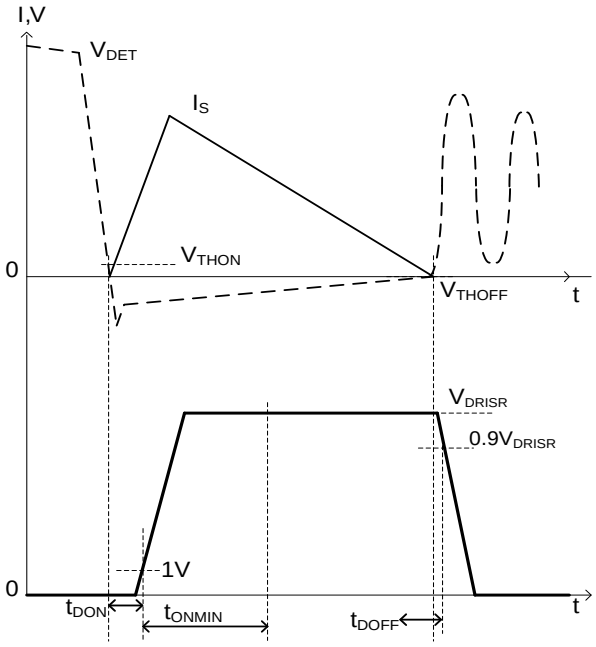

Figure 1. Typical Waveforms of APR347 in DCM

Minimum On/Off Time

When the controlled MOSFET gate is turned on, some ringing noise is generated. The minimum on-time timer blanks the V_{THOFF} comparator, keeping the controlled MOSFET on for at least the minimum on time. During the minimum on time, the turn off threshold is totally blanked.

After the SR driver turns off, the SR control block initiates a minimum off time timer during which the SR will remain off to avoid the ringing from turning on the synchronous MOSFET.

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Synchronous Rectification Principle Description (continued)

The Value and Meaning of AREF Resistor

As to DCM operation flyback converter, after the secondary rectifier stops conducting, the primary MOSFET Drain-to-source ringing waveform is resulted from the resonant of primary inductance and output capacitance of equivalent switch device. This ringing waveform probably leads to Synchronous Rectifier error conduction. To avoid this fault happening, the APR347 has a special function design by means of volt-second product detecting. Regarding of the sensed voltage of VDET pin, the volt-second product of voltage above V_{CC} at primary switch on time is much higher than that of each cycle ringing voltage above V_{CC}. Therefore, before every time Synchronous Rectifier turns on, the APR347 judges if the detected volt-second product of VDET voltage above V_{CC} is higher than a threshold, and then turn on synchronous Rectifier. The purpose of AREF resistor is to determine the volt-second product threshold. The APR347 has a parameter, Kqs, which converts R_{AREF} value to volt-second product.

$$Area2 = R_{AREF} * Kqs$$

In general, the Area1 and Area3 values depend on the system design and always are fixed if the system design is frozen. As to Diodes PSR design, the Area1 value changes with primary peak current value and Area3 value generally keeps constant at all of conditions. So the AREF resistor design should consider the worst case, the minimum primary peak current condition. Since of system design parameter distribution, Area1 and Area3 have moderate tolerance. So Area2 should be designed in the middle of Area1 and Area3 to ensure enough design margins.

$$Area3 < R_{AREF} * Kqs < Area1$$

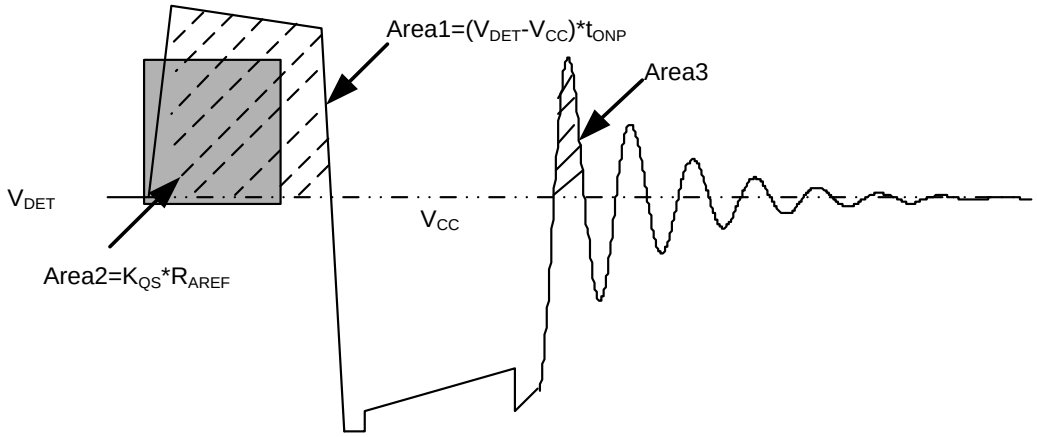

Figure 2. AREF Function

SR Minimum Operating Voltage

The APR347 sets a minimum SR operating voltage by comparing the difference between V_{DET} and output voltage (V_{CC}). The value of V_{DET}–V_{CC} must be higher than its internal reference, then the APR347 will begin to integrate the area of (V_{DET}–V_{CC})*t_{ONP}. If not, the area integrating will not begin and the SR driver will be disabled.

Recommended Application Circuit Parameters

The C_{AREF} is suggested to be parallel with the AREF resistor to keep the volt-second product threshold stable. And the recommended value of C_{AREF} is 20nF.

The recommended value of C24 is 100nF. The value of V_{DD} capacitor C23 is 4.7μF.

Green Mode at Light Load

When the system is running with light load, rectifier conduction loss no longer dominates the secondary-side power loss, in which condition it is preferred the SR MOSFET keeps off to save the driver loss.

The APR347 will sense the non-switching duration cycle by cycle, when the non-switching duration keeps longer than the internal light load timing t_{LL}, the IC will shutdown the gate driver and keeps it off for the next two cycles.

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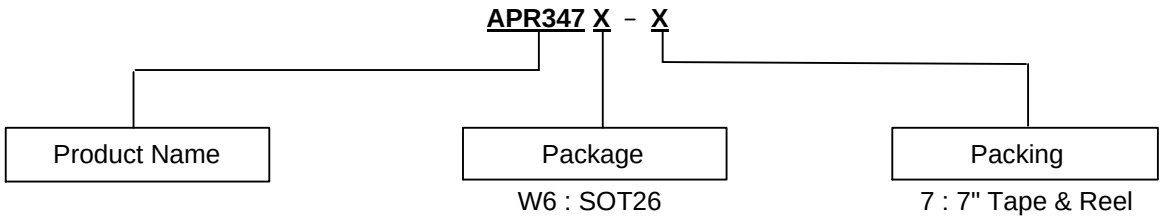
Synchronous Rectification Principle Description (continued)

V_{DD}

The V_{DD} is the output voltage of Pulse Linear Regulator (PLR) or the Low Dropout Regulator (LDO). It provides bias voltage for the controller. A capacitor (typical 4.7μF) should be connected between the VDD pin and GND pin.

A Pulse Linear Regulator is integrated in the controller to provide voltage to the VDD pin of APR347. With the PLR, the APR347 can operate at a low voltage output condition, in which the system output voltage may drop to as low as 2V. The bias voltage will change from the PLR to the LDO, when the system output voltage is higher than 4.75V. In that case the system output provides voltage to VDD of APR347 through the internal LDO.

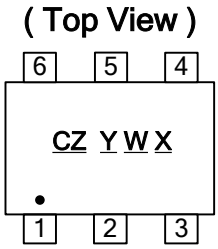
Ordering Information



Package	Temperature Range	Part Number	Marking ID	7"Tape and Reel	
				Quantity	Part Number Suffix
SOT26	-40°C to +85°C	APR347W6-7	CZ	3000/Tape and Reel	-7

Marking Information

(1) SOT26



XX : Identification Code
Y : Year 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents 52 and 53 week
X : Internal Code

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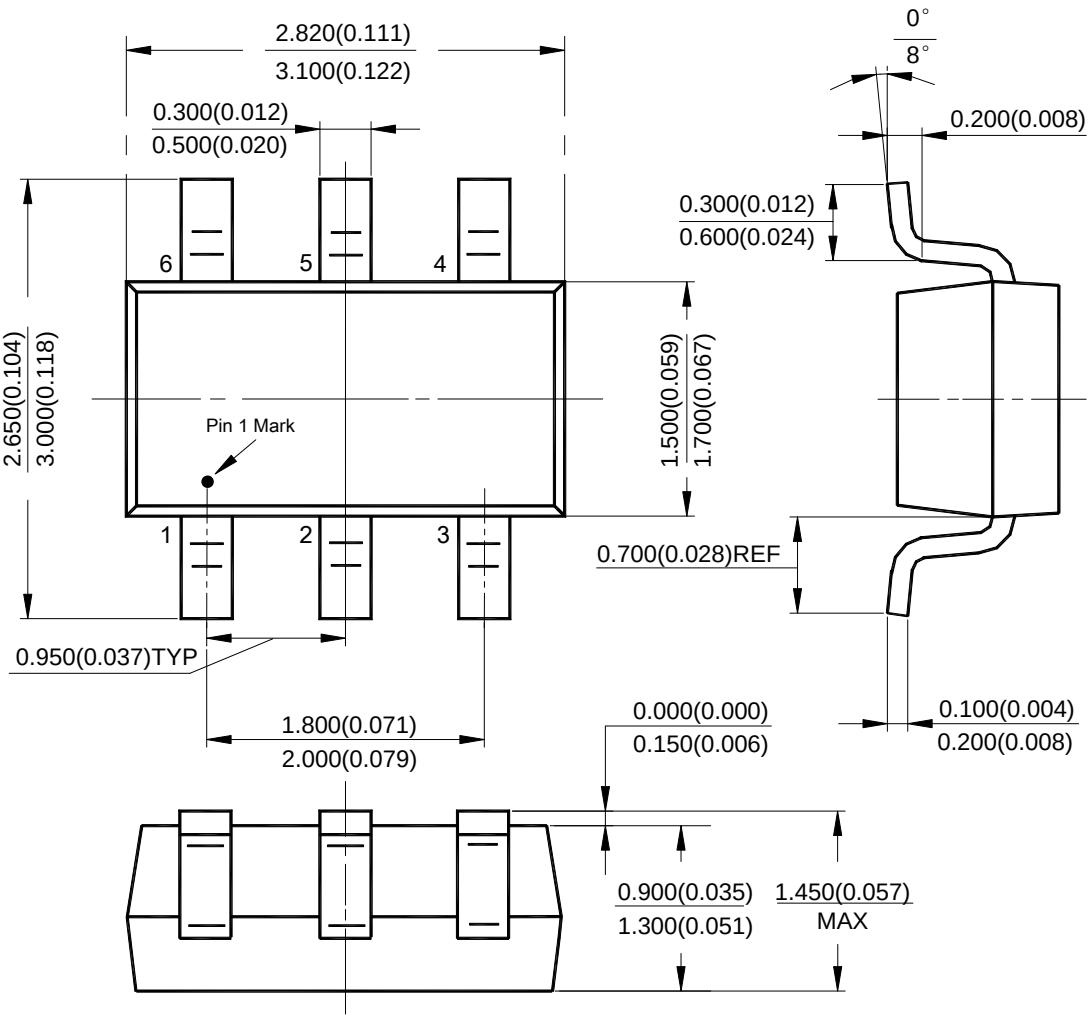
Package Outline Dimensions (All dimensions in mm (inch).)

(1) Package Type: SOT26



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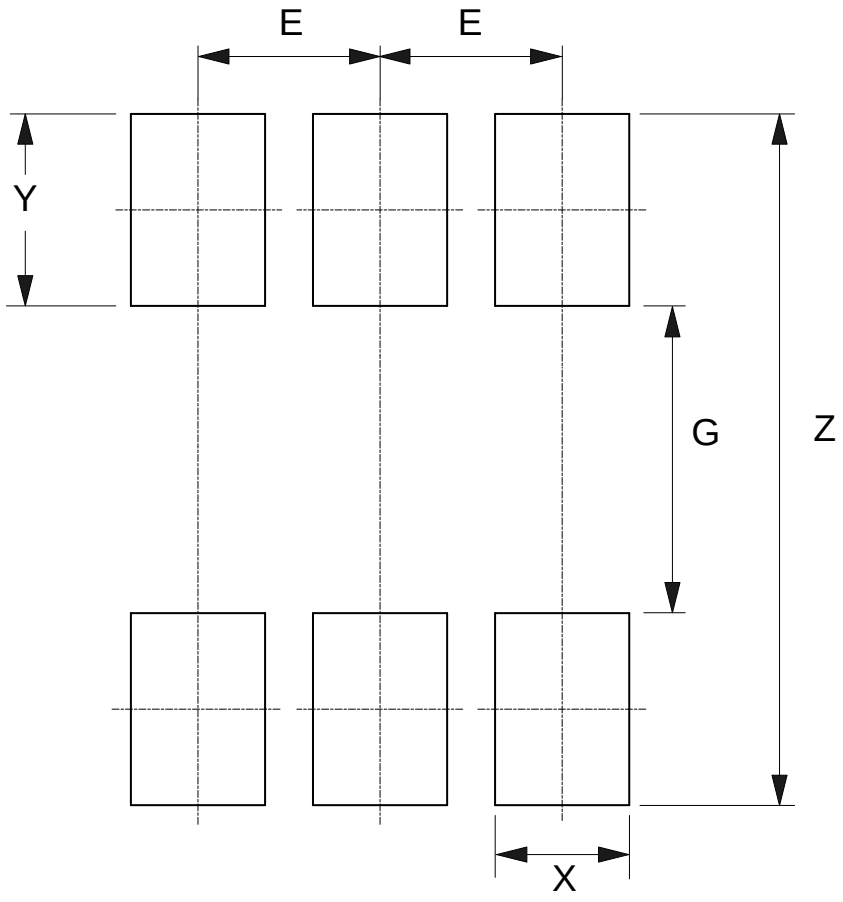
Suggested Pad Layout

(1) Package Type: SOT26



Dimensions	Z (mm)/(inch)	G (mm)/(inch)	X (mm)/(inch)	Y (mm)/(inch)	E (mm)/(inch)
Value	3.600/0.142	1.600/0.063	0.700/0.028	1.000/0.039	0.950/0.037

NEW PRODUCT

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