Datasheet

APM32F035x8/M3514x8

Arm® Cortex®-M0+ based 32-bit MCU

Version: Draft V0.10

1 Product Characteristics

Core

- 32-bit Arm® Cortex®-M0+Core
- Up to 72MHz working frequency, Support single-cycle 32-bit hardware multiplier
- M0CP coprocessor, its hardware includes: shift unit, 32bit/32bit divider, optional multiply and add operation with saturation, square root (register form), trigonometric function, SVPWM (phase shift function is realized by software)

Memory

- Flash：64KB
- SRAM：10KB (8KB+2KB Coprocessor dedicated space)

Clock

- HSECLK: 4~32MHz Crystal oscillator
- LSECLK: 32KHz RTC oscillator with calibration (only F035 supported)
- HSICLK: Internal 8MHz RC oscillator
- HSICLK14: Internal 14MHz RC oscillator
- LSICLK: Internal 40KHz RC oscillator
- PLL: Phase-locked loop, supports 2~16 frequency doubling

Power and Power Management

- Digital supply voltage: V_{DD}=2.0~3.6V
- Analog supply voltage: V_{DDA}=V_{DD}~3.6V
- Power-on/ Power-down reset (POR/PDR)

Low Power Consumption Mode

- Sleep, Stop and S tandby mode

I/O

- F035: up to 42 I/Os
- M3514: up to 29 I/Os
- All I/Os are mappable to external interrupt vectors
- F035: Up to 39 I/Os with 5V input tolerance
- M3514: Up to 39 I/Os with 5V input tolerance

DMA

- One 7-channel DMA controller

Analog Peripherals

- One 12-bit ADC, support programmable conversion resolution and improve conversion rate supporting up to 16 external channels (M3514 is up to 13 external channels), with conversion range of 0~3.6V, independent analog power supply: V_{DDA}=2.4~3.6V
- Two programmable analog comparators
- Up to four universal operational amplifiers, which can adjust the gain of the operational amplifier through external resistance, or select the internal preset gain gear through setting. The conversion rate is up to 10v/us, and the gain bandwidth product is up to 10MHz
- One temperature sensor

RTC

- Support calendar function
- Alarm and regular wake-up from stop/standby mode

Timer

- One 16-bit advanced control timer which can provide up to 7 channels of PWM output, six channels realize complementary PWM output, support braking function, and support interaction with M0CP coprocessor
- One 32-bit general timer (TMR2) and two 16-bit general timers (TMR3/4)
- Two 16-bit basic timers (TMR6/7)
- Two watchdog timers: one independent watchdog IWDT and one window watchdog WWDT
- One 24-bit self-reducing system tick timer
- Support infrared reception function for remote control

Communication Interface

- One I2C interface
- Two U(S)ART interfaces, support full duplex communication
- One SPI interfaces (18Mbit/s), support I2S interface multiplexing
- One CAN interface

Integrated driver（only M3514 supported）

- 6N 200V Gate Driver
- 3.3V LDO, input voltage: 5V~20V

CRC Calculation Unit

- 8/16/32bit CRC calculation result

BootLoader: support USART upgrade

Serial line debugging (SWD)

Chip security

- 96-Bit UID
- Flash supports read and write protection

Package

- F035: LQFP48
- M3514: LQFP48, QFN48

Contents

2 Product Information for F035

See the following table for APM32F035x8 product functions and peripheral configuration.

Table 1 APM32F035x8 Series Chip Functions and Peripherals

Product		**APM32F035**
Type		**C8T7**
Package		**LQFP48**
Core and maximum working frequency		Arm® 32-bit Cortex®-M0+@72MHz
M0CP coprocessor		1
Flash(KB)		64
SRAM(KB)		10
Timer	32-bit/16-bit general	1/2
	16-bit advanced	1
	16-bit basic	2
	System tick timer	1
	Watchdog	2(1 independent watchdog+1 window watchdog)
	RTC	1
Communication interface	USART	2
	SPI/I2S	1/1
	I2C	1
	CAN	1
Real-time clock		1
12-bit ADC	Unit	1
	External channel	16
	Internal channel	3
Analog comparator		2
Operational amplifier		4
GPIOs		42
Working temperature		Ambient temperature: -40°C to 105°C Junction temperature: -40°C to 125°C
Working voltage		2.0~3.6V

3 Product Information for M3514

See the following table for APM32M3514x8 product functions and peripheral configuration.

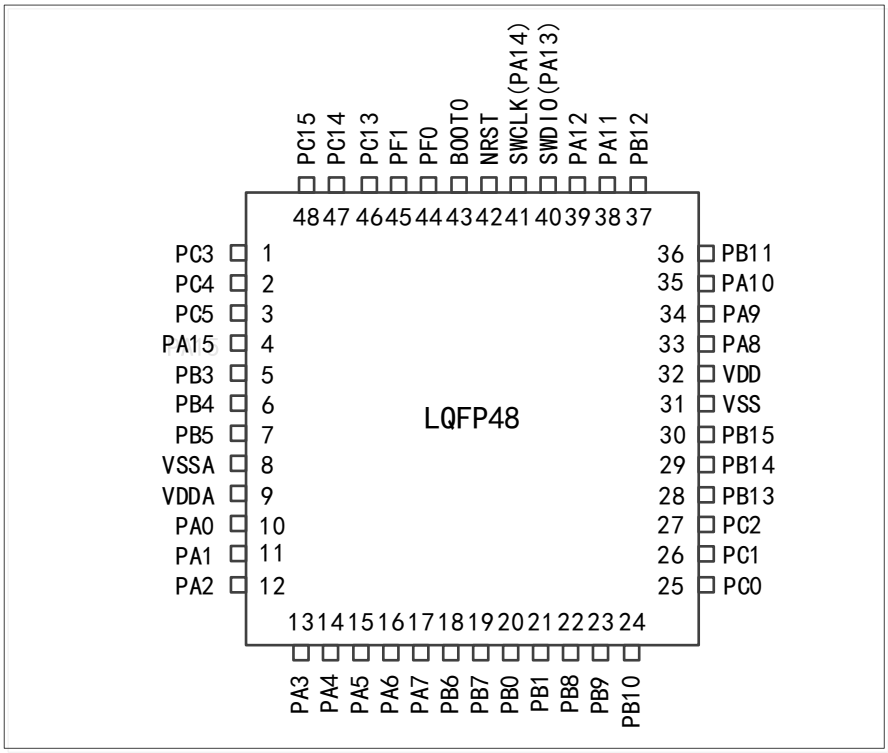
Table 2APM32M3514x8 Series Chip Functions and Peripherals

Product		**APM32M3514**	
Type		**C8T7**	**C8U7**
Package		**LQFP48**	**QFN48**
Core and maximum working frequency		Arm® 32-bit Cortex®-M0+@72MHz	
M0CP coprocessor		1	
Flash(KB)		64	
SRAM(KB)		10	
Timer	32-bit/16-bit general	1/2	
	16-bit advanced	1	
	16-bit basic	2	
	System tick timer	1	
	Watchdog	2(1 independent watchdog+1 window watchdog)	
	RTC	1	
Communication interface	USART	2	
	SPI/I2S	1/1	
	I2C	1	
	CAN	1	
Real-time clock		1	
12-bit ADC	Unit	1	
	External channel	13	
	Internal channel	3	
Analog comparator		2	
Operational amplifier		4	
Supply voltage of the built-in driver.		5V~20V	
Gate Driver		6N	
Voltage resistance of driver power		25V	
Voltage resistance of high-side floating		200V	
GPIOs		29	
Working temperature		Ambient temperature: -40°C to 105°C Junction temperature: -40°C to 125°C	
Working voltage		2.0V~3.6V	

4 Pin Information

4.1 Pin Distribution for F035

Figure 1 Pin Distribution Diagram of APM32F035x8 Series LQFP48



4.2 Pin Function Description for F035

Table 3Legends/Abbreviations Used in Output Pin Table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in parentheses below the pin name, the pin functions during and after reset are the same as the actual pin name	
Pin type	P	Power supply pin
	I	Input pins only
	I/O	I/O pins
I/O structure	5T	I/O with 5V tolerance
	5Tf	I/O, FM+ function with 5 V tolerance
	STDA	I/O with 3.3 V tolerance is directly connected to ADC
	STD	Standard 3.3VI/O
	B	Dedicated BOOT0 pin
	RST	Bidirectional reset pin with built-in weak pull-up resistor
Note	Unless otherwise specified in the notes, all I/O is set as floating input during and after reset	

Name		Abbreviation	Definition
Pin function	Multiplexing function	The function selected by GPIOx_AFR register	
	Additional function	Functions directly selected/enabled through peripheral registers	

Table 4APM32F035x8T7 Sort Description by Pin Name

LQFP48	Pin name (Function after reset)	Multiplexing function	Additional function	Type	Structure
1	PC3	EVENTOUT, TMR1_ETR, TMR2_CH4, USART1_RTS, COMP2_OUT	ADC_IN13	I/O	5T
2	PC4	EVENTOUT，I2C1_SDA, USART1_TX, CAN_TX，TMR1_CH4	ADC_IN14	I/O	5Tf
3	PC5	I2C1_SCL, USART1_RX, CAN_RX，TMR1_CH5	ADC_IN15	I/O	5Tf
4	PA15	SPI1_NSS, I2S1_WS, USART2_RX, TMR2_CH1_ETR, EVENTOUT，TMR4_CH1	OP1P	I/O	5T
5	PB3	SPI1_SCK, I2S1_CK, EVENTOUT，TMR2_CH2, TMR3_CH2, TMR4_CH2	OP1N	I/O	5T
6	PB4	SPI1_MISO, I2S1_MCK, TMR3_CH1, EVENTOUT，TMR2_CH3，TMR4_CH3	OP2P	I/O	5T
7	PB5	SPI1_MOSI, I2S1_SD, TMR3_CH2，I2C1_SMBA, TMR3_ETR, TMR4_CH4	OP2N	I/O	5T
8	VSSA	VSSA	VSSA	P	-
9	VDDA	VDDA	VDDA	P	-

LQFP48	Pin name (Function after reset)	Multiplexing function	Additional function	Type	Structure
1	PC3	EVENTOUT, TMR1_ETR, TMR2_CH4, USART1_RTS, COMP2_OUT	ADC_IN13	I/O	5T
10	PA0	USART2_CTS, TMR2_CH1_ETR, COMP1_OUT	ADC_IN4, COMP1_INM4, COMP2_INM4	I/O	5T
11	PA1	EVENTOUT，USART2_RTS, TMR2_CH2, USART1_CK	ADC_IN5, COMP1_INM5, COMP2_INM5	I/O	5T
12	PA2	USART2_TX, TMR2_CH3, CAN_TX，USART1_TX，COMP2_OUT	ADC_IN0, COMP1_INM6, OPA1_OUT	I/O	5T
13	PA3	USART2_RX, TMR2_CH4, TMR2_CH3	ADC_IN1, COMP1_INP	I/O	5T
14	PA4	SPI1_NSS, I2S1_WS, USART2_CK, CAN_RX，USART1_RX	ADC_IN2, COMP2_INM6, OPA2_OUT	I/O	5T
15	PA5	SPI1_SCK, I2S1_CK, TMR2_CH1_ETR	ADC_IN3, COMP2_INP"	I/O	5T
16	PA6	SPI1_MISO, I2S1_MCK, TMR3_CH1, TMR1_BKIN, EVENTOUT，COMP1_OUT	ADC_IN6	I/O	5T
17	PA7	SPI1_MOSI, I2S1_SD, TMR3_CH2, TMR1_CH1N, COMP2_OUT, EVENTOUT	ADC_IN7	I/O	5T

LQFP48	Pin name (Function after reset)	Multiplexing function	Additional function	Type	Structure
1	PC3	EVENTOUT, TMR1_ETR, TMR2_CH4, USART1_RTS, COMP2_OUT	ADC_IN13	I/O	5T
18	PB6	USART1_TX, I2C1_SCL, TMR3_CH3, TMR4_ETR	OP3P	I/O	5Tf
19	PB7	USART1_RX, I2C1_SDA	OP3N	I/O	5Tf
20	PB0	TMR3_CH3, TMR1_CH2N, CAN_RX，USART2_RX, EVENTOUT	ADC_IN8, OPA3_OUT	I/O	5T
21	PB1	"TMR3_CH4, TMR1_CH3N"	ADC_IN9	I/O	5T
22	PB8	I2C1_SCL	OP4P	I/O	5Tf
23	PB9	I2C1_SDA, IR_OUT, TMR3_CH4, EVENTOUT	OP4N	I/O	5Tf
24	PB10	TMR2_CH3	OP4OUT, ADC_IN12	I/O	5T
25	PC0	EVENTOUT, TMR2_CH1_ETR	ADC_IN10	I/O	5T
26	PC1	EVENTOUT, TMR2_CH2	ADC_IN11	I/O	5T
27	PC2	EVENTOUT，TMR2_CH3	-	I/O	5T
28	PB13	SPI1_SCK, I2S1_CK, TMR1_CH1N, TMR1_CH3N	-	I/O	5T
29	PB14	TMR1_CH2N, SPI1_MISO, I2S1_MCK, TMR1_CH3，TMR1_CH1	-	I/O	5T

LQFP48	Pin name (Function after reset)	Multiplexing function	Additional function	Type	Structure
1	PC3	EVENTOUT, TMR1_ETR, TMR2_CH4, USART1_RTS, COMP2_OUT	ADC_IN13	I/O	5T
30	PB15	SPI1_MOSI, I2S1_SD, TMR1_CH3N, TMR1_CH1N, TMR1_CH2N	-	I/O	5T
31	VSS	VSS	VSS	P	-
32	VDD	VDD	VDD	P	-
33	PA8	USART1_CK, TMR1_CH1, EVENTOUT, TMR1_CH2，TMR1_CH3, MCO	-	I/O	5T
34	PA9	USART1_TX, TMR1_CH2, TMR1_CH1N, TMR1_CH3N	-	I/O	5T
35	PA10	USART1_RX, TMR1_CH3, TMR1_CH1, TMR4_CH1	-	I/O	5T
36	PB11	CAN_TX，TMR2_CH4, USART2_TX, TMR1_CH4，EVENTOUT	-	I/O	5T
37	PB12	CAN_RX，USART2_RX, SPI1_NSS,I2S1_WS, TMR1_CH5，TMR1_BKIN, EVENT_OUT	-	I/O	5T

LQFP48	Pin name (Function after reset)	Multiplexing function	Additional function	Type	Structure
1	PC3	EVENTOUT, TMR1_ETR, TMR2_CH4, USART1_RTS, COMP2_OUT	ADC_IN13	I/O	5T
38	PA11	USART1_CTS, TMR1_CH4, COMP1_OUT, TMR4_CH2, TMR1_BKIN，TMR1_ETR, EVENTOUT	-	I/O	5T
39	PA12	USART1_RTS, TMR1_ETR, COMP2_OUT, TMR1_CH4, TMR4_CH3, EVENTOUT	-	I/O	5T
40	SWDIO(PA13)	IR_OUT, TMR4_CH4, TMR3_CH1, TMR2_CH1_ETR，USART2_RX，CAN_RX, SWDIO	-	I/O	5T
41	SWCLK(PA14)	USART2_TX, TMR4_ETR, TMR2_CH2，CAN_TX，SWCLK	-	I/O	5T
42	NRST	USART2_TX, TMR4_ETR, TMR2_CH2，CAN_TX，SWCLK	NRST	RST	RST
43	BOOT0	BOOT0	BOOT0	I	B
44	PF0	USART1_TX	OSC_IN	I/O	5T
45	PF1	USART1_RX，I2C1_SMBA	OSC_OUT	I/O	5T

LQFP48	Pin name (Function after reset)	Multiplexing function	Additional function	Type	Structure
1	PC3	EVENTOUT, TMR1_ETR, TMR2_CH4, USART1_RTS, COMP2_OUT	ADC_IN13	I/O	5T
46	PC13	-	RTC_TAMP1, RTC_TS, RTC_OUT, WKUP2	I/O	STD
47	PC14	-	OSC32_IN	I	STD
48	PC15	-	OSC32_OUT	O	STD

4.3 Pin Distribution for M3514

Figure 2 Pin Distribution Diagram of APM32M3514x8 Series LQFP48

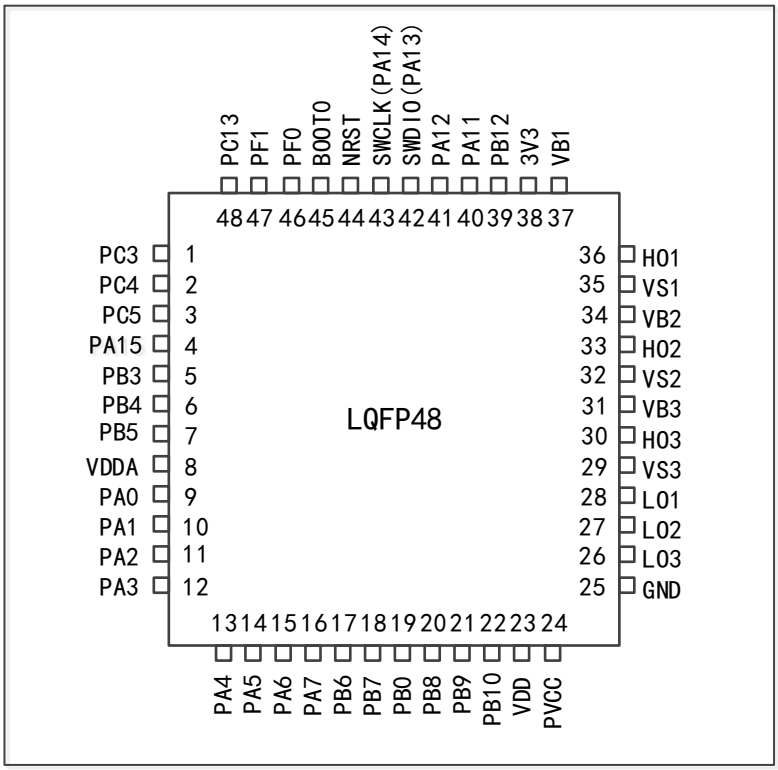
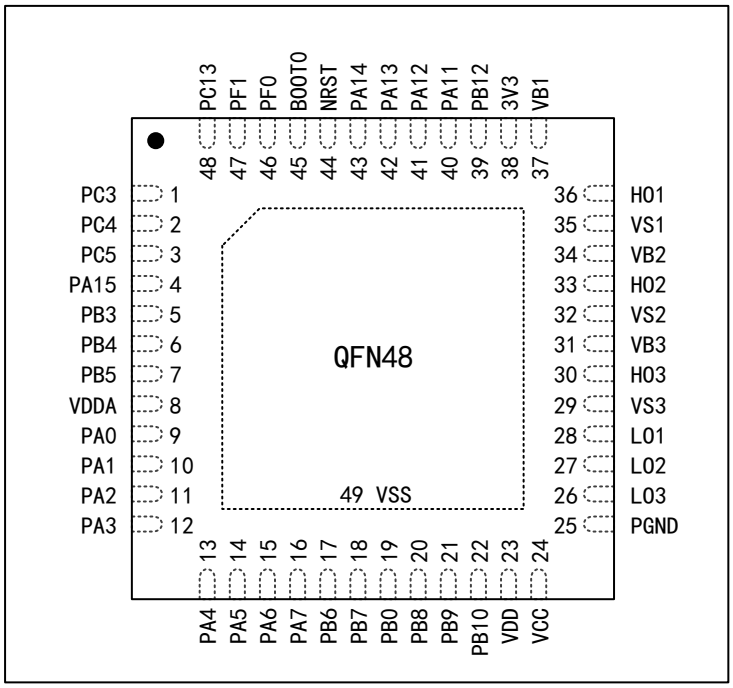


Figure 3 Pin Distribution Diagram of APM32M3514x8 Series QFN48



4.4 Pin Function Description for M3514

Table 5Legends/Abbreviations Used in Output Pin Table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in parentheses below the pin name, the pin functions during and after reset are the same as the actual pin name	
Pin type		P	Power supply pin
		I	Input pins only
		I/O	I/O pins
I/O structure		5T	I/O with 5V tolerance
		5Tf	I/O, FM+ function with 5 V tolerance
		STDA	I/O with 3.3 V tolerance is directly connected to ADC
		STD	Standard 3.3VI/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with built-in weak pull-up resistor
Note		Unless otherwise specified in the notes, all I/O is set as floating input during and after reset	
Pin function	Multiplexing function	The function selected by GPIOx_AFR register	
	Additional function	Functions directly selected/enabled through peripheral registers	

Table 6 APM32F035x8T7 Sort Description by Pin Name

LQFP48	Pin name (Function after reset)	Multiplexing function	Additional function	Type	Structure
1	PC3	EVENTOUT, TMR1_ETR, TMR2_CH4, USART1_RTS, COMP2_OUT	ADC_IN13	I/O	5T
2	PC4	EVENTOUT，I2C1_SDA, USART1_TX, CAN_TX，TMR1_CH4	ADC_IN14	I/O	5Tf
3	PC5	I2C1_SCL, USART1_RX, CAN_RX，TMR1_CH5	ADC_IN15	I/O	5Tf
4	PA15	SPI1_NSS, I2S1_WS, USART2_RX, TMR2_CH1_ETR, EVENTOUT，TMR4_CH1	OP1P	I/O	5T
5	PB3	SPI1_SCK, I2S1_CK, EVENTOUT，TMR2_CH2, TMR3_CH2, TMR4_CH2	OP1N	I/O	5T
6	PB4	SPI1_MISO, I2S1_MCK, TMR3_CH1, EVENTOUT，TMR2_CH3，TMR4_CH3	OP2P	I/O	5T
7	PB5	SPI1_MOSI, I2S1_SD, TMR3_CH2，I2C1_SMBA, TMR3_ETR, TMR4_CH4	OP2N	I/O	5T
8	VDDA	VDDA	VDDA	P	-
9	PA0	USART2_CTS, TMR2_CH1_ETR, COMP1_OUT	ADC_IN4, COMP1_INM4, COMP2_INM4	I/O	5T

LQFP48	Pin name (Function after reset)	Multiplexing function	Additional function	Type	Structure
10	PA1	EVENTOUT，USART2_RTS, TMR2_CH2, USART1_CK	ADC_IN5, COMP1_INM5, COMP2_INM5	I/O	5T
11	PA2	USART2_TX, TMR2_CH3, CAN_TX，USART1_TX，COMP2_OUT	ADC_IN0, COMP1_INM6, OPA1_OUT	I/O	5T
12	PA3	USART2_RX, TMR2_CH4, TMR2_CH3	ADC_IN1, COMP1_INP	I/O	5T
13	PA4	SPI1_NSS, I2S1_WS, USART2_CK, CAN_RX，USART1_RX	ADC_IN2, COMP2_INM6, OPA2_OUT	I/O	5T
14	PA5	SPI1_SCK, I2S1_CK, TMR2_CH1_ETR	ADC_IN3, COMP2_INP"	I/O	5T
15	PA6	SPI1_MISO, I2S1_MCK, TMR3_CH1, TMR1_BKIN, EVENTOUT，COMP1_OUT	ADC_IN6	I/O	5T
16	PA7	SPI1_MOSI, I2S1_SD, TMR3_CH2, TMR1_CH1N, COMP2_OUT, EVENTOUT	ADC_IN7	I/O	5T
17	PB6	USART1_TX, I2C1_SCL, TMR3_CH3, TMR4_ETR	OP3P	I/O	5Tf
18	PB7	USART1_RX, I2C1_SDA	OP3N	I/O	5Tf
19	PB0	TMR3_CH3, TMR1_CH2N, CAN_RX，USART2_RX, EVENTOUT	ADC_IN8, OPA3_OUT	I/O	5T

LQFP48	Pin name (Function after reset)	Multiplexing function	Additional function	Type	Structure
20	PB8	I2C1_SCL	OP4P	I/O	5Tf
21	PB9	I2C1_SDA, IR_OUT, TMR3_CH4, EVENTOUT	OP4N	I/O	5Tf
22	PB10	TMR2_CH3	OP4OUT, ADC_IN12	I/O	5T
23	VDD	VDD	VDD	P	-
24	PVCC (Chip Driver Power Supply)	-	-	P	-
25 (LQFP48)	GND	-	-	GND	-
25 (QFN48)	PGND (Chip Driver Ground)	-	-	GND	-
26	LO3 (Three-Phase Low-Side Output)	-	-	O	-
27	LO2 (Two-Phase Low-Side Output)	-	-	O	-
28	LO1 (One-Phase Low-Side Output）	-	-	O	-
29	VS3 (Three-Phase High-Side Floating Terminal)	-	-	P	-
30	HO3 (Three-Phase High-Side Output)	-	-	O	-
31	VB3 (Three-Phase High-Side Bootstrap Power Supply)	-	-	P	-
32	VS2 (Two-Phase High-Side Floating Terminal)	-	-	P	-
33	HO2 (Two-Phase High-Side Output)	-	-	O	-
34	VB2 (Two-Phase High-Side Bootstrap Power Supply)	-	-	P	-
35	VS1 (One-Phase High-Side Output)	-	-	P	-
36	HO1 (One-Phase High-Side Output)	-	-	O	-
37	VB1 (One-Phase High-Side Bootstrap Power Supply)	-	-	P	-
38	3V3 （3.3V Output）	-	-	P	-

LQFP48	Pin name (Function after reset)	Multiplexing function	Additional function	Type	Structure
39	PB12	CAN_RX， USART2_RX, SPI1_NSS,I2S1_WS, TMR1_CH5， TMR1_BKIN, EVENT_OUT	-	I/O	5T
40	PA11	USART1_CTS, TMR1_CH4, COMP1_OUT, TMR4_CH2, TMR1_BKIN， TMR1_ETR, EVENTOUT	-	I/O	5T
41	PA12	USART1_RTS, TMR1_ETR, COMP2_OUT, TMR1_CH4, TMR4_CH3, EVENTOUT	-	I/O	5T
42	SWDIO(PA13)	IR_OUT, TMR4_CH4, TMR3_CH1, TMR2_CH1_ETR， USART2_RX， CAN_RX, SWDIO	-	I/O	5T
43	SWCLK(PA14)	USART2_TX, TMR4_ETR, TMR2_CH2， CAN_TX， SWCLK	-	I/O	5T
44	NRST	USART2_TX, TMR4_ETR, TMR2_CH2， CAN_TX， SWCLK	NRST	RST	RST
45	BOOT0	BOOT0	BOOT0	I	B
46	PF0	USART1_TX	OSC_IN	I/O	5T
47	PF1	USART1_RX， I2C1_SMBA	OSC_OUT	I/O	5T

LQFP48	Pin name (Function after reset)	Multiplexing function	Additional function	Type	Structure
48	PC13	-	RTC_TAMP1, RTC_TS, RTC_OUT, WKUP2	I/O	STD
49	VSS	-	-	GND	-

4.5 GPIO Multiplexing Function Configuration

Please refer to the pin function description sections of F035 and M3514 to check the configuration of the pin multiplexing functions.

Table 7 GPIOA Multiplexing Function Configuration

Pin name/ configuration	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0		USART2_CTS	TMR2_CH1_ETR					COMP1_OUT
PA1	EVENTOUT	USART2_RTS	TMR2_CH2	USART1_CK				
PA2		USART2_TX	TMR2_CH3	CAN_TX	USART1_TX			COMP2_OUT
PA3		USART2_RX	TMR2_CH4	TMR2_CH3				
PA4	SPI1_NSS, I2S1_WS	USART2_CK		CAN_RX	USART1_RX			
PA5	SPI1_SCK, I2S1_CK		TMR2_CH1_ETR					
PA6	SPI1_MISO, I2S1_MCK	TMR3_CH1	TMR1_BKIN				EVENTOUT	COMP1_OUT
PA7	SPI1_MOSI, I2S1_SD	TMR3_CH2	TMR1_CH1N				EVENTOUT	COMP2_OUT
PA8	MCO	USART1_CK	TMR1_CH1	EVENTOUT	TMR1_CH2	TMR1_CH3		
PA9		USART1_TX	TMR1_CH2		TMR1_CH1N	TMR1_CH3N		
PA10		USART1_RX	TMR1_CH3		TMR1_CH1	TMR4_CH1		
PA11	EVENTOUT	USART1_CTS	TMR1_CH4	TMR1_BKIN	TMR1_ETR	TMR4_CH2		COMP1_OUT
PA12	EVENTOUT	USART1_RTS	TMR1_ETR	TMR1_CH4		TMR4_CH3		COMP2_OUT
PA13	SWDIO	IR_OUT	TMR2_CH1_ETR	CAN_RX	TMR3_CH1	TMR4_CH4	USART2_RX	
PA14	SWCLK	USART2_TX	TMR2_CH2	CAN_TX		TMR4_ETR		
PA15	SPI1_NSS, I2S1_WS	USART2_RX	TMR2_CH1_ETR	EVENTOUT		TMR4_CH1		

Table 8GPIOB Multiplexing Function Configuration

Pin name/ configuration	AF0	AF1	AF2	AF3	AF4	AF5
PB0	EVENTOUT	TMR3_CH3	TMR1_CH2N	CAN_RX	USART2_RX	
PB1		TMR3_CH4	TMR1_CH3N			
PB3	SPI1_SCK, I2S1_CK	EVENTOUT	TMR2_CH2		TMR3_CH2	TMR4_CH2
PB4	SPI1_MISO, I2S1_MCK	TMR3_CH1	EVENTOUT	TMR2_CH3		TMR4_CH3
PB5	SPI1_MOSI, I2S1_SD	TMR3_CH2		I2C1_SMBA	TMR3_ETR	TMR4_CH4
PB6	USART1_TX	I2C1_SCL			TMR3_CH3	TMR4_ETR
PB7	USART1_RX	I2C1_SDA				
PB8		I2C1_SCL				
PB9	IR_OUT	I2C1_SDA		EVENTOUT	TMR3_CH4	
PB10			TMR2_CH3			
PB11	EVENTOUT		TMR2_CH4	CAN_TX	USART2_TX	TMR1_CH4
PB12	SPI1_NSS, I2S1_WS	EVENTOUT	TMR1_BKIN	CAN_RX	USART2_RX	TMR1_CH5
PB13	SPI1_SCK, I2S1_CK		TMR1_CH1N		TMR1_CH3N	
PB14	SPI1_MISO, I2S1_MCK	TMR1_CH1	TMR1_CH2N		TMR1_CH3	
PB15	SPI1_MOSI, I2S1_SD	TMR1_CH1N	TMR1_CH3N		TMR1_CH2N	

Table 9GPIOC Multiplexing Function Configuration

Pin name/ configuration	AF0	AF1	AF2	AF3	AF4
PC0	EVENTOUT		TMR2_CH1_ETR		
PC1	EVENTOUT		TMR2_CH2		
PC2	EVENTOUT		TMR2_CH3		
PC3	EVENTOUT	TMR1_ETR	TMR2_CH4	USART1_RTS	COMP2_OUT
PC4	EVENTOUT	I2C1_SDA	USART1_TX	CAN_TX	TMR1_CH4
PC5		I2C1_SCL	USART1_RX	CAN_RX	TMR1_CH5

Table 10 GPIOF Multiplexing Function Configuration

Pin name/ configuration	AF0	AF1	AF2
PF0		USART1_TX	
PF1		USART1_RX	I2C1_SMBA

5 Function Description

The chip is a 32-bit high-performance micro-controller based on the Arm® Cortex®-M0+core, and its operating frequency can reach 72MHz. The built-in coprocessor supports interaction with TMR1 to improve the calculation speed of PWM parameters, thus improving the PWM configuration speed.

Built-in high-speed memory (up to 64KB of flash memory and 10KB of SRAM), the chip pins reuse a lot of enhanced peripherals and I/O. Provide standard communication interfaces: I2C interface, SPI (I2S) interface, USART interface, CAN interface. In terms of chip security, 96-bit unique UID is supported.

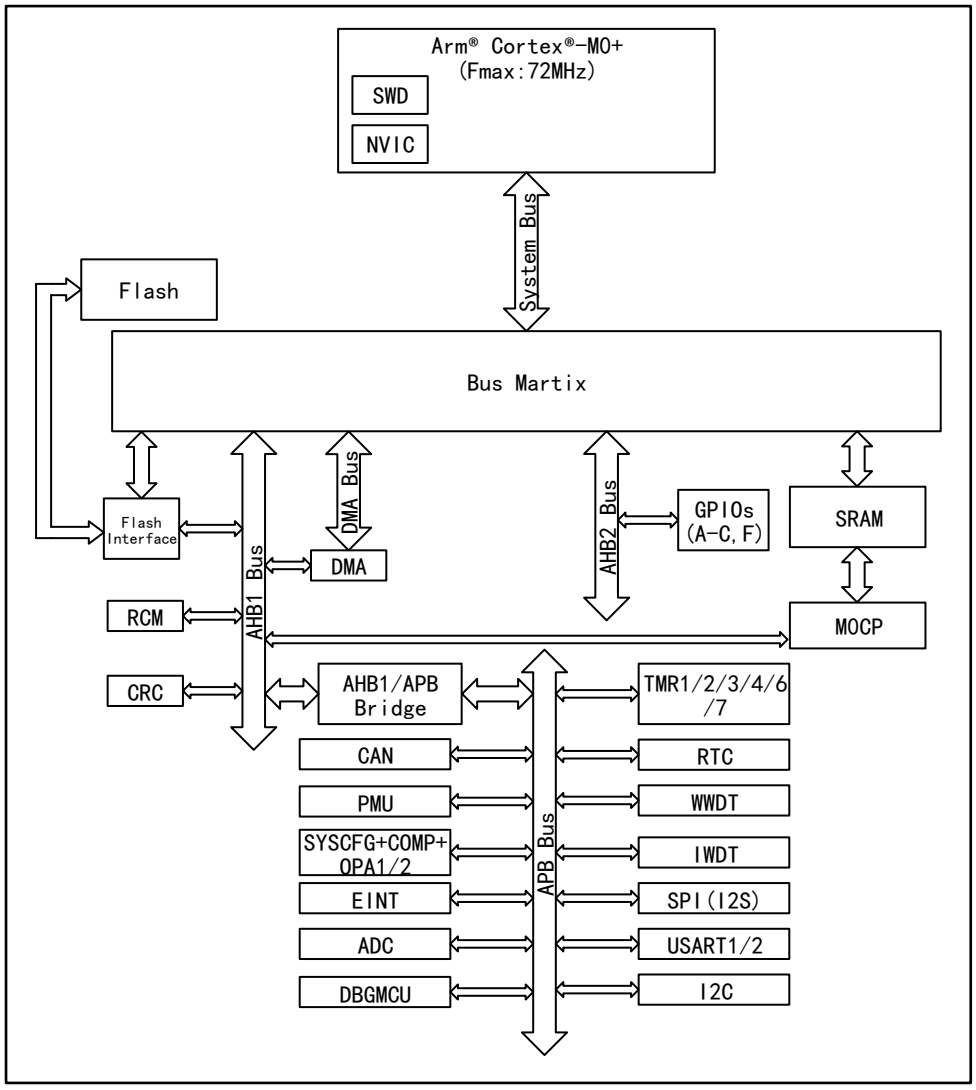
The ambient temperature range is - 40 ℃~+105 ℃ (the temperature sensor works at - 40 ℃ ~105 ℃, and the accuracy is 3 ℃), and the voltage range is 2.0~3.6V. Multiple power-saving modes ensure the requirements of low-power applications.

For information about Arm® Cortex®-M0+core, please refer to the Arm® Cortex®-M0+technical reference sheet, which can be downloaded from Arm's website.

5.1 System Architecture

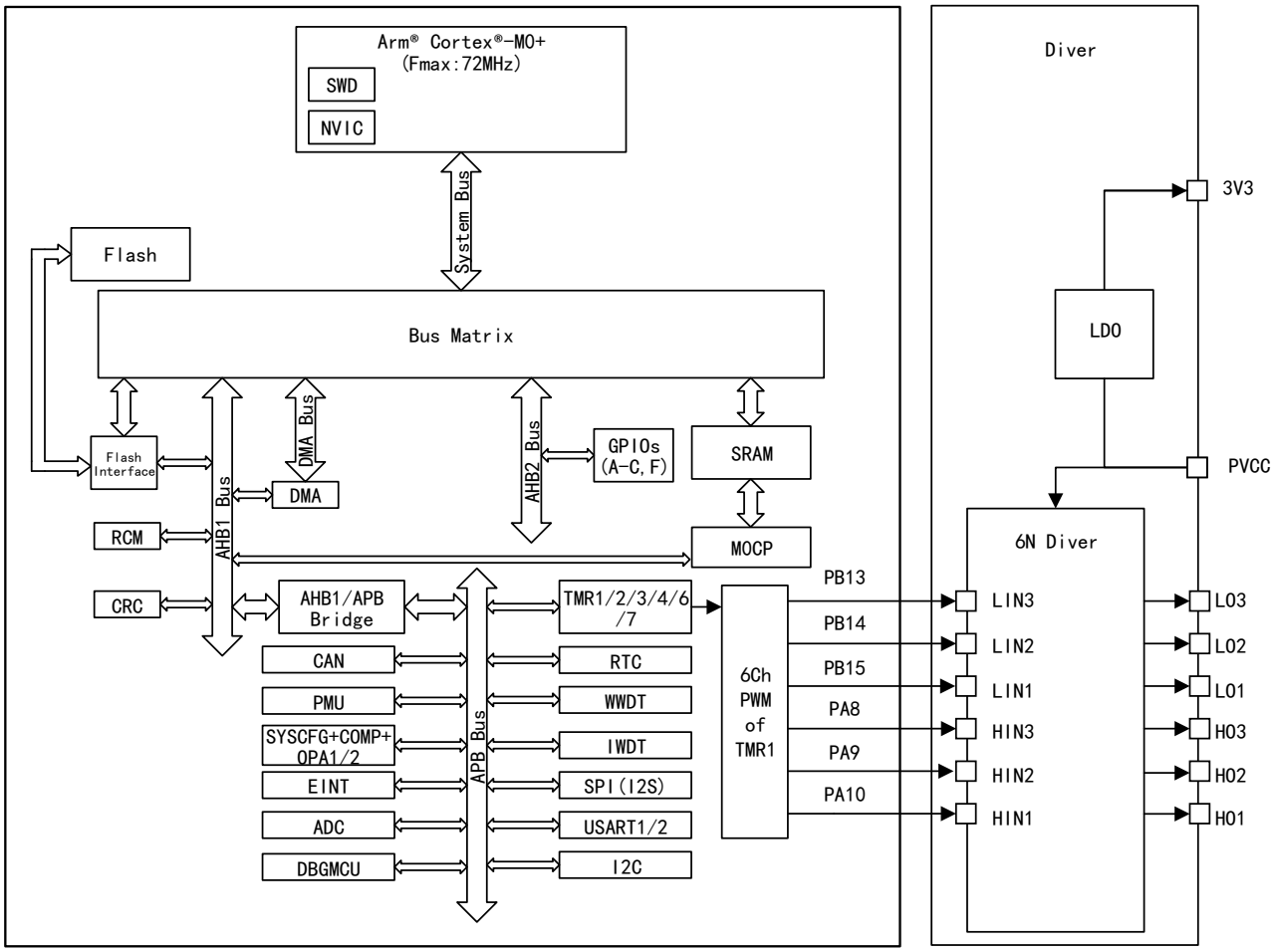
5.1.1 System Block Diagram for F035

Figure 4 APM32F035x8 System Block Diagram



5.1.2 System Block Diagram for M3514

Figure 5 APM32M3514x8 System Block Diagram



5.1.3 Driver Logic Truth Value

（1） VBS undervoltage will only set the HO output low.

（2） VCC undervoltage will set both LO and HO outputs low.

（3） The VG signal is pulled up to high by default, and the LDO output is turned off when the external pull-down is low.

（4） After the over temperature protection function is triggered, both the drive output and LDO output are turned off.

Table 11 Logic Truth Value

OTP	VG	VCCUV	VBSUV	LIN	HIN	LO	HO	LDO
normal	normal	normal	normal	L	H	L	H	3.3V
normal	normal	normal	normal	H	L	H	L	3.3V
normal	normal	normal	normal	L	L	L	L	3.3V
normal	normal	normal	normal	H	H	L	L	3.3V
normal	normal	normal	UV	H&L	H&L	H&L	L	3.3V
normal	normal	UV	normal	H&L	H&L	L	L	3.3V
normal	L	normal	normal	H&L	H&L	H&L	H&L	0V

OTP	VG	VCCUV	VBSUV	LIN	HIN	LO	HO	LDO
OVER	normal	normal	normal	H&L	H&L	L	L	0V

5.1.4 Memory Mapping

Table 12APM32F035x8/M3514x8 Memory Address Boundary

Conduct	Boundary address	Size(Byte)	Memory Space
APM32F035x8T7	0x2000 2000 - 0x3FFF FFFF	~512 MB	Reserve
	0x2000 0000 - 0x2000 27FF	10 KB	SRAM
	0x1FFF FC00 - 0x1FFF FFFF	1 KB	Reserve
	0x1FFF F800 - 0x1FFF FBFF	1 KB	Option bytes
	0x1FFF F79C-0x1FFF F7FF	100 B	Chip configuration region
	0x1FFF_F780-0x1FFF_F79B	28 B	OTP (Option Byte)
	0x1FFF EC00 - 0x1FFF F77F	2944 B	System memory
	0x0801 0000 - 0x1FFF EBFF	~384 MB	Reserve
	0x0800 0000 - 0x0800 FFFF	64 KB	Main Flash memory
	0x0001 0000 - 0x07FF FFFF	~128 MB	Reserve
	0x0000 0000 - 0x0000 FFFF	64 KB	Main Flash memory, system memory or SRAM depending on BOOT configuration

Table 13 APM32F035x8/M3514x8 Peripheral Register Address Boundary

Bus	Boundary address	Size(Byte)	Peripheral
-	0xE000 0000 - 0xE00F FFFF	1MB	Cortex®-M0 internal peripherals
-	0x4800 1800 - 0x5FFF FFFF	~384 MB	Reserve
AHB2	0x4800 1400 - 0x4800 17FF	1KB	GPIOF
	0x4800 0C00 - 0x4800 13FF	2KB	Reserve
	0x4800 0800 - 0x4800 0BFF	1KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1KB	GPIOA
-	0x4002 5400 - 0x47FF FFFF	~128 MB	Reserve
AHB1	0x4002 5000 - 0x4002 53FF	1 KB	Reserve
	0x4002 4400 - 0x4002 4FFF	3 KB	Reserve
	0x4002 4000 - 0x4002 43FF	1 KB	M0CP
	0x4002 3400 - 0x4002 3FFF	3 KB	Reserve
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserve
	0x4002 2000 - 0x4002 23FF	1 KB	FLASH interface

Bus	Boundary address	Size(Byte)	Peripheral
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserve
	0x4002 1000 - 0x4002 13FF	1 KB	RCM
	0x4002 0400 - 0x4002 0FFF	3 KB	Reserve
	0x4002 0000 - 0x4002 03FF	1 KB	DMA
-	0x4001 8000 - 0x4001 FFFF	32 KB	Reserve
APB	0x4001 5C00 - 0x4001 7FFF	9 KB	Reserve
	0x4001 5800 - 0x4001 5BFF	1 KB	DBGMCU
	0x4001 4400 - 0x4001 57FF	5 KB	Reserve
	0x4001 4000 - 0x4001 43FF	1 KB	TMR7
	0x4001 3C00 - 0x4001 3FFF	1 KB	Reserve
	0x4001 3800 - 0x4001 3BFF	1 KB	USART1
	0x4001 3400 - 0x4001 37FF	1 KB	Reserve
	0x4001 3000 - 0x4001 33FF	1 KB	SPI
	0x4001 2C00 - 0x4001 2FFF	1 KB	TMR1
	0x4001 2800 - 0x4001 2BFF	1 KB	Reserve
	0x4001 2400 - 0x4001 27FF	1 KB	ADC
	0x4001 0800 - 0x4001 23FF	7 KB	Reserve
	0x4001 0400 - 0x4001 07FF	1 KB	EINT
	0x4001 0000 - 0x4001 03FF	1 KB	SYSCFG COMP OPA
	0x4000 7400 - 0x4000 FFFF	35 KB	Reserve
	0x4000 7000 - 0x4000 73FF	1 KB	PMU
	0x4000 6800 - 0x4000 6FFF	2 KB	Reserve
	0x4000 6400 - 0x4000 67FF	1 KB	CAN
	0x4000 6000 - 0x4000 63FF	1 KB	CAN SRAM
	0x4000 5800 - 0x4000 5BFF	1 KB	Reserve
	0x4000 5400 - 0x4000 57FF	1 KB	I2C
	0x4000 4800 - 0x4000 53FF	3 KB	Reserve
	0x4000 4400 - 0x4000 47FF	1 KB	USART2
	0x4000 3400 - 0x4000 43FF	4 KB	Reserve
	0x4000 3000 - 0x4000 33FF	1 KB	IWDT
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDT
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC

Bus	Boundary address	Size(Byte)	Peripheral
	0x4000 2400 - 0x4000 27FF	1 KB	Reserve
	0x4000 2000 - 0x4000 23FF	1 KB	TMR4
	0x4000 1400 - 0x4000 1FFF	3 KB	Reserve
	0x4000 1000 - 0x4000 13FF	1 KB	TMR6
	0x4000 0800 - 0x4000 0FFF	2 KB	Reserve
	0x4000 0400 - 0x4000 07FF	1 KB	TMR3
	0x4000 0000 - 0x4000 03FF	1 KB	TMR2

5.1.5 Startup Mode

At startup, the user can select one of the following three startup modes by setting the high and low levels of the Boot pin:

- Boot from main memory
- Boot from BootLoader
- Boot from built-in SRAM

The user can use USART interface to reprogram the user Flash if boot from BootLoader.

5.2 Core

Arm® Cortex®-M0+ is the latest generation of embedded Arm core. Based on low development cost and power consumption characteristics of this platform, it can provide excellent calculation performance and advanced system interrupt response, and is compatible with all Arm tools and software.

5.3 Coprocessor M0CP

The coprocessor includes hardware division, hardware square root, trigonometric function generation, SVPWM generation five-segment and seven-segment functions.

The coprocessor (M0CP) is designed to accelerate some applications related to FOC (Field Oriented Control) running on Arm® Cortex®-M0+.

5.4 On-Chip Memory

User-modifiable memory includes main memory, SRAM, option byte and BootLoader. The BootLoader has been written at ex-works and cannot be modified.

Table 14Memory Description

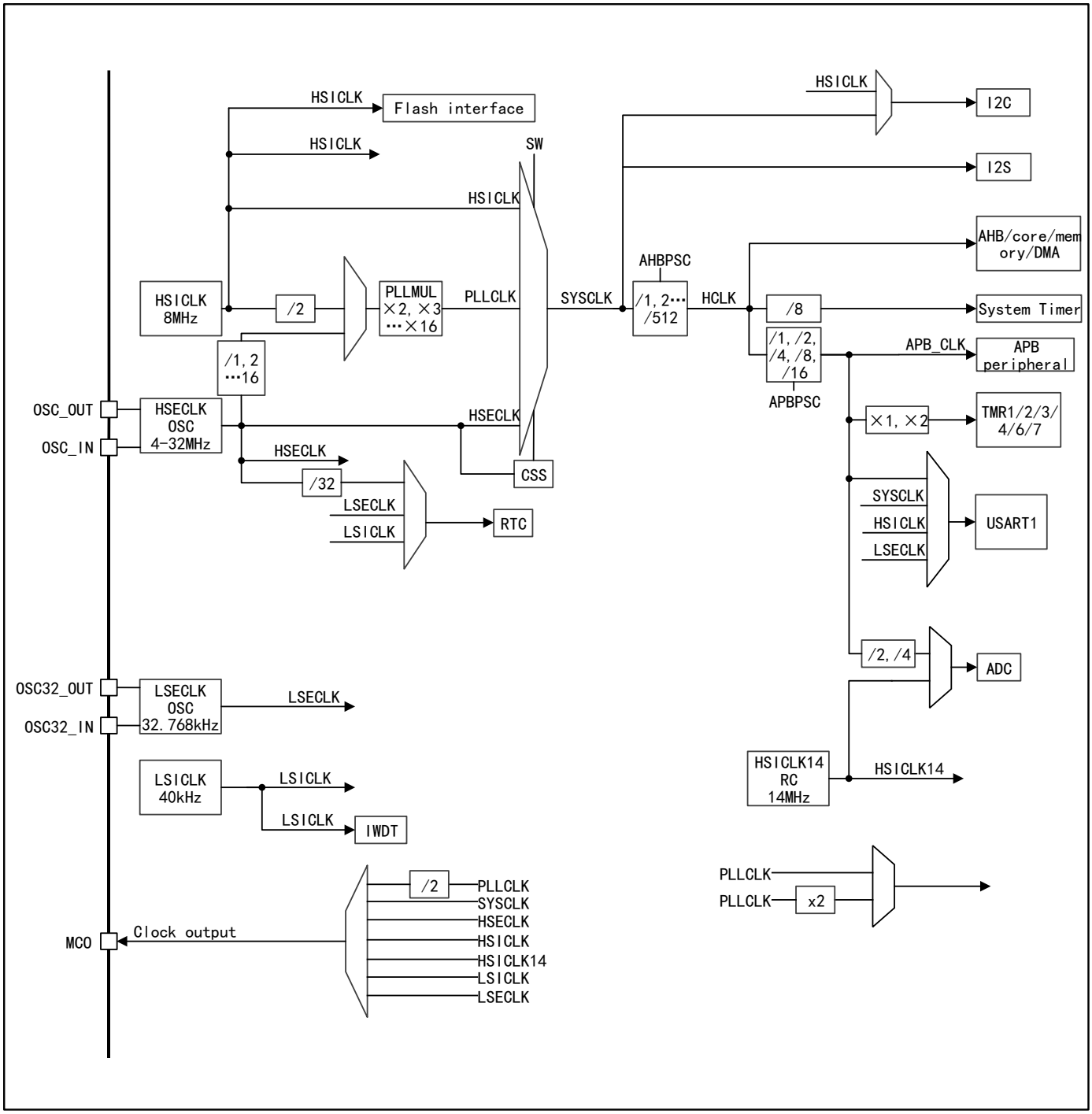
Memory	Max bytes	Description
main memory	64KB	Store user's code and constant data
SRAM	10KB	Parity is not supported. Among them, 2KB belongs to the coprocessor private space.

Memory	Max bytes	Description
Option byte	64Bytes	Three levels can be configured to protect part of the main memory or the whole main memory
BootLoader	2944KB	Store the BootLoader program

5.5 Clock

See the following figure for clock tree of APM32F035x8/M3514x8:

Figure 6 Clock Tree



Note: Only APM32F035x8 support LSECLK.

5.5.1 Clock Source

The clock source is divided into high-speed clock and low-speed clock according to speed. High-speed clock includes HSICLK, HSICLK14 and HSECLK, and low-speed clock includes LSECLK and LSICLK; The internal clock includes LSICLK, HSICLK and HSICLK14, and the external clock includes HSECLK and LSECLK. HSICLK will be calibrated at the factory.

5.5.2 System Clock

The SYSCLK clock source can be HSECLK, PLLCLK or HSICLK.

5.5.3 Bus Clock

The clock source of AHB is SYSCLK, and the clock source of APB is HCLK. The required clock can be obtained by configuring the frequency division coefficient. The maximum value of HCLK and PCLK is 72MHz.

5.6 Power Management

5.6.1 Power Supply Scheme

Table 15Power Supply Scheme

Name	Voltage Range	Description
V_{DD}	2.0~3.6V	V_{DD} directly supplies power to IO port, and V_{DD} supplies power to core circuit through voltage regulator
V_{DDA}	V_{DD}~3.6V	The V_{DDA} supplies power to the ADC, reset module, RC oscillator and PLL, and the voltage level of V_{DDA} must always be greater than or equal to the voltage level of V_{DD}, which should be given priority.

Note: For more details on how to connect the power supply pins, see Power Supply Scheme Figure.

5.6.2 Voltage Regulator

Table 16Working Mode of Regulator

Name	Description
Master mode (MR)	Used in running mode
Low power mode (LPR)	Used in stop mode
Power-down mode	Used in standby mode, when the voltage regulator has high impedance output, the core circuit is powered down, the power consumption of the voltage regulator is zero, and all data of registers and SRAM will be lost.

Note: The voltage regulator is always in working state after reset, and outputs with high impedance in power-down mode.

5.6.3 Power Supply Monitor

Power-on reset (POR) and power-down reset (PDR) circuits are integrated inside the product. These two circuits are always in working condition. When the power-down reset circuit monitors that the power supply voltage is lower than the specified threshold value ($V_{POR/PDR}$), even if the external reset circuit is used, the system will remain reset.

The product has a built-in programmable voltage regulator (PVD) that can monitor V_{DD} and compare it with V_{PVD} threshold. When V_{DD} is outside the V_{PVD} threshold range and the interrupt is enabled, the MCU can be set to a safe state through the interrupt service program.

5.7 Low Power Mode

APM32F035x8T7 supports three low power consumption modes: sleep, shutdown, and standby. These three modes differ in power consumption, wake-up time, and wake-up mode. The low power consumption mode can be selected according to actual application

requirements.

5.8 Interrupt ContReeler

5.8.1 Nested Vector Interrupt ContReeler (NVIC)

The APM32F035x8T7 product has a nested vector interrupt contReeler, and NVIC can handle up to 32 maskable interrupt channels (excluding 16 interrupt lines of Cortex®-M0+) and 4 priorities. The interrupt vector entry address can be directly transmitted to the core, so that the interrupt response processing with low delay can give priority to the late higher priority interrupt.

5.8.2 External Interrupt/ Event ContReeler (EINT)

The external interrupt/event contReeler has 19 edge detectors, each of which includes an edge detection circuit and an interrupt/event request generation circuit. Each detector can be configured as rising edge trigger, falling edge trigger and double edge trigger, and can also be shielded separately. Up to 42 GPIO can be connected to 16 external interrupt lines.

5.9 DMA

A built-in DMA supports seven DMA channels, each channel supports multiple DMA requests, but only one DMA request is allowed to enter the DMA channel at the same time. The peripherals supporting DMA requests are ADC、SPI1、USART1/2、I2C1、TMR1、TMR2、TMR3、TMR6、TMR7. Four levels of DMA channel priority can be configured, and data transmission of "Memory → Memory, Memory → Peripheral, Peripheral → Memory" can be supported (memory includes Flash and SRAM).

5.10 GPIO

The working modes of GPIO can be configured as gengeral input, general output, multiplexing function and analog input/output. General input can be configured as floating input, pull-up input and pull-down input, while general output can be configured as push-pull output and open-drain output. Multiplexing function can be used for digital peripherals, while analog input/output can be used for analog peripherals and low power consumption mode. It can be configured with resistors that prohibit pull-up/pull-down. The speeds of 2MHz, 10MHz and 50MHz can be configured. The higher the speed, the greater the power consumption and noise.

5.11 Analog Peripherals

5.11.1 ADC

One built-in 12-bit ADCs, up to 16 external channels and 3 internal channels, which measure reference voltage and V_{BAT} voltage respectively. It can be configured with the resolution, the sampling time is programmable, and it support self-calibration. The startup mode supports software trigger and hardware trigger. The conversion mode supports single conversion, continuous conversion and intermittent conversion, and the conversion channel selection supports single channel conversion and scanning conversion of a certain sequence of channels. It supports analog watchdog and DMA.

5.11.1.1 Temperature sensor

1 temperature sensor (TSensor) is built in, which is internally connected with ADC_IN16 channel. The voltage generated by the sensor changes linearly with temperature, and the converted voltage value can be obtained by ADC and converted into temperature.

Table 17 Calibration Value of Tsensor

Calibration Value Name	Description	Memory Address
V_{sensor_CAL1}	At 30℃ (±5℃), Original data collected at VDDA=3.3V (±10mV)	0x1FFF F7B8 - 0x1FFF F7B9
V_{sensor_CAL2}	At 105℃ (±5℃), Original data collected at VDDA=3.3V (±10mV)	0x1FFF F7C2 - 0x1FFF F7C3

5.11.1.2 Internal reference voltage (V_{REFINT})

The internal reference voltage (V_{REFINT}) provides a stable (band gap) voltage output for the ADC. V_{REFINT} is internally connected to the ADC_IN17 input channel, which is accessed in read-only mode.

Table 18 Internal Reference Voltage Calibration Value

Calibration Value Name	Description	Memory Address
VREFINT_CAL	Original data collected at 30°C(± 5 °C) and V_{DDA} = 3.3V (10mV)	0x1FFF F7BA - 0x1FFF F7BB

5.11.1.3 Voltage of 1/2*VDD pin

1/2*VDD pin input voltage selects ADC1_IN18 input channel.

5.11.2 Comparator

Two built-in fast rail-to-rail comparators, the internal/external reference voltage, hysteresis, speed and support are programmable, which can generate interrupts. They could be waked up by external interrupts when MCU entering sleep and stop modes, and keep running in Stop mode.

5.11.3 Operational Amplifier (OPA)

Built-in up to 4 independent OPAs can also be used in combination with COMP and ADC. The amplifier output can be used as the input of the ADC conversion module.

5.12 Timer

A built-in 16-bit advanced timer TMR1, a 32-bit general timer TMR2, two 16-bit general timers TMR3/4, two basic timers TMR6/7, an independent watchdog timer, a window watchdog timer , a system tick timer and a infrared timer IRTMR.

Watchdog timer can be used to detect whether the program is running normally.

The system tick timer is a peripheral of the core, which has the function of automatic reloading. When the counter is 0, it can generate a masked system interrupt, which can be used for real-time operating system and general delay.

The characteristics are compared as follows:

Table 19 Function Comparison between Advanced/General-purpose/Basic Timers

Project	Specific content/category	Advanced timer	General-purpose timer		Basic timer
Timer name	-	TMR1	TMR2	TMR3/4	TMR6/7
Timebase unit	Counter	16 bits	32 bits	16 bits	16 bits
	Prescaler	16 bits	16 bits	16 bits	16 bits
	Count mode	Up, down, up/down	Up, down, up/down		Up
Channel	Input channel	4	4	4	0
	Capture/Comparison channel	4	4	4	0
	Output channel	8	4	4	0
	Complementary outputs	3 groups	0	0	0
Function	General DMA request	OK	OK	OK	OK
	PWM mode	Yes	Yes	Yes	No
	Monopulse mode	Yes	Yes	Yes	No
	Forced output mode	Yes	Yes	Yes	No
	Deadband insertion	Yes	No	No	No

5.13 Communication Interface

5.13.1 USART

Two universal synchronous/asynchronous transceivers are built in the chip. USRAT1 supports smart card mode, while USART2 does not.

5.13.2 I2C

Built-in up to two I2Cs can work in multi-master mode and slave mode. It supports 7-bit and 10-bit addressing modes, standard mode (up to 100kbit/s), fast mode (up to 400kbit/s) and ultra-fast mode (1Mbit/s). The DMA controller can be used.

In addition, I2C1 also provides hardware support for SMBUS2.0 and PMBUS1.1: ARP function, host notification protocol, hardware CRC(PEC) generation/verification, timeout verification and alarm protocol management.

See the following table for the differences between I2C1 and I2C2:

5.13.3 SPI/I2S

One SPI interface is built in, which supports full-duplex and half-duplex communication in master mode and slave mode. DMA controller can be used, and 4~16 bits per frame can be configured, with a maximum communication rate of 18Mbit/s.

I2S and SPI belong to the same IP, and have the master-slave mode of simplex communication (only send/receive), with optional 16/24/32 bit data length.

5.13.4 CAN

A built-in CAN, conforming to CAN2.0A and CAN2.0B(active) specifications, the highest bit rate supporting 1Mbit/s, sending and receiving frame format supporting standard frame grid with 11-bit identifier and extended frame with 29-bit identifier.

5.14 Real-Time Clock（RTC）

A built-in RTC with LSECLK signal input pins (OSC32_IN, OSC32_OUT), three TAMP input signal detection pins (RTC_TAMP1), one reference clock input signal (RTC_REFIN), one output timestamp event output pin (RTC_TS), and one signal output pin RTC_OUT (It can be configured as calibration signal output or alarm clock signal output).

The external crystal oscillator, resonator or oscillator, LSICLK and HSECLK/32 with external frequency of 32.768kHz can be selected as the clock source.

With calendar function, it can display sub-seconds, seconds, minutes, hours (12 or 24 hours format), weeks, dates, months and years. It supports alarm clock function, output alarm clock signal for external use, and wake up from low power consumption mode. It can receive signals to wake up from low power consumption mode. In terms of accuracy, it supports daylight saving time compensation, month angel compensation and leap year days compensation. In terms of accuracy, the error caused by crystal oscillator can be repaired by RTC digital calibration function, and the accuracy of calendar can be improved by using a more accurate second source

clock (50 or 60Hz).

5.15 CRC calculation unit

A CRC (cyclic redundancy check) calculation unit is built in, which can generate CRC codes and operate 8-bit, 16-bit and 32-bit data.

5.16 Gate Driver

The M3514x8 series integrates a three-phase medium-voltage high-speed gate driver IC, specifically designed for driving dual N-channel VDMOS power MOSFETs or IGBTs in bridge circuits. It is suitable for applications such as battery-powered brushless DC motors. The typical built-in dead time is 500 ns. When the dead time of the microcontroller output signal is less than the built-in dead time, the actual dead time will be the built-in dead time; conversely, when the dead time of the microcontroller output signal is greater than the built-in dead time, the actual dead time will be the microcontroller output dead time. The built-in VCC and VBS undervoltage protection features prevent the system from turning on external power devices at low driving voltages. The high-side and low-side driver outputs are controlled via input signals. The driver includes a built-in LDO that supports powering control chips like the MCU, with an output voltage of 3.3V.

5.17 Main characteristics

- Operating supply voltage range: 5~20V
- Floating offset voltage: +200V
- Embedded minimum dead time:500ns
- Embedded VCC and VBS undervoltage protection
- Embedded straight-through prevention function
- Embedded input pull-down resistor
- Embedded output pull-down resistor
- Matching the transmission time of high and low-end channels
- High dv/dt noise suppression capability
- Input and output in-phase
- Compatible with 3.3V/5V logic input
- Peak input current 1.1A@15V, 3.3nF load fall time 40ns
- Peak output current 0.9A@15V, 3.3nF load rise time 65ns
- LDO load capacity 60mA@15V
- Overtemperature protection threshold 151 ° C /131 ° C

6 Electrical Characteristics

6.1 Test Conditions of Electrical Characteristics

All voltage parameters (unless otherwise specified) refer to V_{SS}.

6.1.1 Maximum and Minimum Values

Unless otherwise specified, all products are tested on the production line at T_A=25℃. Its maximum and minimum values can support the worst ambient temperature, power supply voltage and clock frequency.

In the notes at the bottom of each table, it is stated that the data obtained through comprehensive evaluation, design simulation or process characteristics are not tested on the production line. On the basis of comprehensive evaluation, take the average value and add and subtract three times the standard deviation (average ±3∑) to get the maximum and minimum values after passing the sample test.

6.1.2 Typical values

Unless otherwise specified, typical data are measured based on T_A=25℃,

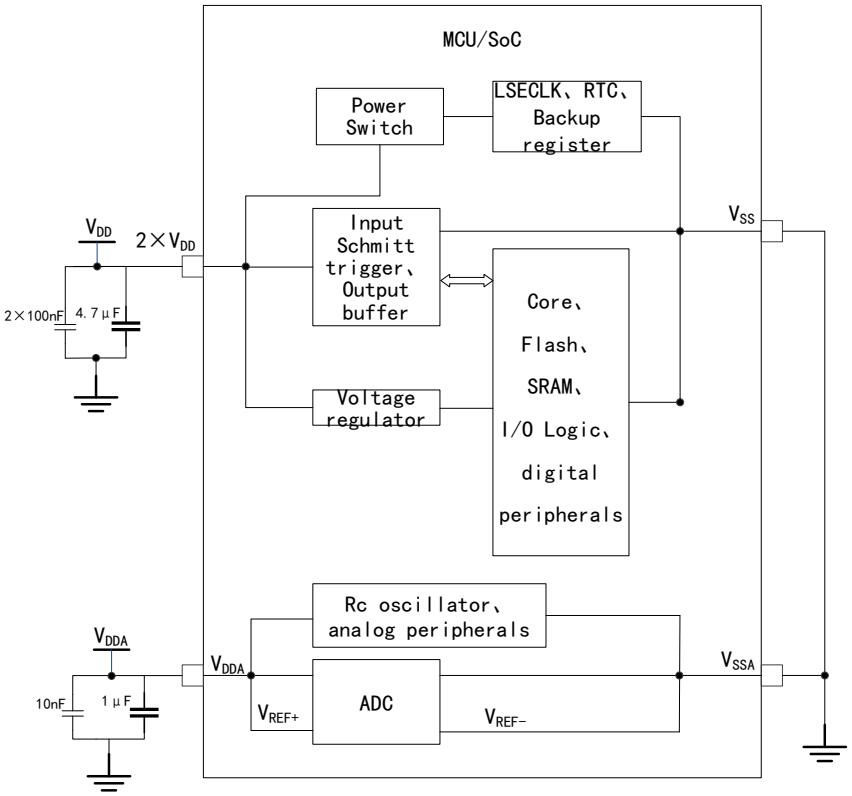
V_{DD}=V_{DDIO2}=V_{DDA}=3.3V. these data are only used for design guidance.

6.1.3 Typical curve

Unless otherwise specified, typical curves will not be tested on the production line, and will only be used for design guidance.

6.1.4 Power Supply Scheme

Figure 7 Power Supply Scheme



6.1.5 Load Capacitance

Figure 8 Load Conditions when Measuring Pin Parameters

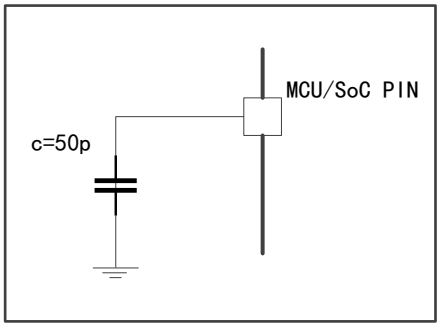


Figure 9 Pin Input Voltage Measurement Scheme

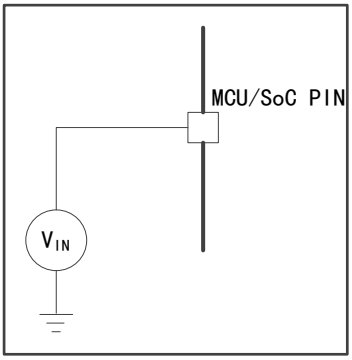
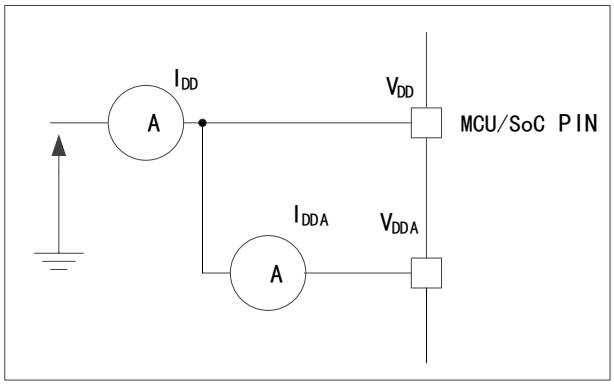


Figure 10 Power Consumption Measurement Scheme



6.2 Testing under General Working Conditions

Table 20General Working Conditions

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
f_{HCLK}	Internal AHB clock frequency	-	-	72	MHz
f_{PCLK}	Internal APB clock frequency	-	-	36	
V_{DD}	Standard operating voltage	-	2	3.6	V
V_{DDA}	Analog operating voltage (when neither ADC nor DAC is used)	V_{DDA} must not be less than V_{DD}	V_{DD}	3.6	V
	Analog operating voltage (when ADC and DAC is used)		2.4	3.6	
V_{IN}	I/O input voltage	STD and RST I/O	-0.3	V_{DDIOX}+0.3	V
		STDA I/O	-0.3	V_{DDA}+0.3	
		5T and 5Tf I/O	-0.3	5.5	
		Boot0	0	5.5	

6.3 Absolute Maximum Rating

If the load on the device exceeds the absolute maximum rating, it may cause permanent damage to the device. Here, only the maximum load that can be borne is given, and there is no guarantee that the device functions normally under this condition.

6.3.1 Maximum Temperature Characteristics

Table 21Temperature Characteristics

Symbol	Description	Numerical value	Unit
T_{STG}	Storage temperature range	–65~+150	℃
T_J	Maximum junction temperature	150	℃

6.3.2 Maximum Rated Voltage Characteristics

All power supply (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the power supply within the external limited range.

Table 22Maximum Rated Voltage Characteristics

Symbol	Description	Minimum value	Maximum value	Unit
V_{DD}-V_{SS}	External main supply voltage (V_{DD})(1)	-0.3	4.0	V
V_{DDA}-V_{SSA}	External analog supply voltage（V_{DDA}）	-0.3	4.0	
V_{DD}-V_{DDA}	Allowable voltage difference of V_{DD}>V_{DDA}	-	0.4	
V_{IN}	Input voltage on 5T and 5Tf pins	V_{SS}-0.3	V_{DD}+4.0(2)	
	Input voltage on STDA pin	V_{SS}-0.3	4.0	
	Boot0	0	V_{DD}+4.0	
	Input voltage on any other pin	V_{SS}-0.3	4.0	
$\|\Delta V_{DDx}\|$	Voltage difference between different power supply pins	-	50	mV
$\|V_{SSx}$-$V_{SS}\|$	Voltage difference between different grounding pins	-	50	

Note:

(1) The V_{DD},V_{DDA} 和 V_{SS},V_{SSA} pin must always be connected to an external power supply.

(2) If IO is configured as pull-up or pull-down input, the maximum input voltage is 4V.

6.3.3 Maximum Rated Current Characteristics

Table 23Maximum Rated Current Characteristics

Symbol	Description	Maximum value	Unit
ΣI_{VDD}	Total current into sum of all V_{DD} power lines (source)(1)	120	mA
ΣI_{VSS}	Total current out of sum of all V_{SS} ground lines (sink)(1)	-120	
$I_{DD（PIN）}$	Maximum current into each V_{DD} power pin (source)(1)	100	
$I_{SS（PIN）}$	Maximum current out of each V_{SS} ground pin (sink)(1)	-100	
$I_{IO（PIN）}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	-25	
$\Sigma I_{IO（PIN）}$	Total output current sunk by sum of all I/Os and control pins(2)	80	
	Total output current sourced by sum of all I/Os and control pins(2)	-80	
$II_{INJ(PIN)}$ (3)	Injected current on 5T and 5Tf pins	-5/+0（4）	
	Injected current on STD and RST pin	±5	
	Injected current on STDA pins(5)	±5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(6)	±25	

（1） All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

（2） This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.

（3） A positive injection is induced by $V_{IN} > V_{DDIOx}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded.

（4） Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.

（5） On these I/Os, a positive injection is induced by $V_{IN} > V_{DDA}$. Negative injection disturbs the analog performance of the device.

（6） When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

6.3.4 ESD Characteristics

Table 24ESD Characteristics

Symbol	Parameter	Pin	Condition	Maximum value	Unit
$V_{ESD(HBM)}$(1)	Electrostatic discharge voltage (Human Model)	MCU	ANSI/ESDA/JEDEC JS-001-2017，24℃	±4000	V
		Gate Driver(2)	ANSI/ESDA/JEDEC JS-001-2023，24℃	±1000	V

Note:

(1) It is tested by a third-party testing organization instead of in production.

(2) LO3，LO2，LO1，VS3，HO3，VB3，VS2，HO2，VB2，VS1，HO1，VB1 are the pins for gate driver。

6.3.5 Static Latch-up

Table 25 Static Latch-up

Symbol	Parameter	Condition	Type
LU	Class of static latch-up	T_A=+105℃	Class II-A

Note: It is tested by a third-party testing organization instead of in production.

6.4 On-Chip Memory

6.4.1 Flash Characteristics

Table 26Flash Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
t_{prog}	16 bit programming time	T_A=-40~105℃, V_{DD}=2.0~3.6V	-	22.4	-	μs
t_{ERASE}	Page (2KB) erase time	T_A=-40~105℃, V_{DD}=2.0~3.6V	-	1.5	-	ms
t_{ME}	Whole erase time	T_A=25℃, V_{DD}=3.3V	-	6.2	-	ms
V_{prog}	Programming voltage	T_A=-40~105℃	2	-	3.6	V
NRW	Erase Cycle	T_A=25℃ T_A=85℃	100k	-	-	

Note: It is tested in comprehensive evaluation instead of in production.

6.5 Clock System

6.5.1 Characteristics of External Clock Source

High-speed external clock generated by crystal resonator

For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer.

Table 27Characteristics of HSECLK 4 ~ 32 MHz Oscillator

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R_F	Feedback resistance	-	-	200	-	kΩ
$t_{SU(HSECLK)}$	Startup time	V_{DD} is stable	-	2.28	-	ms
$Duty_{(HSECLK)}$	Duty cycle	-	50	-	55	%

Note: It is tested in comprehensive evaluation instead of in production.

Low-speed external clock generated by crystal resonator

For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer.

Table 28LSECLK oscillator characteristics (fLSECLK=32.768KHz)

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
$t_{SU(LSECLK)}$(1)	Startup time	V_{DDIOx} is stable	-	2	-	s
$Duty_{(LSECLK)}$	Duty cycle	-	40	-	60	%

Note: It is tested in comprehensive evaluation instead of in production.

（1） $t_{SU(LSECLK)}$ is the starting time, which is measured from the software enabling LSECLK until the stable oscillation at 32.768KHz is obtained. This value is measured using a standard crystal resonator, which may vary from crystal manufacturer to crystal manufacturer.

6.5.2 Characteristics of Internal Clock Source

High speed internal (HSICLK)RC oscillator

Table 29HSICLK Oscillator Characteristics

Symbol	Parameter	Condition		Minimum value	Typical value	Maximum value	Unit
f_{HSICLK}	Frequency	-		-	8	-	MHz
$A_{CCHSICLK}$	Accuracy of HSICLK oscillat	Factory calibration	V_{DD}=3.3V，T_A=25℃(1)	-1	-	1	%
			V_{DD}=2-3.6V，T_A=-40~105℃	-3	-	3	%
$t_{SU(HSICLK)}$	Startup time of HSICLK oscillator	V_{DD}=3.3V T_A=-40~105℃		4	-	6	μs

Note: Except for (1) calibration in production, other data are obtained in comprehensive evaluation instead of in production.

Table 30HSICLK14 Oscillator Characteristics

Symbol	Parameter	Condition		Minimum value	Typical value	Maximum value	Unit
$f_{HSICLK14}$	Frequency	-		-	14	-	MHz
$A_{CCHSICLK14}$	Accuracy of HSICLK14 oscillator	Factory calibration	V_{DD}=3.3V，T_A=25℃(1)	-1	-	1	%
			V_{DD}=2-3.6V，T_A=-40~105℃	-7	-	3	%
$t_{SU(HSICLK14)}$	Startup time of HSICLK14 oscillator	V_{DD}=3.3V T_A=-40~105℃		4	-	7	μs

Note: Except for (1) calibration in production, other data are obtained in comprehensive evaluation instead of in production.

Low speed internal (LSICLK)RC oscillator

Table 31LSICLK Oscillator Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value
f_{LSICLK}	Frequency（V_{DD}=2-3.6V，T_A=-40~105℃）	30	42	50	KHz
$t_{SU(LSICLK)}$	Startup time of LSICLK oscillator（V_{DD}=3.3V，T_A=-40~105℃）	-	-	35	μs

Note: It is tested in comprehensive evaluation instead of in production.

6.5.3 PLL Characteristics

Table 32PLL Characteristics

Symbol	Parameter	Numerical value			Unit
		Minimum value	Typical value	Maximum value	
f_{PLL_IN}	PLL input clock	1	8.0	25	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL frequency doubling output clock (V_{DD}=3.3V，T_A=-40~105℃）	2	-	72	MHz
t_{LOCK}	PLL phase locking time	-	-	200	μs

Note: It is tested in comprehensive evaluation instead of in production.

6.6 Power Management

6.6.1 Characteristic test of embedded reset and power control module

Table 33 Embedded Reset and Power Control Module Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
$V_{POR/PDR}$(1)	Power-on/power-down reset threshold	Falling edge	1.86	1.88	1.92	V
		Rising edge	1.92	1.94	1.98	V
$V_{PDRhyst}$	PDR hysteresis	-	-	100	-	mV
$T_{RSTTEMPO}$	Reset duration	-	2.02	2.43	3.78	ms

Note: It is tested in comprehensive evaluation instead of in production.

（1）PDR detector monitors V_{DD} and V_{DDA} (if enabled in option byte), POR detector monitors V_{DD} only.

Table 34Programmable Voltage Detector Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{PVD}	Level selection of programmable voltage detector	PLS[2:0]=000 (rising edge)	2.08	2.10	2.18	V
		PLS[2:0]=000 (falling edge)	2.18	2.20	2.29	V
		PLS[2:0]=001 (rising edge)	2.19	2.20	2.29	V
		PLS[2:0]=001 (falling edge)	2.28	2.31	2.40	V
		PLS[2:0]=010 (rising edge)	2.27	2.30	2.39	V
		PLS[2:0]=010 (falling edge)	2.38	2.41	2.51	V
		PLS[2:0]=011 (rising edge)	2.37	2.40	2.50	V
		PLS[2:0]=011 (falling edge)	2.47	2.50	2.60	V
		PLS[2:0]=100 (rising edge)	2.46	2.49	2.59	V
		PLS[2:0]=100 (falling edge)	2.57	2.61	2.71	V
		PLS[2:0]=101 (rising edge)	2.56	2.60	2.70	V
		PLS[2:0]=101 (falling edge)	2.67	2.70	2.81	V
		PLS[2:0]=110 (rising edge)	2.66	2.70	2.80	V
		PLS[2:0]=110 (falling edge)	2.77	2.80	2.91	V
		PLS[2:0]=111 (rising edge)	2.76	2.80	2.91	V
		PLS[2:0]=111 (falling edge)	2.86	2.90	3.01	V
$V_{PVDhyst}$	PVD hysteresis	-	-	100	-	mV

Note: It is tested in comprehensive evaluation instead of in production.

6.7 Power Consumption

6.7.1 Power consumption test environment

（1） Test under the conditions of Coremark, KeilV5 compiling environment and L3 compiling optimization level.

（2） All I/O pins are configured as analog inputs, which are connected to V_{DD} or V_{SS} (non-load) at a static level.

（3） Unless otherwise specified, all peripherals are turned off.

（4） The relationship between the setting of flash waiting period and f_{HCLK}:

0~24MHz: 0 waiting period,

24~48MHz: 1 waiting period.

48~72MHz: 2 waiting periods

（5） Instruction prefetch function is enabled (Note: this bit must be set before clock setting and bus frequency division).

（6） When the peripheral is turned on: $f_{PCLK}=f_{HCLK}$.

6.7.2 F035 Power Consumption

Table 35 Program Execution in Flash, Power Consumption in Running Mode

Parameter	Condition	f_{HCLK}	Typical value (1) (mA)	Maximum value (1) (mA)
			T_A=25℃, V_{DD}=3.3V	T_A=105℃, V_{DD}=3.6V
Power consumption in running mode	HSECLK bypass(2), enabling all peripherals	72MHz	18.37	20.53
		48MHz	11.58	12.35
		24MHz	6.07	6.51
		8MHz	2.31	2.62
	HSECLK bypass(2), turn off all peripherals	72MHz	13.44	14.89
		48MHz	8.32	8.82
		24MHz	4.41	4.78
		8MHz	1.77	2.08
	HSICLK(2), enabling all peripherals	72MHz	13.67	15.46
		48MHz	11.14	11.78
		24MHz	5.60	5.97
		8MHz	1.85	2.08
	HSICLK(2), turn off all peripherals	72MHz	10.38	11.72
		48MHz	7.83	8.27
		24MHz	3.88	4.27
		8MHz	1.26	1.47

Note:

（1）It is tested in comprehensive evaluation instead of in production.

（2）The external clock is 8MHz, and when fHCLK>8MHz, turn on PLL, otherwise, turn off PLL.

Table 36 Program Execution in SRAM, Power Consumption in Running Mode

Parameter	Condition	f_{HCLK}	Typical value (1) (mA)	Maximum value (1) (mA)
			T_A=25℃, V_{DD}=3.3V	T_A=105℃, V_{DD}=3.6V
Power consumption in running mode	HSECLK bypass(2), enabling all peripherals	72MHz	15.65	17.41
		48MHz	9.12	9.16
		24MHz	4.79	4.87
		8MHz	1.93	1.92
	HSECLK bypass(2), turn off all peripherals	48MHz	11.67	12.98
		72MHz	5.91	6.35
		24MHz	3.24	3.61
		8MHz	1.39	1.72
	HSICLK(2), enabling all peripherals	72MHz	11.68	13.07
		48MHz	8.69	8.74
		24MHz	4.35	4.46
		8MHz	1.48	1.53
	HSICLK(2), turn off all peripherals	72MHz	10.53	11.87
		48MHz	5.39	5.77
		24MHz	2.74	3.04
		8MHz	0.88	1.07

Notes:

（1）It is tested in comprehensive evaluation instead of in production.

（2）The external clock is 8MHz, and when f_{HCLK}>8MHz, turn on PLL, otherwise, turn off PLL.

Table 37 Program Executed in SRAM or Flash, Power Consumption in Sleep mode

Parameter	Condition	f_{HCLK}	Typical value [1] (mA)	Maximum value [1] (mA)
			T_A=25℃, V_{DD}=3.3V	T_A=105℃, V_{DD}=3.6V
Input the lowest bit	HSECLK bypass[2], enabling all peripherals	72MHz	11.45	11.51
		48MHz	6.45	6.87
		24MHz	3.57	3.86
		8MHz	1.48	1.8
	HSECLK bypass[2], turn off all peripherals	72MHz	4.45	5.59
		48MHz	2.62	2.91
		24MHz	1.66	1.97
		8MHz	0.81	1.18
	HSICLK[2], enabling all peripherals	72MHz	8.05	8.60
		48MHz	5.99	6.38
		24MHz	3.11	3.38
		8MHz	1.01	1.2
	HSICLK[2], turn off all peripherals	72MHz	3.45	4.74
		48MHz	2.10	2.35
		24MHz	1.14	1.35
		8MHz	0.34	0.5

Notes:

（1）It is tested in comprehend sive evaluation instead of in production.

（2）The external clock is 8MHz, and when fHCLK>8MHz, turn on PLL, otherwise, turn off PLL.

Table 38 Power Consumption in Stop and Standby Mode

Parameter	Condition		Typical value(1), (T_A=25℃)				Maximum value(1), (T_A=105℃)	
			V_{DD}=2.4V		V_{DD}=3.3V		V_{DD}=3.6V	
			I_{DDA}(μA)	I_{DD}(μA)	I_{DDA}(μA)	I_{DD}(μA)	I_{DDA}(μA)	I_{DD}(μA)
Power consumption in stop mode	V_{DDA} monitoring ON	The voltage regulator is in running mode and all oscillators are off	1.12	24.58	1.71	21.98	6.04	150.17
		The voltage regulator is in low power mode, and all oscillators are off	2.11	10.43	2.17	7.48	7.39	123.99
Power consumption in standby mode		The LSICLK and IWDT are on	2.61	4.59	2.54	1.93	7.48	12.14
		The LSICLK and IWDT are off	2.26	4.61	2.81	1.46	6.80	11.46
Power consumption in stop mode	V_{DDA} monitoring OFF	The voltage regulator is in low power mode, and all oscillators are off	2.41	10.21	2.92	7.47	7.34	119.53
Power consumption in standby mode		The LSICLK and IWDT are on	1.43	4.32	2.22	1.94	7.19	11.97
		The LSICLK and IWDT are off	1.10	3.60	1.27	1.45	5.61	11.33

Note: It is tested in comprehensive evaluation instead of in production.

6.7.3 M3514 Power Consumption

Table 39 Operating Power Consumption I_{VCC}

LIN/HIN	Mode	System clock	Condition	Minimum value	Maximum value	Unit
LH	RUN/Peripheral ON	72MHz	VCC=15V, VBS=15V, -40~85℃	16	18	mA
HL		72MHz		16.91	18.19	mA
LH	RUN/Peripheral OFF	72MHz		12.57	13.45	mA
HL		72MHz		13.03	13.86	mA
LH	SLEEP/Peripheral ON	72MHz		9.70	10.52	mA
HL		72MHz		10.19	10.91	mA

LIN/HIN	Mode	System clock	Condition	Minimum value	Maximum value	Unit
LH	SLEEP/Peripheral OFF	72MHz		4.93	5.25	mA
HL		72MHz		5.29	5.7	mA

Table 40 Operating Power Consumption I_{VBS}

LIN/HIN	Mode	System clock	Condition	Minimum value	Maximum value	Unit
LH	RUN/Peripheral ON	72MHz	VCC=15V， VBS=15V， -40~85℃	435.7	560.5	uA
HL		72MHz		114.5	161	uA
LH	RUN/Peripheral OFF	72MHz		434.9	560	uA
HL		72MHz		114.3	170.9	uA
LH	SLEEP/Peripheral ON	72MHz		434.1	559.4	uA
HL		72MHz		114.2	170.3	uA
LH	SLEEP/Peripheral OFF	72MHz		432.8	558.4	uA
HL		72MHz		113.9	162.8	uA

6.7.4 Peripheral power consumption

The HSECLK Bypass 1M is adopted as clock source, f_{PCLK}=f_{HCLK}=1M.

Peripheral power consumption = current that enables the peripheral clock-current that disables the peripheral clock.

Table 41 Peripheral Power Consumption

Parameter	Peripheral	Typical value(1) T_A=25℃，V_{DD}=3.3V	Unit
SARM	/	0.20	MHz/μA
AHB2	GPIOF	0.17	
	GPIOC	0.11	
	GPIOB	0.13	
	GPIOA	0.09	
	CRC	0.13	
	FMC	0.19	
	DMA	0.22	
APB	DBGMCU	0.15	
	TMR7	0.20	
	USART1	0.17	
	SPI	0.11	
	TMR1	0.09	
	ADC	0.14	
	OPA（Simple）	3050	
	PMU	0.12	
	CAN	0.15	
	I2C	0.19	
	USART2	0.16	
	IWDT	0.74	
	WWDT	0.21	
	RTC	0.9	
	TMR4	0.22	
	TMR6	0.21	
	TMR3	0.16	
	TMR2	0.22	

6.7.5 Wake-up Time in Low Power Mode

The measurement of wake-up time with low power consumption is from the start of wake-up event to the time when the user program reads the first instruction, in which V_{DD}=V_{DDA}.

Table 42Low Power Wake-up Time

Symbol	Parameter	Condition	Typical value (1), (T_A=25℃)			Maximum value (1)	Unit
			2V	3.3V	3.6V		
$t_{WUSLEEP}$	Wake up from sleep mode	-	173.00	172.80	172.00	-	μs
t_{WUSTOP}	Wake up from stop mode	The voltage regulator is in running mode	4.04	3.64	3.57	4.20	
		The voltage regulator is in low power mode	8.82	6.10	5.82	9.80	
$t_{WUSTDBY}$	Wake up from standby mode	-	44.04	32.69	31.08	50.30	

Note: It is tested in comprehensive evaluation instead of in production.

6.8 I/O Port Characteristics

Table 43 DC Characteristics (T_A=-40℃-105℃,V_{DD}=2~3.6V)

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{IL}	Input low level voltage	STD and STDA I/O	-	-	$0.3V_{DD}$+0.1	V
		5T and 5Tf I/O	-	-	$0.476V_{DD}$-0.4	
		I/O pins except Boot0	-	-	$0.3V_{DD}$	
V_{IH}	Input high level voltage	STD and STDA I/O	$0.447V_{DD}$+0.402	-	-	V
		5T and 5Tf I/O	$0.5V_{DD}$+0.2	-	-	
		I/O pins except Boot0	$0.7V_{DD}$	-	-	
V_{hys}	Schmitt trigger hysteresis	STD and STDA I/O		200		mV
		5T and 5Tf I/O		300		
I_{lkg}	Input leakage current	STD, 5T and 5Tf I/OTTa in digital mode, VSS≤VIN≤VDDIOx	-	-	±0.1	μA
		STDA in digital mode, V_{DDIOx}≤V_{IN}≤V_{DDA}	-	-	1	
		5T and 5Tf I/O V_{DDIOx}≤V_{IN}≤5V	-	-	±0.1	
R_{PU}	Weak pull-up equivalent resistance	V_{IN}=V_{SS}	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistance	V_{IN}=V_{DDIOx}	30	40	50	kΩ

Table 44 AC Characteristics (T_A =25℃)

SPEED[1:0]	Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
10(2MHz)	$f_{max(IO)out}$	Maximum frequency	C_L=50 pF, V_{DD}=2.4~3.6V	-	2	MHz
	$t_{f(IO)out}$	Output falling time from high to low level	C_L=50 pF, V_{DD}=2.4~3.6V	-	125	ns
	$t_{r(IO)out}$	Output rising time from low to high level		-	125	
01(10MHz)	$f_{max(IO)out}$	Maximum frequency	C_L=50 pF, V_{DD}=2.4~3.6V	-	10	MHz
	$t_{f(IO)out}$	Output falling time from high to low level	C_L=50 pF, V_{DD}=2.4~3.6V	-	25	ns
	$t_{r(IO)out}$	Output rising time from low to high level		-	25	
11(50MHz)	$f_{max(IO)out}$	Maximum frequency	C_L=30 pF, V_{DD}=2.7~3.6V	-	50	MHz
	$t_{f(IO)out}$	Output falling time from high to low level	C_L=30 pF, V_{DD}=2.7~3.6V	-	5	ns
	$t_{r(IO)out}$	Output rising time from low to high level		-	5	
	$f_{max(IO)out}$	Maximum frequency		-	2	MHz

SPEED[1:0]	Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
FM+ Configuration	$t_{f(IO)out}$	Output falling time	C_L=50pF，V_{DDIOx} =2.4~3.6V	-	34	ns
	$t_{r(IO)out}$	Output rising time		-	34	
FM+ Configuration	$f_{max(IO)out}$	Maximum frequency	C_L=50 pF, V_{DD}=2.4~3.6V C_L=50 pF, V_{DD}=2.4~3.6V	-	2	MHz
	$t_{f(IO)out}$	Output falling time		-	125	ns
	$t_{r(IO)out}$	Output rising time		-	125	

Figure 11 Definition of Input and Output AC characteristics

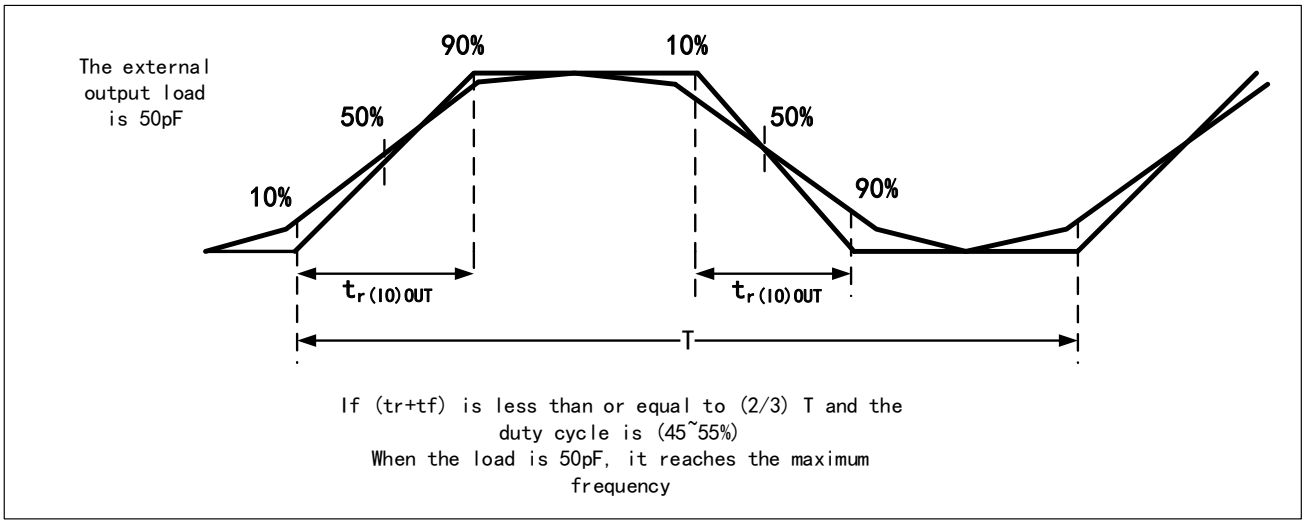


Table 45 Output Drive Current Characteristics (T_A =25℃)

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
V_{OL}	I/O pin outputs low voltage	$\|I_{IO}\|$=8mA, V_{DDIOx}≥2.7V	-	0.4	V
V_{OH}	I/O pin outputs high voltage		V_{DDIOx}-0.4	-	
V_{OL}	I/O pin outputs low voltage	$\|I_{IO}\|$=20mA, V_{DDIOx}≥2.7V	-	1.3	
V_{OH}	I/O pin outputs high voltage		V_{DDIOx}-1.3	-	

Note: It is tested in comprehensive evaluation instead of in production.

6.8.1 NRST pin characteristics

The input drive of NRST pin adopts CMOS process, which is connected with a permanent pull-up resistor R_{PU}

Table 46 NRST Pin Characteristics (T_A=-40~105℃, V_{DD}=2~3.6V)

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
$V_{IL(NRST)}$	NRST input low voltage	-	-	-	0.3V_{DD}+0.07	V
$V_{IH(NRST)}$	NRST input high voltage	-	0.446V_{DD}+0.41	-	-	

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
$V_{hys(NRST)}$	Voltage hysteresis of NRST Schmitt trigger	-	-	300	-	mV
R_{PU}	Weak pull-up equivalent resistance	$V_{IN}=V_{SS}$	30	40	50	kΩ

6.9 Communication Interface

6.9.1 I2C Interface Characteristics

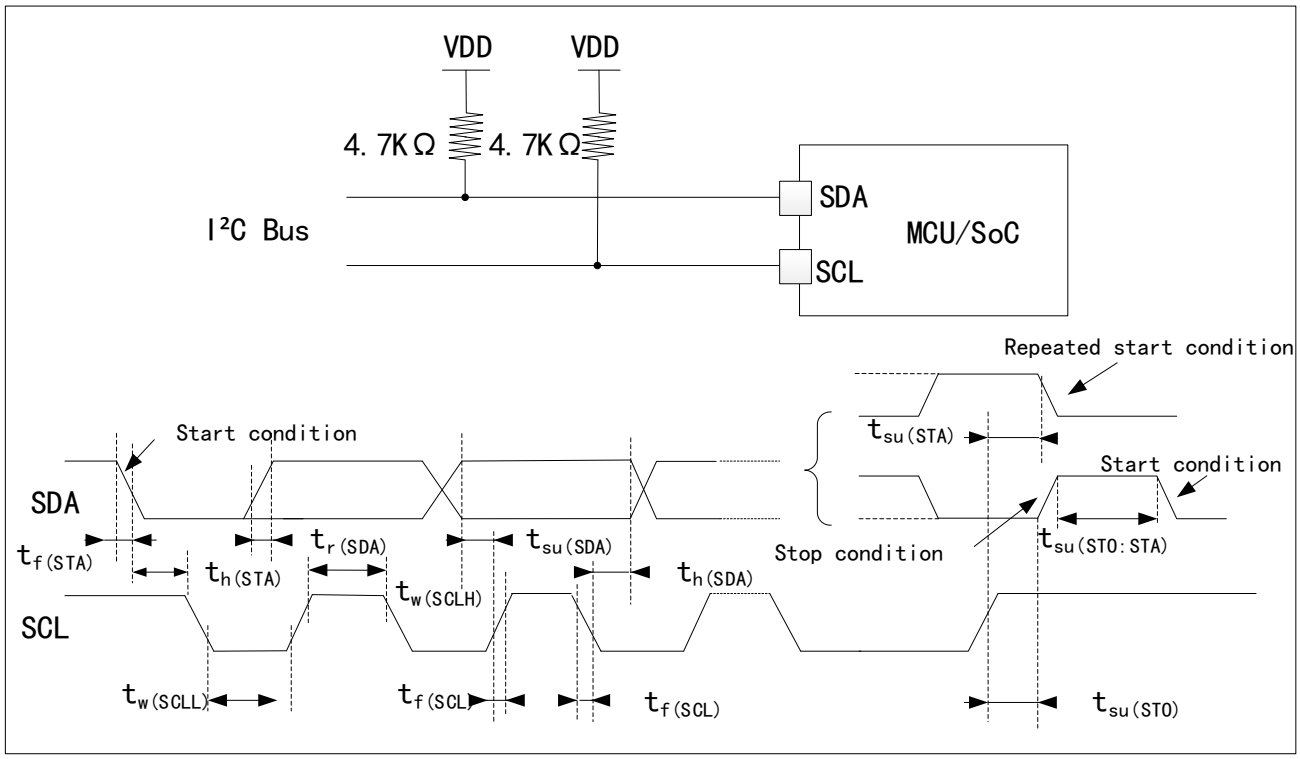
- Standard mode (Sm): Up to 100kbit/s
- Fast mode (Fm): Up to 400kbit/s
- Ultrafast mode (Fm+): Up to 1Mbit/s

Table 47 I2C Interface Characteristics (T_A=25℃, V_{DD}=3.3V)

Symbol	Parameter	Standard I2C		Fast I2C		Ultrafast I2C		Unit
		Minimum value	Maximum value	Minimum value	Maximum value	Minimum value	Maximum value	
$t_{w(SCLL)}$	SCL clock low time	4.91	-	1.78	-	0.65	-	μs
$t_{w(SCLH)}$	SCL clock high time	5.09	-	0.80	-	0.44	-	
$t_{su(SDA)}$	SDA setup time	4595.4	-	1432.1	-	311.11	-	ns
$t_{h(SDA)}$	SDA data holding time	-	237.34	-	210.83	-	209.88	
$t_{r(SDA)}$/ $t_{r(SCL)}$	SDA and SCL rising time	-	451.90	-	434.16	-	395.19	
$t_{f(SDA)}$/ $t_{f(SCL)}$	SDA and SCL falling time	-	6.46	-	3.61	-	3.76	
$t_{h(STA)}$	Start condition holding time	5.02	-	0.77	-	0.41	-	μs
$t_{su(STA)}$	Repeated start condition setup time	4.82	-	0.97	-	0.60	-	
$t_{su(STO)}$	Setup time of stop condition	4.94	-	1.82	-	0.70	-	μs
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus idle)	7.15	-	7.00	-	5.71	-	μs

Note: It is tested in comprehensive evaluation instead of in production.

Figure 12 Bus AC Waveform and Measurement Circuit



Note: the measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

6.9.2 SPI Interface Characteristics

Table 48 SPI Characteristics (T_A=25℃, V_{DD}=3.3V)

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rising and falling time	Load capacitance: C=15pF	-	6	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	$4T_{PCLK}$	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	$2T_{PCLK}$ + 10	-	ns
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, f_{PCLK}=36MHz, Prescaler coefficient =4	T_{PCLK}/2-2	T_{PCLK}/2+1	ns
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	13	-	ns
		Slave mode	22	-	
$t_{h(MI)}$ $t_{h(SI)}$	Data input hold time	Master mode	35	-	ns
		Slave mode	24	-	
$t_{a(SO)}$	Data output access time	Slave mode, f_{PCLK}=20MHz	-	15	ns
$t_{dis(SO)}$	Data output prohibition time	Slave mode	-	18	ns

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
$t_{v(SO)}$	Effective time of data output	Slave mode (after enable edge)	-	15	ns
$t_{v(MO)}$	Effective time of data output	Master mode (after enable edge)	-	5	ns
$t_{h(SO)}$	Data output holding time	Slave mode (after enable edge)	12	-	ns
$t_{h(MO)}$		Master mode (after enable edge)	2	-	

Note: It is tested in comprehensive evaluation instead of in production.

Figure 13 SPI Timing Diagram—Slave Mode and CPHA=0

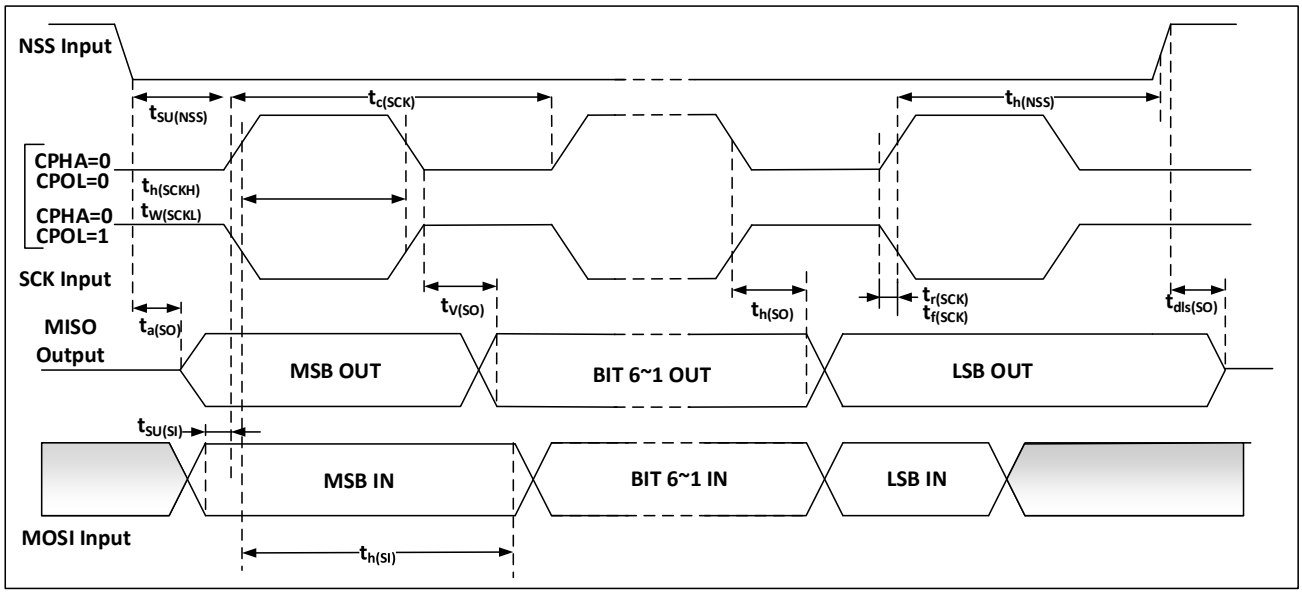
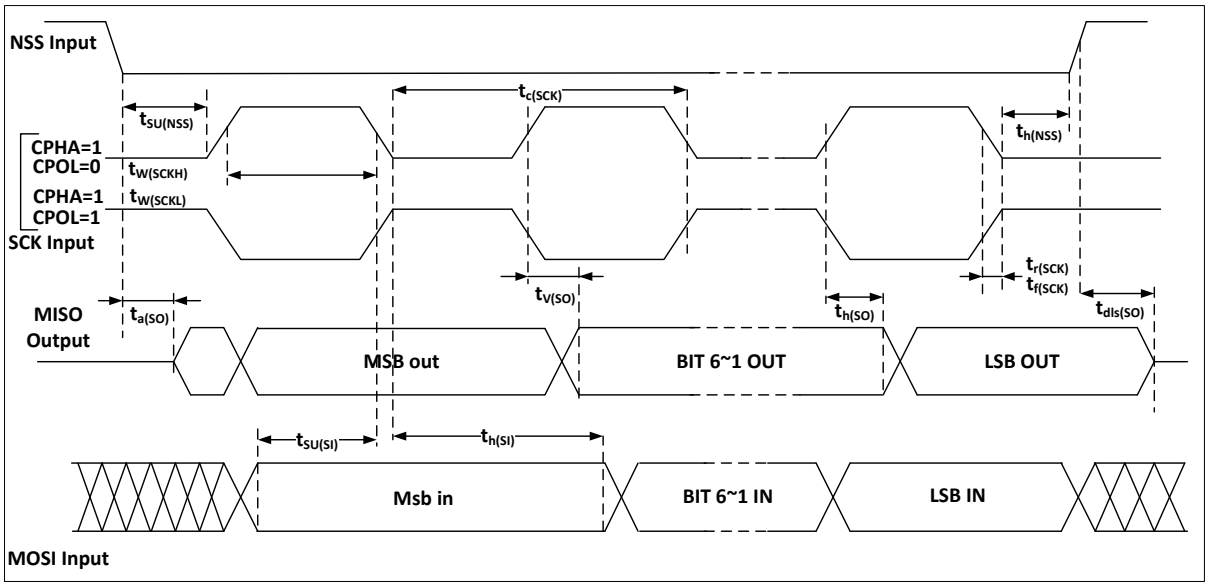
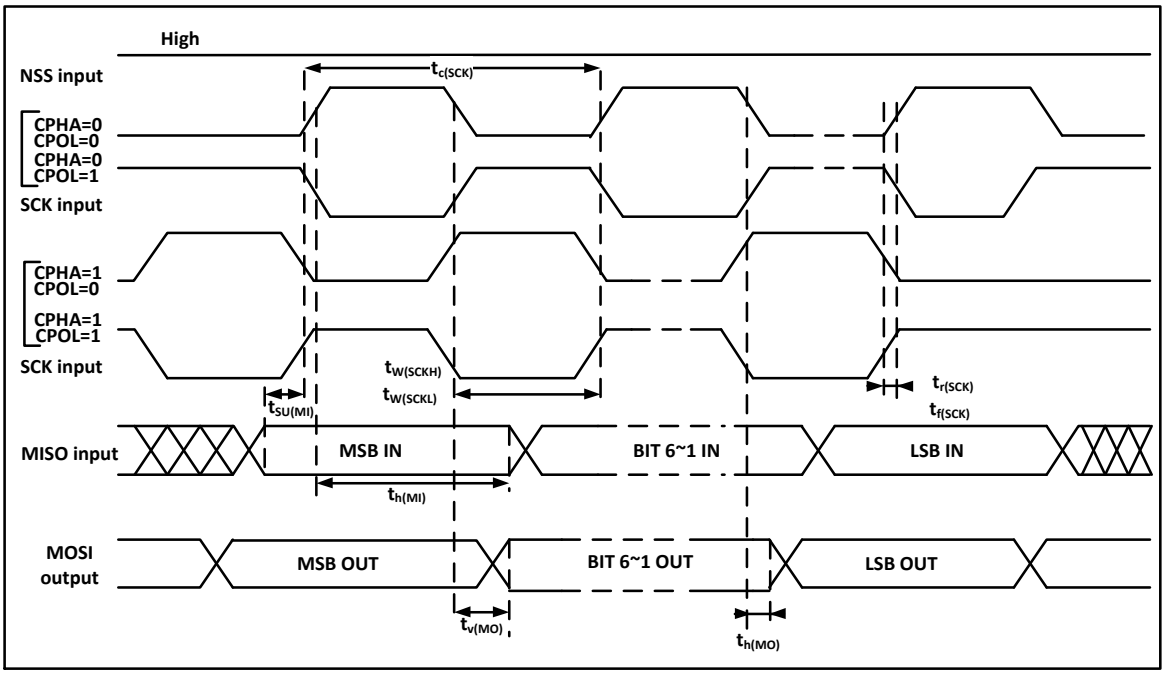


Figure 14 SPI Timing Diagram of figure. 1—slave mode and CPHA=1



Note: the measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 15 SPI Timing Diagram—Master mode



Note: the measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

6.10 ADC

6.10.1 Built-in Reference Voltage Characteristics

Table 49Built-in Reference Voltage Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{REFINT}	Built-in reference voltage	-40℃<T_A<+105℃	1.20	1.21	1.24	V
t_{START}	ADC_IN17 buffer startup time	-	-	-	10	μs
$T_{S\_vrefint}$	Sampling time of ADC when reading out internal reference voltage	-	4	-	-	μs
ΔV_{REFINT}	Built-in reference voltage extends to temperature range	V_{DDA}=3.3V	-	-	10	mV

Note: It is tested in comprehensive evaluation instead of in production.

6.10.2 Temperature Sensor Characteristics

Table 50 Temperature Sensor Characteristics

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
Slope(1)	Average slope（V_{DD} = 3.3V，T_A = -40~105℃）	3.6	4.0	4.6	mV/ºC
V25	Vaoltage in 25ºC（V_{DD} = 2.0-3.6V）	1.40	1.42	1.45	V
TS_temp(2)	ADC sampling time when reading temperature	-	-	17.1	μs

Note: (1) It is guaranteed by design and will not be tested in production.

(2) The minimum sampling time can be determined by the application through multiple loops.

6.10.3 12-bit ADC Characteristics

Table 5112-bit ADC Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{DDA}	service voltage	-	2.4	-	3.6	V
I_{DDA}	ADC power consumption	V_{DDA}=3.3V，f_{ADC}=4MHz，Sampling time =1.5 个 f_{ADC}	-		-	mA
f_{ADC}	ADC frequency	-	0.6	-	14	MHz
C_{ADC}	Internal sample and hold capacitor	-	-	8	-	pF
R_{ADC}	Sampling resistance	-	-	-	1000	Ω
t_S	Sampling time	f_{ADC}=14MHz	0.107	-	17.1	μs
T_{CONV}	Sampling and conversion time	f_{ADC}=14MHz,12-bit conversion	1	-	18	μs

Note: It is tested in comprehensive evaluation instead of in production.

Table 52Accuracy of 12-bit ADC

Symbol	Parameter	Condition	Typical value	Maximum value	Unit
$\|E_T\|$	Composite error	f_{PCLK}=48MHz, f_{ADC}=14MHz, V_{DDA}=2.4V-3.6V T_A=-40℃~105℃	±2.7	±5	LSB
$\|E_O\|$	Offset error		±1.6	±2.5	
$\|E_G\|$	Gain error		±2.6	±3	
$\|E_D\|$	Differential linear error		±1	±2	
$\|E_L\|$	Integral linearity error		±1.5	±3	

Note: It is tested in comprehensive evaluation instead of in production.

6.11 Comparator Characteristics

Table 53Comparator Characteristics

Symbol	Parameter	Condition		Minimum value	Typical value	Maximum value	Unit
V_{DDA}	Analog supply voltage	-		V_{DD}	-	3.6	V
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	-
t_D	Full range step, overload propagation delay of 100mV	Very low power mode		-	2	7	μs
		Low power consumption mode		-	0.7	2.1	
		Medium power mode		-	0.3	1.2	
		Full speed mode	-	90	180	180	ns
			-	110	300	300	
V_{OFFSET}	offset error	-		-	+4	±10	mv

Note: It is tested in comprehensive evaluation instead of in production.

6.12 Operational Amplifier Characteristics

Table 54 Operational Amplifier Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
avdd3p3	Supply Voltage	-	2.4	3.3	3.6	V
CMIR	Common-mode input voltage range	-	0	-	avdd	V
Voffset	Input Offset Voltage	-	-	0.6	-	mV
ILOAD	Load current	-	-	2	-	mA
IDDOPA	Consume current	non-load	-	2	-	mA
CMRR	Common-mode rejection ratio	@1KHz	-	76	-	dB
PSRR	Power Supply Rejection Rario	@1KHz	-	73	-	dB
AV	OPEN-LOOP GAIN	CL=15pF	-	80	-	dB
GBW	Unity-gain bandwidth	CL=15pF	-	10	-	MHz
PM	Phase margin	CL=15pF	-	60	-	°
SR	Slew rate	CL=15pF	-	10	-	V/us
Twakeup	Establishment time from shutdown to wake-up, 0.1% accuracy	CL≤15pF，RL≥4KΩ,Follower	-	2	-	us
RLOAD	Resistive load	-	4	-	-	KΩ
CLOAD	Capacitive load	-	-	-	15	pF
VOHSAT	High saturation output voltage	RL=4KΩ,Input avdd	avdd-100	-	-	mV
		RL=20KΩ,Input avdd	avdd-20	-	-	mV
VOLSAT	Low saturation output voltage	RL=4KΩ,Input 0	-	-	100	mV
		RL=20KΩ, Input 0	-	-	20	mV
EN	Equivalent input voltage noise density	-	80	-	-	nV/sqrtHz
			30	-	-	

6.13 Gate Driver

6.13.1 Recommended safe operating range

T_A=25℃, all pins take GND as the reference points, unless otherwise specified.

Table 55 General Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_A	Ambient temperature	-40	-	105	℃
$V_{HO1,2,3}$	High-side output voltage	$VS_{1,2,3}$	$VS_{1,2,3}$+15	$VB_{1,2,3}$	V
$V_{LO1,2,3}$	Low-side output voltage	0	15	VCC	V
$VB_{1,2,3}$	High-side floating offset absolute voltage	$VS_{1,2,3}$+5	$VS_{1,2,3}$+15	$VS_{1,2,3}$+20	V
$VS_{1,2,3}$	High-side floating offset relative voltage	GND-5	-	140	V
VCC	Supply voltage	5	15	20	V
V_{IN}	Input voltage (HIN1, 2, 3/LIN1, 2, 3)	0	-	5	V
VG	LDO switch enable pin	0	-	5	V
PGND	Power ground	-1.0	0	1.0	V

Note:

(1) When $VB_{1,2,3}$=$VS_{1,2,3}$+10, and $VS_{1,2,3}$ is (COM-5V)~(COM-VBS), the HO logic state is maintained. When $VS_{1,2,3}$ is (COM-5V) ~140V, HO operates normally.

(2) Operation beyond the recommended conditions for a long time may affect its reliability.

6.13.2 Absolute maximum rated value

T_A=25℃, all pins take GND as the reference points, unless otherwise specified.

Table 56 Power Consumption

Symbol	Description	Min	Max	Unit
P_D	Maximum power consumption	-	1.25	W

Note: At any time, the power consumption cannot exceed P_D. The calculation formula for the maximum power consumption at different ambient temperatures is: $P_D=(150℃-T_A)/\theta_{JA}$,
150℃ is the maximum operating junction temperature of the circuit, T_A is the operating ambient temperature of the circuit, and θ_{JA} is the thermal resistance of the package.

Table 57 Temperature Characteristics

Symbol	Description	Min	Max	Unit
T_s	Storage temperature	-55	150	℃
θ_{JA}	Junction-to-ambient thermal resistance	-	75	℃/W
T_J	Junction temperature	-	150	℃
T_L	Pin welding temperature (duration 10s)	-	260	℃

Table 58 Maximum Rated Voltage Characteristics

Symbol	Description	Min	Max	Unit
$V_{HO1,2,3}$	High-side output voltage	$VS_{1,2,3}$-0.3	$VB_{1,2,3}$+0.3	V
$V_{LO1,2,3}$	Low-side output voltage	-0.3	VCC+0.3	V
$VB_{1,2,3}$	High-side floating offset absolute voltage	-0.3	225	V
$VS_{1,2,3}$	High-side floating offset relative voltage	$VB_{1,2,3}$-25	$VB_{1,2,3}$+0.3	V
VCC	Maximum supply voltage	-0.3	25	V
V_{IN}	Maximum input voltage (HIN1,2,3/LIN1,2,3)	-0.3	10	V
VG	LDO switch enable pin	0	14	V
PGND	Power ground	-1.2	1.2	V
dVS/dt	Maximum slew rate of offset voltage	-	50	V/ns

Table 59 ESD Characteristics

Symbol	Description	Min	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	-	1000	V

Note: The 100pF capacitor is discharged through a 1.5kΩ resistor.

6.13.3 Electrical characteristic parameters

T_A=25℃, VCC=$VBS_{1,2,3}$=15V, $VS_{1,2,3}$=GND; all pins take GND as the reference points, unless otherwise specified.

Table 60 Supply Voltage Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VBS_{HY+}	VBS undervoltage high-level potential	4.0	4.3	4.6	V
VBS_{HY-}	VBS undervoltage low-level potential	3.7	4.0	4.3	V
VBS_{HY}	VBS undervoltage hysteresis level	0.2	0.3	0.4	V
VCC_{HY+}	VCC undervoltage high-level potential	4.5	4.6	4.75	V
VCC_{HY-}	VCC undervoltage low-level potential	4.25	4.35	4.45	V
VCC_{HY}	VCC undervoltage hysteresis level	0.15	0.25	0.3	V

Table 61 Supply Current Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{CCD}	VCC dynamic current	$f_{LIN1,2,3}$=20kHz	700	1350	2000	uA
I_{BSD}	VBS dynamic current	$f_{HIN1,2,3}$=20kHz	100	150	400	uA
I_{CCQ}	VCC quiescent current	V_{IN}=0V	700	950	1200	uA
I_{BSQ}	VBS quiescent current	V_{HIN}=0V	30	50	80	uA
I_{LK}	VB floating power supply leakage current	VB=225V	0	0.1	5	uA

Table 62 Time Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{ON}	Output rising edge transmission time	No Load	160	270	350	ns
t_{OFF}	Output falling edge transmission time	No Load	160	270	350	ns
t_r	Output rise time	C_L=3.3nF	55	90	110	ns
t_f	Output fall time	C_L=3.3nF	40	60	90	ns
DT	Dead time	No Load	300	500	650	ns
MT	High and low-side matching time	No Load	0	20	50	ns
tLDO_ON	LDO enable transmission time		300	400	700	ns
tLDO_OFF	LDO disable transmission time		300	400	700	ns

Table 63 Input-end Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IN+}	Input high-level potential		1.70	2.15	2.40	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IN-}	Input low-level potential		0.65	1.45	1.85	V
I_{IN+}	Input high-level current	V_{IN}=5V	8	11	15	uA
I_{IN-}	Input low-level current	V_{IN}=0V	-1	0	1	uA
V_{INHY}	Input hysteresis level		0.45	0.7	1.1	V

Table 64 Driver output-end Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OUT+}	High-level output voltage	I_{OUT}=100mA 15V- V_{OUT}	-	0.51	-	V
V_{OUT-}	Low-level output voltage	I_{OUT}=100mA V_{OUT}-GND	-	0.18	-	V
V_{OUT-}	Low-level output voltage	I_{OUT}=10mA 15V- V_{OUT}	0.05	0.07	0.1	V
V_{OUT-}	Low-level output voltage	I_{OUT}=10mA V_{OUT}-GND	0.02	0.04	0.08	V
I_{OUT+}	High-level short-circuit pulse current	V_{IN}=5V V_O=0V PWD≤10μs	0.7	0.9	1.2	A
I_{OUT-}	Low-level short-circuit pulse current	V_{IN}=0V V_O=15V PWD≤10μs	0.9	1.1	1.5	A

Table 65 Built-in LDO parameters

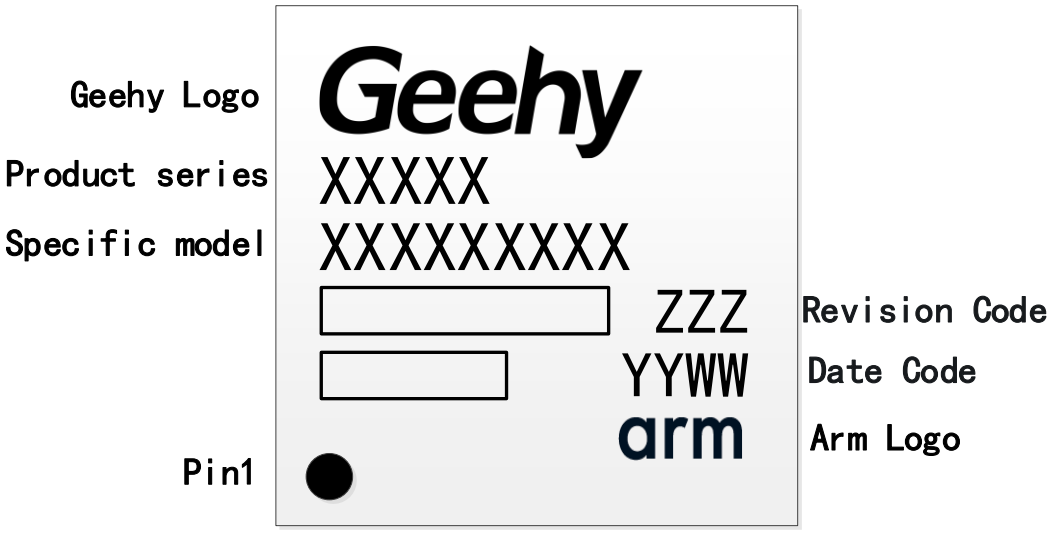
Parameter	Symbol	Condition	Min	Typ	Max	Unit
VLDO	LDO output voltage	VCC=5~20V, Iload=1mA~60mA	3.23	3.3	3.37	V
ΔVLDO_LOAD	Load adjustment	VCC=15V, Iload=0.1mA~33mA	-	20	40	mV
ΔVLDO_LOAD	Load adjustment	VCC=5V, Iload=0.1mA~33mA	-	30	60	mV
ΔVLDO_VCC	Power adjustment	VCC=4~20V, Iload=0.1mA	-	10	20	mV
ΔVLDO_VCC	Power adjustment	VCC=4~20V, Iload=33mA	-	15	30	mV
PSR	Power suppression	Feq=10kHz, VCC=15V, CL=10uF	50	60	-	dB
ΔVLDO_TEMP	Temperature drift	Iload=1mA, -40℃~105℃	-	50	100	mV
IINIT_LIMIT	Output startup current limiting	Vout<0.7V	15	25	40	mA
IOUT_LIMIT	Maximum output current limiting	VCC=15V	70	100	130	mA
OTPHY+	High temperature protection threshold	VCC=15V	147	151	157	℃
OTPHY-	Low temperature protection threshold	VCC=15V	120	125	131	℃

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OTPHY	Temperature protection hysteresis	VCC=15V	21	27	33	℃
Cload	Load capacitance		4.7	10	100	uF
ESR	Equivalent series resistance		0	0	1	Ω

7 Package Information

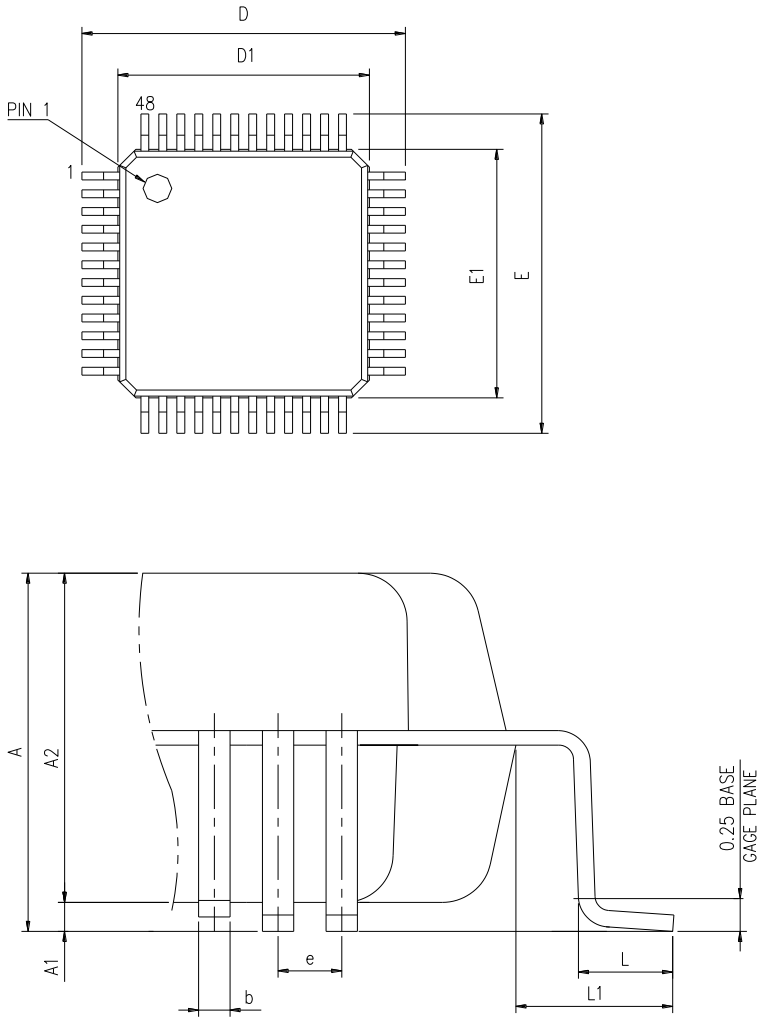
7.1 Product Silkscreen Diagram

Figure 16 Product Silkscreen Diagram



7.2 LQFP48 Package Information

Figure 17 LQFP48 Package Diagram



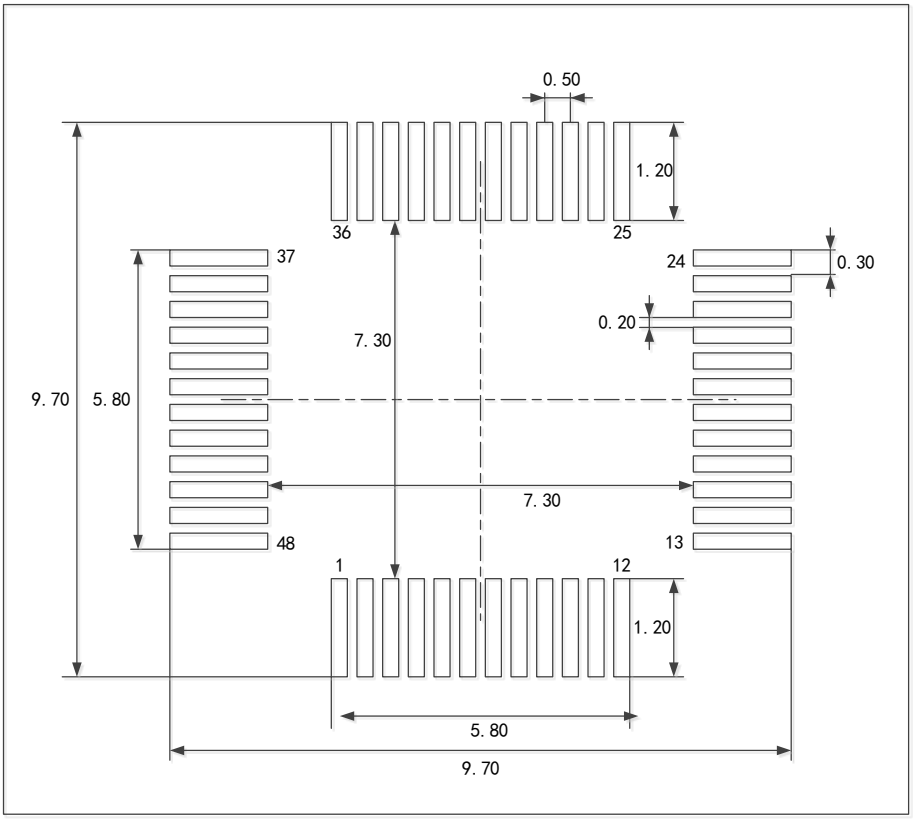
Note: The drawing is not drawn to scale.

Table 66 LQFP48 Package Data

S/N	SYM	Millimeters		
		Min	Typ	Max
1	A	-	-	1.60
2	A1	0.05	-	0.15
3	A2	1.35	1.40	1.45
4	D	8.80	9.00	9.20
5	D1	6.90	7.00	7.10
6	E	8.80	9.00	9.20
7	E1	6.90	7.00	7.10
8	L	0.45	-	0.75
9	L1	1.00		
10	b	0.18	-	0.26
11	e	0.50		

Note: Dimensions are marked in millimeters.

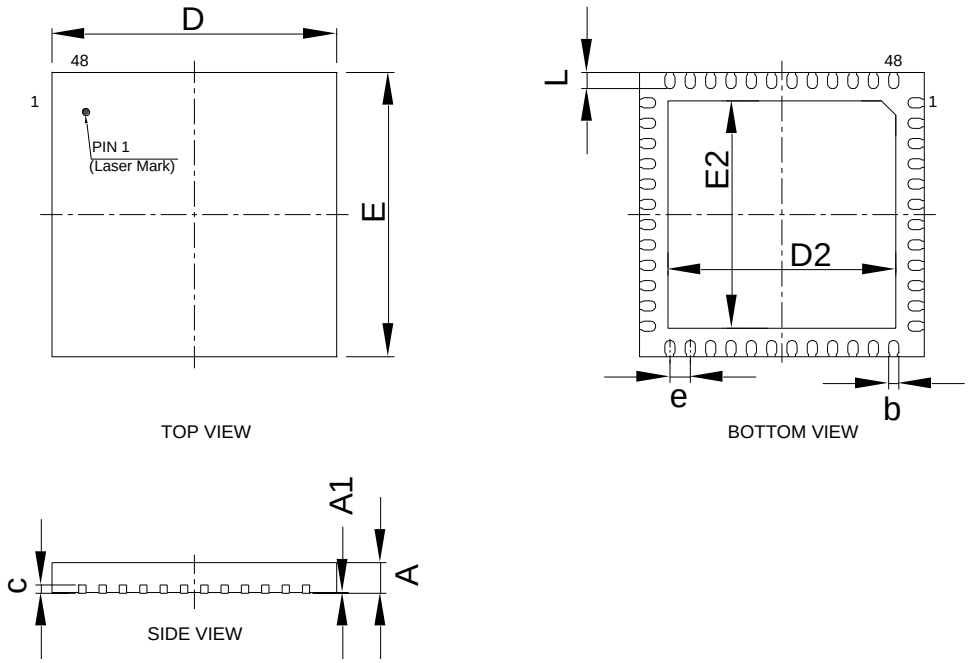
Figure 18 LQFP48 Welding Layout Suggestion



Note: Dimensions are marked in millimeters.

7.3 QFN48 Package Information

Figure 19 QFN48 Package Diagram



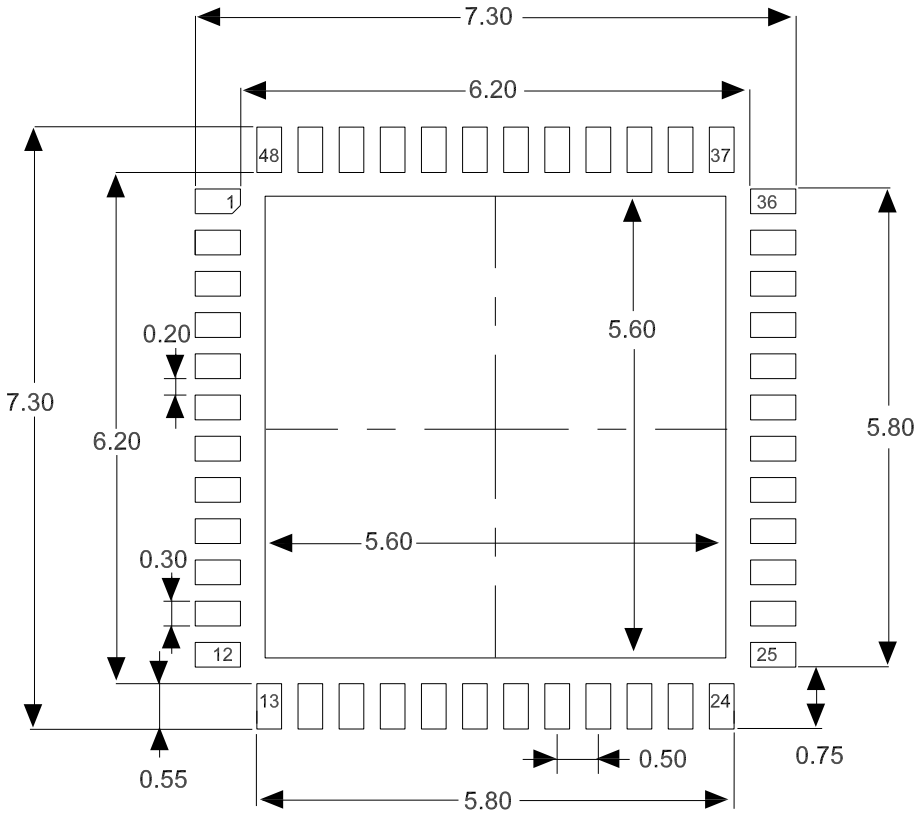
Note: The drawing is not drawn to scale.

Table 67 QFN48 Package Data

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.20	0.25	0.30
c	0.203REF		
e	0.50BSC		
D	6.90	7.00	7.10
D2	5.50	5.60	5.70
E	6.90	7.00	7.10
E2	5.50	5.60	5.70
L	0.35	0.40	0.45

Note: Dimensions are marked in millimeters.

Figure 20 QFN48 Welding Layout Suggestion

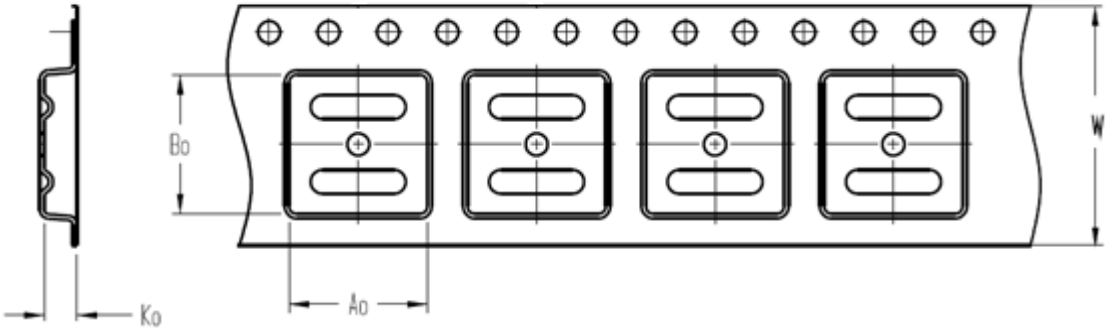


Note: Dimensions are marked in millimeters.

8 Packaging Information

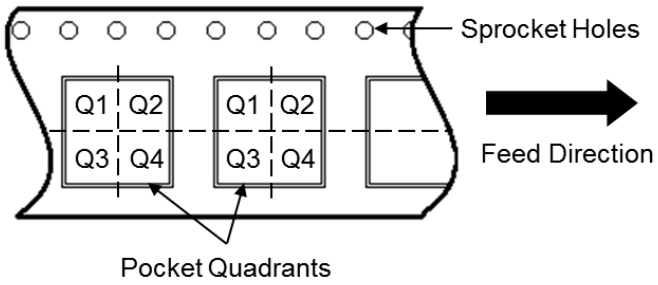
8.1 Reel Packaging

Figure 21 Reel Packaging Specification



A0	Dimensiondesignedtoaccommodatethecomponentwidth
B0	Dimensiondesignedtoaccommodatethecomponentlength
K0	Dimensiondesignedtoaccommodatethecomponentthickness
W	Overallwidthofthecarriertape

QuadrantAssignmentsforPIN1OrientationinTape



ReelDimensions

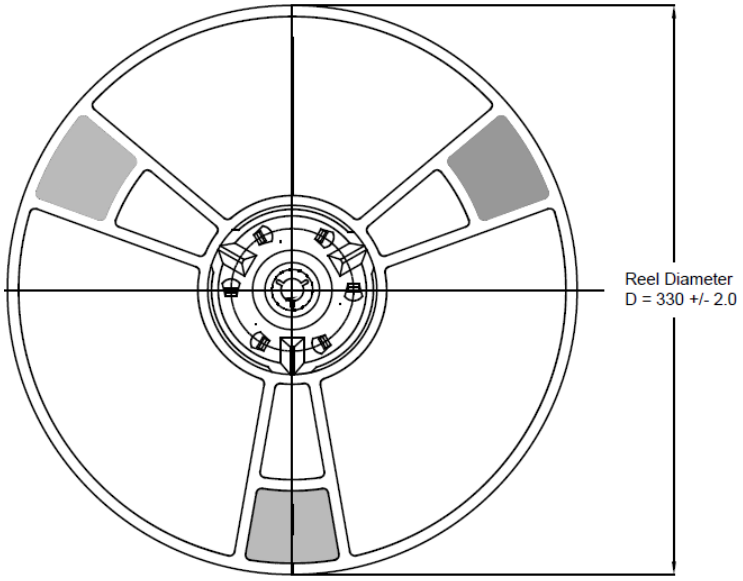
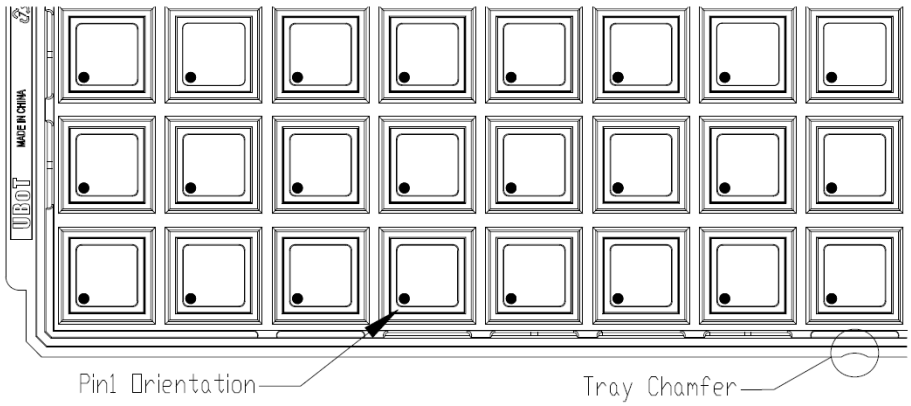


Table 68 Reel Packaging Parameter Specification Table

Device	Package Type	Pins	SPQ	ReelDiameter (mm)	A0 (mm)	B0 (mm)	K0 (mm)	W (mm)	Pin1 Quadrant
APM32F035C8T7	LQFP	48	2000	330	9.3	9.3	2.2	16	Q1

8.2 Tray Packaging

Figure 22 Tray Packaging Schematic Diagram



TrayDimensions

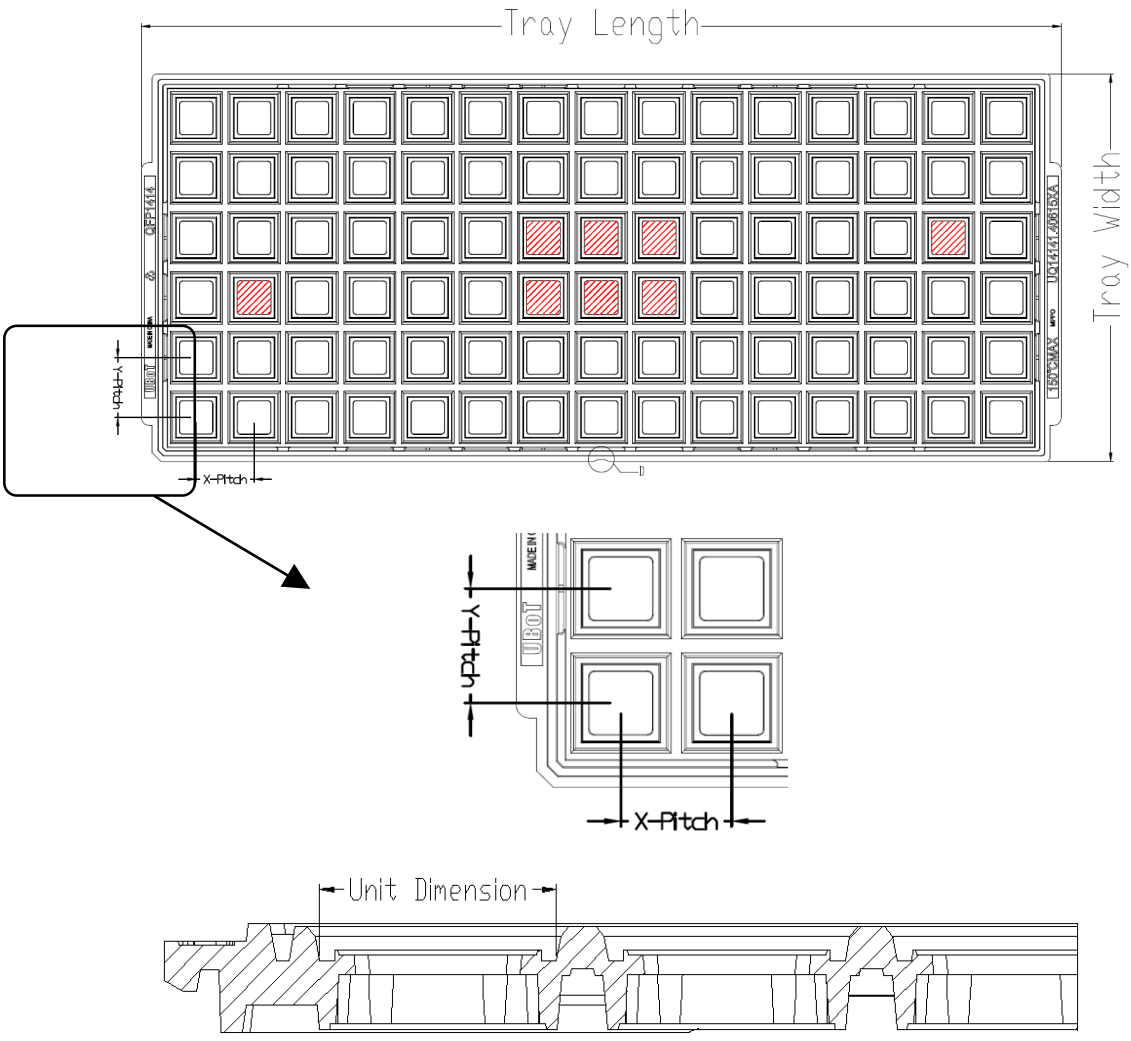
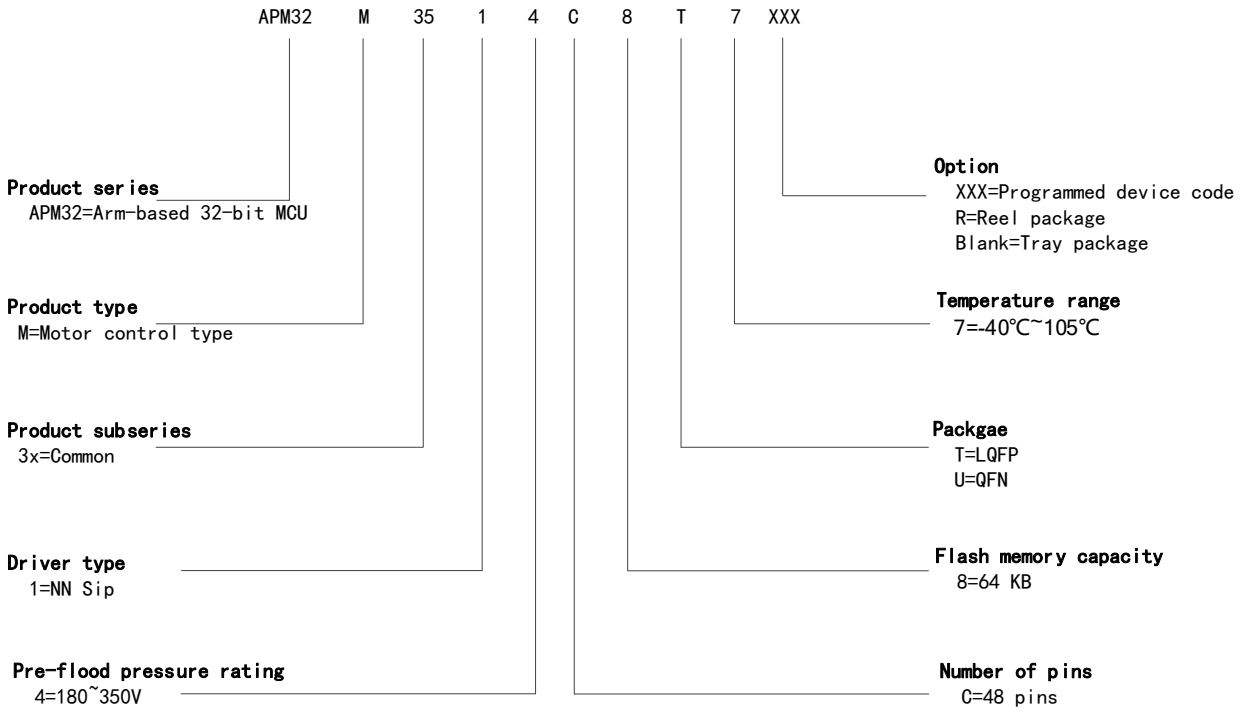

Tray Length
Tray Width
Y-Pitch
X-Pitch
UBOT
Unit Dimension

Table 69 Tray Packaging Parameters Specification Table

Device	Package Type	Pins	SPQ	X-Dimension (mm)	Y-DimensZion (mm)	X-Pitch (mm)	Y-Pitch (mm)	Tray Length (mm)	Tray Width (mm)
APM32M3514C8T7	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32M3514C8U7	QFN	48	2600	7.25	7.25	11.8	12.8	322.6	135.9
APM32F035C8T7	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9

9 Ordering Information

Figure 23 Naming Rules of Ordering Information



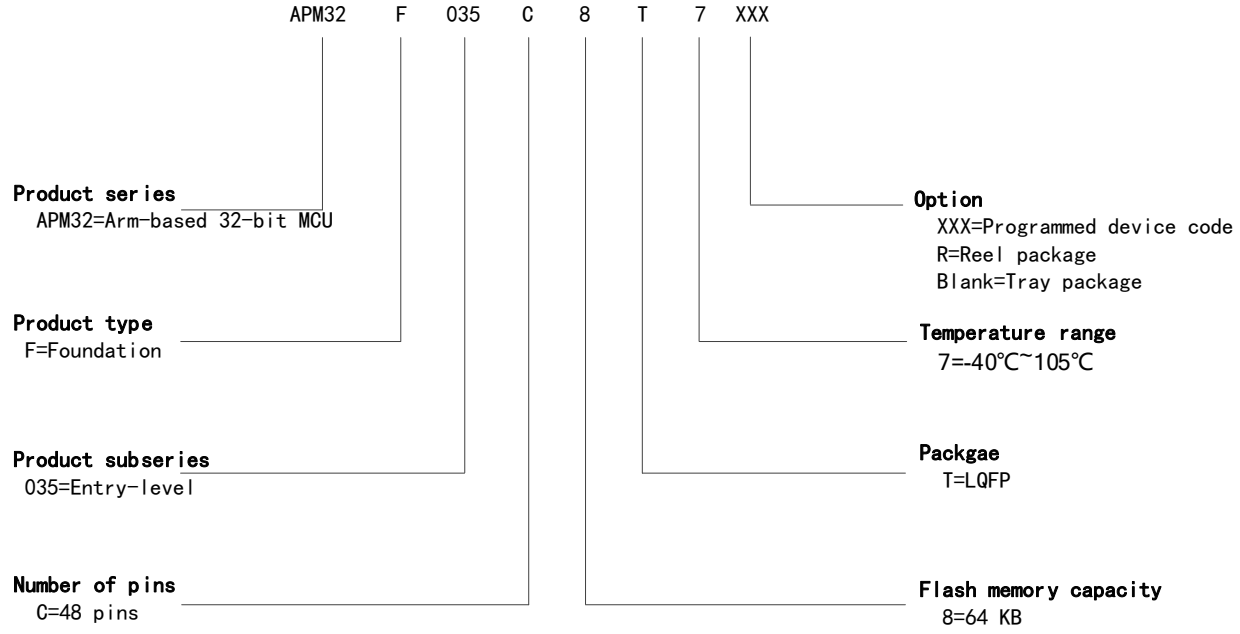


Table 70 List of Ordering Information

Order code	FLASH(KB)	SRAM(KB)	Package	SPQ	Temperature range
APM32F035C8T7-R	64	10	LQFP48	2000	-40℃~105℃

Order code	FLASH(KB)	SRAM(KB)	Package	SPQ	Temperature range
APM32F035C8T7	64	10	LQFP48	2500	-40℃~105℃
APM32M3514C8T7	64	10	LQFP48	2500	-40℃~105℃
APM32M3514C8U7	64	10	QFN48	2600	-40℃~105℃

Note: SPQ=Smallest Packaging Quantity

10 Naming of Common Functional Modules

Table 71Naming of Common Function Modules

Full name	Abbreviations
Reset management unit	RMU
Clock management unit	CMU
Reset and clock management unit	RCM
External interrupt	EINT
General IO	GPIO
Alternate function IO	AFIO
Wake up contReeler	WUPT
Independent watchdog timer	IWDT
Window watchdog timer	WWDT
Timer	TMR
CRC contReeler	CRC
Power management unit	PMU
DmacontReeler	DMA
Attack Damage Carry	ADC
Real-time clock	RTC
ContReeler area network	CAN
I2C interface	I2C
Serial peripheral interface	SPI
Universal asynchronous transceiver	UART
Universal asynchronous synchronous transceiver	USART
Flash interface control unit	FMC
Coprocessor	M0CP

11 Version history

Table 72 Document Version History

Date	Version	Change History
August 2023	0.1	New
January 2024	0.2	(1) Modify Product Characteristics (2) Add module description
July 2024	0.3	(1) Correct error descriptions (2) Adjust chapter order and format (3) Modify Electrical Characteristics
September 2024	0.9	(1) Supplement electrical parameters (2) Supplement ESD description
October 2024	0.10	(1) Add F035 Power Consumption (2) Add Flash erase cycle parameter

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