Datasheet

APM32F411xCxE

Arm® Cortex®-M4F Core-based 32-bit MCU

Version: V1.4

1 Product Characteristics

Core
- 32-bit Arm® Cortex ®-M4F core with FPU
- Up to 120MHz operating frequency

Memory and interface
- Flash: Up to 512KB
- SRAM: 128KB
- SMC: Support CF card, SRAM, PSRAM, NOR and NAND memories

Clock
- HSECLK: 4~26MHz external crystal/ceramic oscillator supported
- LSECLK: 32.768KHz crystal/ceramic oscillator supported
- HSICLK: 16MHz RC oscillator calibrated by factory
- LSICLK: 32KHz RC oscillator supported
- PLL1: Phase locked loop; output frequency is configured by four parameters
- PLL2: Phase locked loop specially used to provide clock signals to I2S; output frequency is configured by three parameters

Power supply and power supply management
- VDD range: 1.8～3.6V
- VDDA range: 1.8～3.6V
- VBAT range of backup domain power supply: 1.8V～3.6V
- Power-on/power-down/brown-out reset (POR/PDR/BOR) supported
- Programmable power supply voltage detector (PVD) supported

Low-power mode
- Sleep, stop and standby modes supported

DMA
- Two DMA; each DMA has 8 data streams, 16 in total

Debugging interface
- JTAG
- SWD

I/O
- Up to 81 I/O
- All I/O can be mapped to external interrupt vector
- Up to 77 FT input I/O

Communication peripherals
- Up to 4 USART, 2 UART, supporting ISO7816, LIN and IrDA functions
- Up to 3 I2C, supporting SMBus/PMBus
- Up to 5 SPI (5 reusable I2S)
- Up to 1 QSPI
- 2 CAN
- 1 USB_OTG controller
- 1 SDIO interface

Analog peripherals
- 2 12-bit ADC
- 2 comparators

Timer
- 2 16-bit advanced timers TMR1/8 that can provide 7-channel PWM output, support dead zone generation and braking input functions
- 2 32-bit general-purpose timers TMR2/5, each with up to 4 independent channels to support input capture, output compare, PWM, pulse count and other functions
- 8 16-bit general-purpose timers TMR3/4/9/10/11/12/13/14, each with up to 2 independent channels to support input capture, output compare, PWM, pulse count and other functions
- 2 watchdog timers: One independent watchdog IWDT and one window watchdog WWDT
- 1 24-bit autodecrement system timer SysTick Timer

RTC
- Support calendar function
- Support alarm and regular wake-up from stop/standby mode

CRC computing unit

96-bit unique device ID

Contents

2 Product information

See the following table for APM32F411xCxE product functions and peripheral configuration.

Table 1 Functions and Peripherals of APM32F411xCxE Series Chips

Product		**APM32F411xCxE**							
Model		CCU6	CEU6	CCT6	CET6	RCT6	RET6	VCT6	VET6
Package		QFN48		LQFP48		LQFP64		LQFP100	
Core and maximum working frequency		Arm® 32-bit Cortex®-M4F@120MHz							
Working voltage		1.8~3.6V							
Flash(KB)		256	512	256	512	256	512	256	512
SRAM(KB)		128							
GPIOs		36				50		81	
Communication interface	USART/UART	3/1				4/2			
	SPI/I2S	3				5			
	I2C	1		1		2		3	
	SMC	0						1	
	USB_OTG	1							
	CAN	2							
	QSPI	0				1			
	SDIO	1							
Timer	16-bit advanced	2							
	32-bit general-purpose	2							
	16-bit general	8							
	System tick timer	1							
	Watchdog	2							
Real-time clock		1							
12-bit ADC	Unit	2							
	Channel	10				16			
Comparator		2							
RNG		1							
Operating temperature		Ambient temperature: -40°C to 85°C Junction temperature: -40℃ to 105℃							

3 Pin information

3.1 Pin distribution

Figure 1 Distribution Diagram of APM32F411xCxE Series LQFP100 Pins

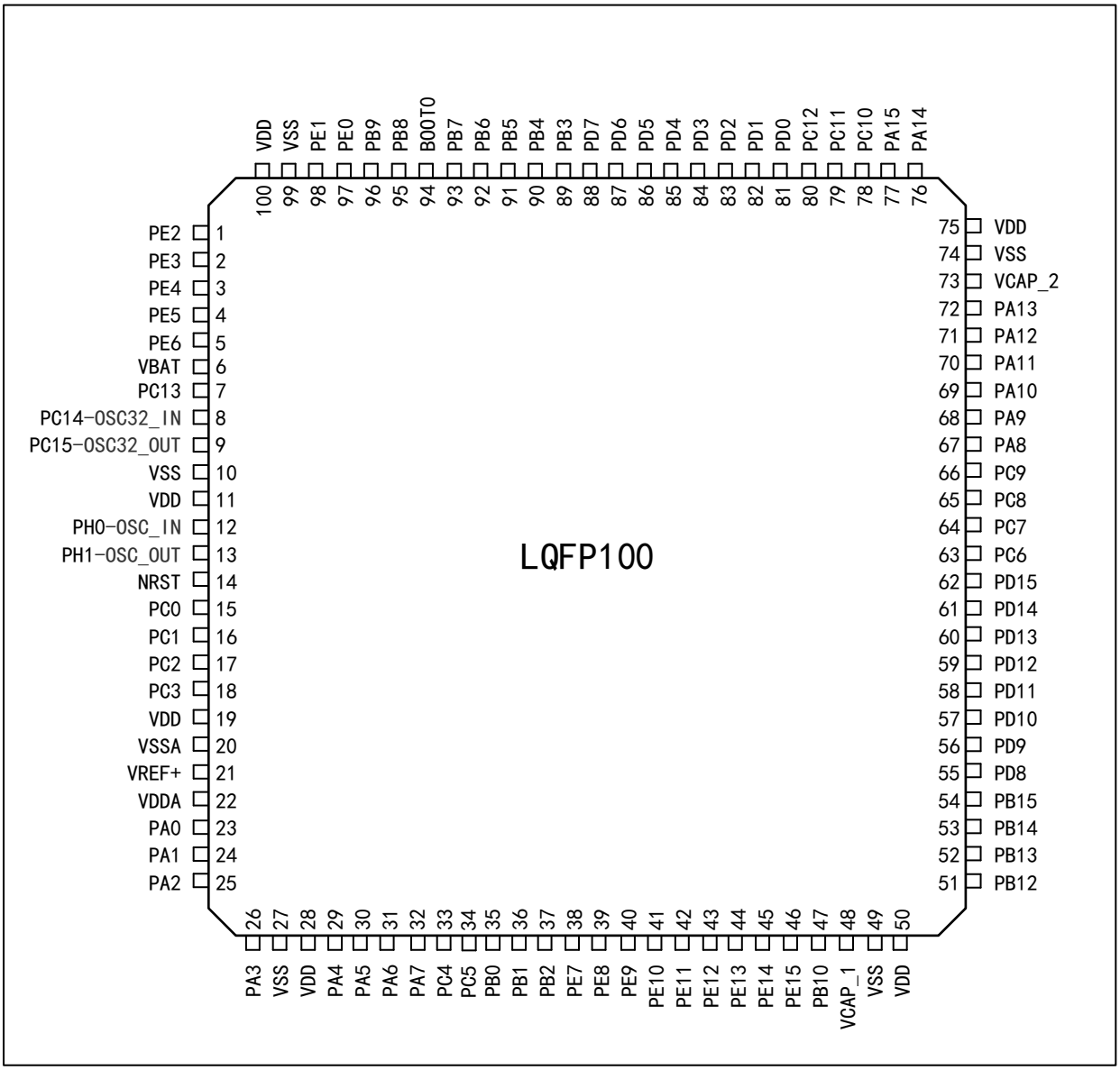


Figure 2 Distribution Diagram of APM32F411xCxE Series LQFP64 Pins

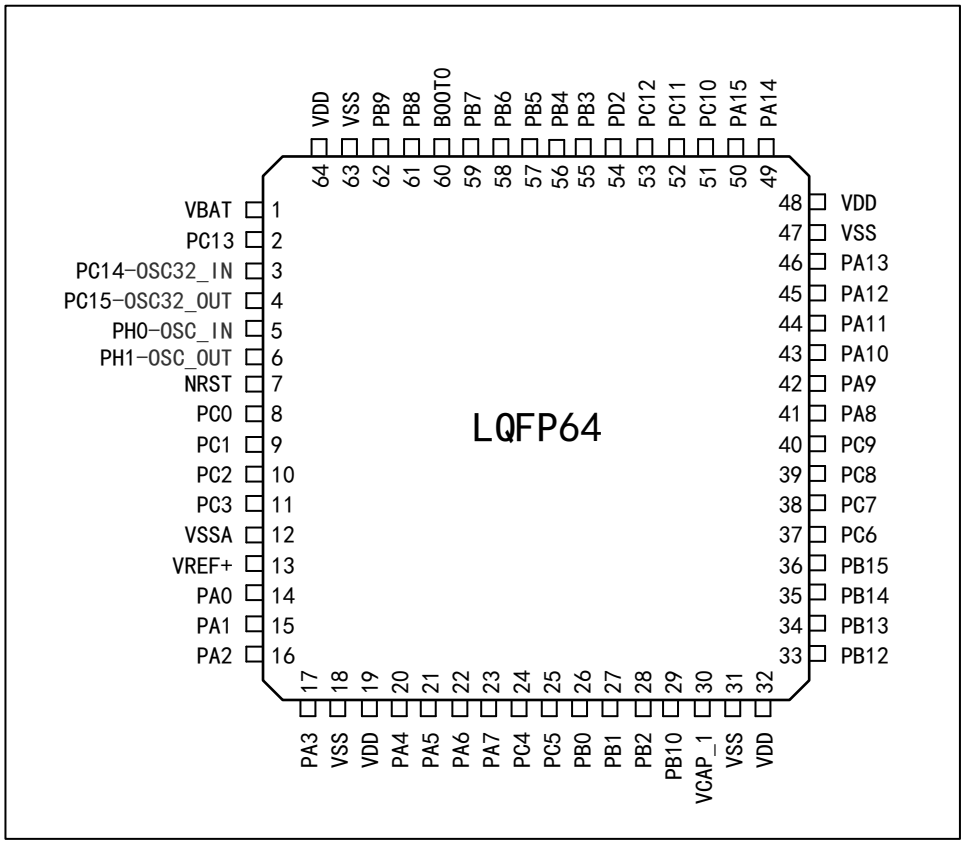


Figure 3 Distribution Diagram of APM32F411xCxE Series LQFP48 Pins

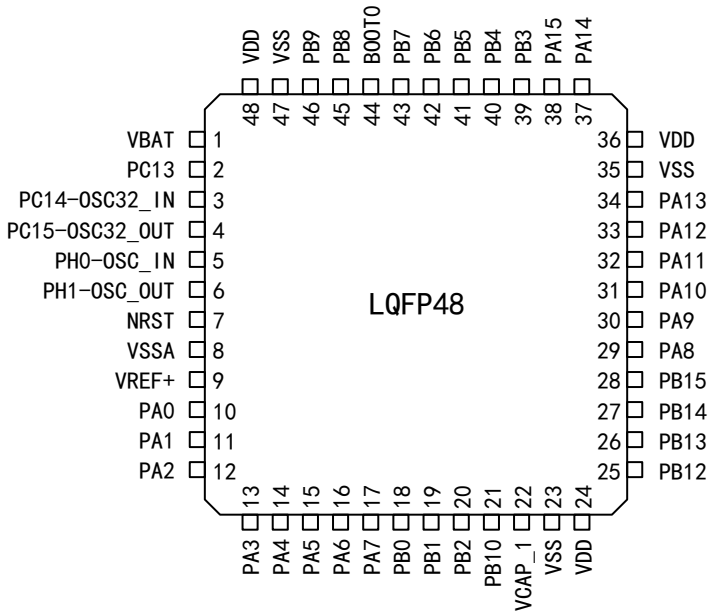
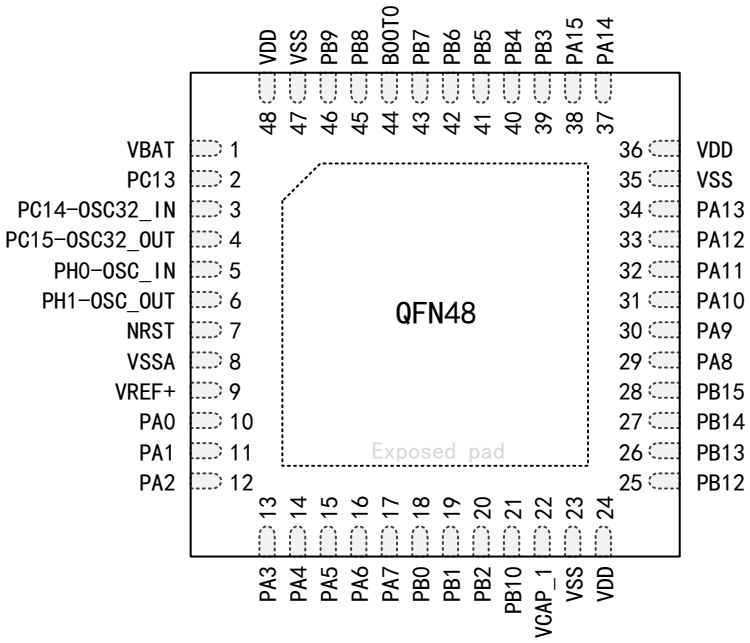


Figure 4 Distribution Diagram of APM32F411xCxE Series QFN48 Pins



3.2 Pin functional description

Table 2 Legends/Abbreviations Used in Output Pin Table

Name		Abbreviations	Definitions
Pin Name		Unless otherwise specified in the bracket below the pin name, the pin functions during and after reset are the same as the actual pin name	
Pin type		P	Power supply pin
		I	Only input pin
		I/O	I/O pin
I/O structure		5T	FT I/O
		STD	3.3V standard I/O
		B	Dedicated Boot0 pin
		RST	Bidirectional reset pin of built-in pull-up resistor
Cautions		Unless otherwise specified in the notes, all I/O is set as floating input during and after reset	
Pin function	Default multiplexing function	Select/enable this function directly through peripheral register	
	Redefining function	Select this function through AFIO remapping register	

Table 3 Description of APM32F411xCxE by Pin Number

Name (Function after reset)	Multiplexing function	Additional function	Type	Structure	LQFP100	LQFP64	LQFP48	QFN48
PE2	TRACECLK SPI4_SCK I2S4_CK SPI5_SCK I2S5_CK QSPI_IO2 SMC_A23 EVENTOUT	—	I/O	5T	1	—	—	—
PE3	TRACED0 SMC_A19 EVENTOUT	—	I/O	5T	2	—	—	—
PE4	TRACED1 SPI4_NSS I2S4_WS SPI5_NSS I2S5_WS SMC_A20 EVENTOUT	—	I/O	5T	3	—	—	—
PE5	TRACED2 TMR9_CH1 SPI4_MISO SPI5_MISO SMC_A21 EVENTOUT	—	I/O	5T	4	—	—	—
PE6	TRACED3 TMR9_CH2 SPI4_MOSI SPI4_SD SPI5_MOSI SPI5_SD SMC_A22 EVENTOUT	—	I/O	5T	5	—	—	—
VBAT	—	—	P	—	6	1	1	1
PC13	—	RTC_AMP1 RTC_TS RTC_OUT	I/O	5T	7	2	2	2
PC14-OSC32_IN (PC14)	—	OSC32_IN	I/O	5T	8	3	3	3

Name (Function after reset)	Multiplexing function	Additional function	Type	Structure	LQFP100	LQFP64	LQFP48	QFN48
PC15-OSC32_OUT (PC15)	—	OSC32_OUT	I/O	5T	9	4	4	4
VSS	—	—	I/O	5T	10	—	—	—
VDD	—	—	I/O	5T	11	—	—	—
PH0-OSC_IN (PH0)	—	OSC_IN	I/O	5T	12	5	5	5
PH1-OSC_OUT (PH1)	—	OSC_OUT	I/O	5T	13	6	6	6
NRST	—	—	I/O	5T	14	7	7	7
PC0	EVENTOUT	ADC1_IN10 ADC2_IN10 COMP1_INP	I/O	5T	15	8	—	—
PC1	EVENTOUT	ADC1_IN11 ADC2_IN11 COMP1_INM	I/O	5T	16	9	—	—
PC2	SPI2_MISO I2S2ext_SD SMC_NEW EVENTOUT	ADC1_IN12 ADC2_IN12 COMP2_INP	I/O	5Tf	17	10	—	—
PC3	SPI2_MOSI I2S2_SD SMC_A0 EVENTOUT	ADC1_IN13 ADC2_IN13 COMP1_INM	I/O	5Tf	18	11	—	—
VDD	—	—	P	—	19	—	—	—
VSSA	—	—	P	—	20	12	8	8
VREF+	—	—	P	—	21	13	9	9
VDDA	—	—	P	—	22	—	—	—
PA0	TMR2_CH1_ETR TMR5_CH1 TMR8_ETR USART2_CTS UART4_TX EVENTOUT	ADC1_IN0 ADC2_IN0	I/O	STD	23	14	10	10

Name (Function after reset)	Multiplexing function	Additional function	Type	Structure	LQFP100	LQFP64	LQFP48	QFN48
PA1	TMR2_CH2 TMR5_CH2 SPI4_MOSI I2S4_SD USART2_RTS UART4_RX QSPI_IO3 EVENTOUT	ADC1_IN1 ADC1_IN1	I/O	5T	24	15	11	11
PA2	TMR9_CH1 TMR5_CH3 TMR2_CH3 2S2_CKIN USART2_TX SMC_D4 EVENTOUT	ADC1_IN2 ADC2_IN2	I/O	5T	25	16	12	12
PA3	TMR9_CH2 TMR5_CH4 TMR2_CH4 I2S2_MCK USART2_RX SMC_D5 EVENTOUT	ADC1_IN3 ADC2_IN3	I/O	5T	26	17	13	13
VSS	—	—	P	—	27	18	—	—
VDD	—	—	P	—	28	19	—	—
PA4	SPI1_NSS SPI1_WS SPI3_NSS SPI3_WS USART2_CK SMC_D6 EVENTOUT	ADC1_IN4 ADC2_IN4	I/O	5T	29	20	14	14
PA5	TMR2_CH1_ETR TMR8_CH1N SPI1_SCK SMC_D7 EVENTOUT	ADC1_IN5 ADC2_IN5	I/O	STD	30	21	15	15

Name (Function after reset)	Multiplexing function	Additional function	Type	Structure	LQFP100	LQFP64	LQFP48	QFN48
PA6	TMR3_CH1 TMR1_BKIN TMR8_BKIN SPI1_MISO I2S2_MCK TMR13_CH1 SDIO_CMD EVENTOUT	ADC1_IN6 ADC2_IN6	I/O	5T	31	22	16	16
PA7	TMR1_CH1N TMR3_CH2 TMR8_CH1N SPI1_MOSI I2S1_SD TMR14_CH1 QSPI_IO1 EVENTOUT	ADC1_IN7 ADC2_IN7	I/O	5T	32	23	17	17
PC4	QSPI_IO2 SMC_NE4 EVENTOUT	ADC1_IN14 ADC2_IN14	I/O	5T	33	24	—	—
PC5	USART3_RX QSPI_IO3 SMC_NOE EVENTOUT	ADC1_IN15 ADC2_IN15	I/O	5T	34	25	—	—
PB0	TMR1_CH2N TMR3_CH3 TMR8_CH2N SPI5_SCK SMC_A24 EVENTOUT	ADC1_IN8 ADC2_IN8	I/O	5T	35	26	18	18
PB1	TMR1_CH3N TMR3_CH4 TMR8_CH3N SPI5_NSS SPI5_WS QSPI_CLK SMC_A25 EVENTOUT	ADC1_IN9 ADC2_IN9	I/O	5T	36	27	19	19
PB2	QSPI_CLK EVENTOUT	BOOT1	I/O	5T	37	28	20	20

Name (Function after reset)	Multiplexing function	Additional function	Type	Structure	LQFP100	LQFP64	LQFP48	QFN48
PE7	TMR1_ETR QSPI_IO0 SMC_D4 SMC_DA4 EVENTOUT	—	I/O	5T	38	—	—	—
PE8	TMR1_CH1N QSPI_IO1 SMC_D5 SMC_DA5 EVENTOUT	—	I/O	5T	39	—	—	—
PE9	TMR1_CH1 QSPI_IO2 SMC_D6 SMC_DA6 EVENTOUT	—	I/O	5T	40	—	—	—
PE10	TMR1_CH2N SMC_D7 SMC_DA7 EVENTOUT	—	I/O	5T	41	—	—	—
PE11	TMR1_CH2 SPI4_NSS SPI4_WS SPI5_NSS SPI5_WS SMC_D8 SMC_DA8 EVENTOUT	—	I/O	5T	42	—	—	—
PE12	TMR1_CH3N SPI4_SCK SPI5_SCK SMC_D9 SMC_DA9 EVENTOUT	—	I/O	5T	43	—	—	—
PE13	TMR1_CH3 SPI4_MISO SPI5_MISO SMC_D10 SMC_DA10 EVENTOUT	—	I/O	5T	44	—	—	—

Name (Function after reset)	Multiplexing function	Additional function	Type	Structure	LQFP100	LQFP64	LQFP48	QFN48
PE14	TMR1_CH4 SPI4_MOSI SPI4_SD SPI5_MOSI SPI5_SD SMC_D11 SMC_DA11 EVENTOUT	—	I/O	5T	45	—	—	—
PE15	TMR1_BKIN SMC_D12 SMC_DA12 EVENTOUT	—	I/O	5T	46	—	—	—
PB10	TMR2_CH3 I2C2_SCL SPI2_SCK I2S3_MCK USART3_TX SDIO_D7 EVENTOUT	—	I/O	5T	47	29	21	21
VCAP_1	—	—	I/O	5T	48	30	22	22
VSS	—	—	P	—	49	31	23	23
VDD	—	—	P	—	50	32	24	24
PB12	TMR1_BKIN I2C2_SMBA SPI2_NSS SPI2_WS SPI4_NSS SPI4_WS SPI3_SCK USART3_CK CAN2_RX SMC_D13 SMC_DA13 EVENTOUT	—	I/O	5T	51	33	25	25
PB13	TMR1_CH1N SPI2_SCK SPI4_SCK USART3_CTS CAN2_TX EVENTOUT	—	I/O	5Tf	52	34	26	26

Name (Function after reset)	Multiplexing function	Additional function	Type	Structure	LQFP100	LQFP64	LQFP48	QFN48
PB14	TMR1_CH2N TMR8_CH2N SPI2_MISO I2S2ext_SD USART3_RTS TMR12_CH1 SMC_D0 SDIO_D6 EVENTOUT	—	I/O	5Tf	53	35	27	27
PB15	RTC_50Hz TMR1_CH3N TMR8_CH3N SPI2_MOSI SPI2_SD TMR12_CH2 SDIO_CK EVENTOUT	RTC_REFIN	I/O	5T	54	36	28	28
PD8	USART3_TX SMC_D13 SMC_DA13 EVENTOUT	—	I/O	5T	55	—	—	—
PD9	USART3_RX SMC_D14 SMC_DA14 EVENTOUT	—	I/O	5T	56	—	—	—
PD10	USART3_CK SMC_D15 SMC_DA15 EVENTOUT	—	I/O	5T	57	—	—	—
PD11	USART3_CTS QSPI_IO0 SMC_A16 EVENTOUT	—	I/O	5T	58	—	—	—
PD12	TMR4_CH1 USART3_RTS QSPI_IO1 SMC_A17 EVENTOUT	—	I/O	5T	59	—	—	—

Name (Function after reset)	Multiplexing function	Additional function	Type	Structure	LQFP100	LQFP64	LQFP48	QFN48
PD13	TMR4_CH2 QSPI_IO3 SMC_A18 EVENTOUT	—	I/O	5T	60	—	—	—
PD14	TMR4_CH3 SMC_D0 SMC_DA0 EVENTOUT	—	I/O	5T	61	—	—	—
PD15	TMR4_CH4 SMC_D1 SMC_DA1 EVENTOUT	—	I/O	5T	62	—	—	—
PC6	TMR3_CH1 TMR8_CH1 I2S2_MCK USART6_TX SMC_D1 SDIO_D6 EVENTOUT	—	I/O	5T	63	37	—	—
PC7	TMR3_CH2 TMR8_CH2 SPI2_SCK I2S3_MCK USART6_RX SDIO_D7 EVENTOUT	—	I/O	5T	64	38	—	—
PC8	TMR3_CH3 TMR8_CH3 USART6_CK QSPI_IO2 SDIO_D0 EVENTOUT	—	I/O	5T	65	39	—	—
PC9	MCO_2 TMR3_CH4 TMR8_CH4 I2C3_SDA I2S2_CKIN QSPI_IO0 SDIO_D1 EVENTOUT	—	I/O	5T	66	40	—	—

Name (Function after reset)	Multiplexing function	Additional function	Type	Structure	LQFP100	LQFP64	LQFP48	QFN48
PA8	MCO_1 TMR1_CH1 I2C3_SCL USART1_CK USB_FS_SOF1 SDIO_D1 EVENTOUT	—	I/O	5T	67	41	29	29
PA9	TMR1_CH2 I2C3_SMBA USART1_TX USB_FS_VBUS SDIO_D2 EVENTOUT	—	I/O	5T	68	42	30	30
PA10	TMR1_CH3 SPI5_MOSI SPI5_SD USART1_RX USB_FS_ID EVENTOUT	—	I/O	5T	69	43	31	31
PA11	TMR1_CH4 SPI4_MISO USART1_CTS USART6_TX CAN1_RX USB_FS_DM SMC_NE2 EVENTOUT	—	I/O	5T	70	44	32	32
PA12	TMR1_ETR SPI5_MISO USART1_RTS USART6_RX CAN1_TX USB_FS_DP SMC_NE3 EVENTOUT	—	I/O	5T	71	45	33	33
PA13	JTMS-SWDIO EVENTOUT	—	I/O	5T	72	46	34	34
VCAP_2	—	—	P	—	73	—	—	—
VSS	—	—	P	—	74	47	35	35
VDD	—	—	P	—	75	48	36	36

Name (Function after reset)	Multiplexing function	Additional function	Type	Structure	LQFP100	LQFP64	LQFP48	QFN48
PA14	JTCK-SWCLK EVENTOUT	—	I/O	5T	76	49	37	37
PA15	JTDI TMR2_CH1_ETR SPI1_NSS SPI1_WS SPI3_NSS SPI3_WS USART1_TX EVENTOUT	—	I/O	5T	77	50	38	38
PC10	SPI3_SCK USART3_TX UART4_TX QSPI_IO1 SDIO_D2 EVENTOUT	-	I/O	5T	78	51	—	—
PC11	I2S3ext_SD SPI3_MISO USART3_RX UART4_RX QSPI_NCS SMC_D2 SDIO_D3 EVENTOUT	-	I/O	5T	79	52	—	—
PC12	SPI3_MOSI SPI3_SD USART3_CK UART5_TX SMC_D3 SDIO_CK EVENTOUT	-	I/O	5T	80	53	—	—
PD0	CAN1_RX SMC_D2 SMC_DA2 EVENTOUT	-	I/O	5T	81	—	—	—
PD1	CAN1_TX SMC_D3 SMC_DA3 EVENTOUT	—	I/O	5T	82	—	—	—

Name (Function after reset)	Multiplexing function	Additional function	Type	Structure	LQFP100	LQFP64	LQFP48	QFN48
PD2	TMR3_ETR UART5_RX SMC_NEW SDIO_CMD EVENTOUT	—	I/O	5T	83	54	—	—
PD3	SPI2_SCK USART2_CTS QSPI_CLK SMC_CLK EVENTOUT	—	I/O	5T	84	—	—	—
PD4	USART2_RTS SMC_NOE EVENTOUT	—	I/O	5T	85	—	—	—
PD5	USART2_TX SMC_NEW EVENTOUT	—	I/O	5T	86	—	—	—
PD6	SPI3_MOSI SPI3_SD USART2_RX SMC_NWAIT EVENTOUT	—	I/O	5T	87	—	—	—
PD7	USART2_CK SMC_NE1 EVENTOUT	—	I/O	5T	88	—	—	—
PB3	JTDO_SWO TMR2_CH2 SPI1_SCK SPI3_SCK USART1_RX I2C2_SDA EVENTOUT	-	I/O	5T	89	55	39	39
PB4	JTRST TMR3_CH1 SPI1_MISO SPI3_MISO I2S3ext_SD I2C3_SDA SDIO_D0 EVENTOUT	-	I/O	5Tf	90	56	40	40

Name (Function after reset)	Multiplexing function	Additional function	Type	Structure	LQFP100	LQFP64	LQFP48	QFN48
PB5	TMR3_CH2 I2C1_SMBA SPI1_MOSI SPI1_SD SPI3_MOSI SPI3_SD CAN2_RX SDIO_D3 EVENTOUT	-	I/O	5T	91	57	41	41
PB6	TMR4_CH1 I2C1_SCL USART1_TX CAN2_TX QSPI_NCS SDIO_D0 EVENTOUT	-	I/O	5Tf	92	58	42	42
PB7	TMR4_CH2 I2C1_SDA USART1_RX SMC_NL EVENTOUT	-	I/O	5Tf	93	59	43	43
BOOT0	—	VPP	I	—	94	60	44	44
PB8	TMR4_CH3 TMR10_CH1 I2C1_SCL SPI5_MOSI SPI5_SD CAN1_RX I2C3_SDA SDIO_D4 EVENTOUT	—	I/O	5Tf	95	61	45	45
PB9	TMR4_CH4 TMR11_CH1 I2C1_SDA SPI2_NSS CAN1_TX I2C2_SDA SDIO_D5 EVENTOUT	—	I/O	5Tf	96	62	46	46

Name (Function after reset)	Multiplexing function	Additional function	Type	Structure	LQFP100	LQFP64	LQFP48	QFN48
PE0	TMR4_ETR SMC_NBL0 EVENTOUT	—	I/O	5T	97	—	—	—
PE1	SMC_NBL1 EVENTOUT	—	I/O	5T	98	—	—	—
VSS	—	—	P	—	99	63	47	47
VDD	—	—	P	—	100	64	48	48

3.3 GPIO multiplexing function configuration

Table 4 GPIOA Multiplexing Function Configuration

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA0	-	TMR2_CH1_ETR	TMR5_CH1	TMR8_ETR	-	-	-	USART2_CTS	UART4_TX	-	-	-	-	-	-	EVENTOUT
PA1	-	TMR2_CH2	TMR5_CH2	-	-	SPI4_MOSI I2S4_SD	-	USART2_RTS	UART4_RX	QSPI_IO3	-	-	-	-	-	EVENTOUT
PA2	-	TMR2_CH3	TMR5_CH3	TMR9_CH1	-	I2S2_CKIN	-	USART2_TX	-	-	-	SMC_D4	-	-	-	EVENTOUT
PA3	-	TMR2_CH4	TMR5_CH4	TMR9_CH2	-	I2S2_MCK	-	USART2_RX	-	-		SMC_D5	-	-	-	EVENTOUT
PA4	-	-	-	-	-	SPI1_NSS I2S1_WS	SPI3_NSS I2S3_WS	USART2_CK	-	-	-	SMC_D6	-	-	-	EVENTOUT
PA5	-	TMR2_CH1_ETR	-	TMR8_CH1N	-	SPI1_SCK I2S1_CK	-	-	-	-	-	SMC_D7	-	-	-	EVENTOUT
PA6	-	TMR1_BKIN	TMR3_CH1	TMR8_BKIN	-	SPI1_MISO	I2S2_MCK	-	-	TMR13_CH1	-	SDIO_CMD	-	-	-	EVENTOUT
PA7	-	TMR1_CH1N	TMR3_CH2	TMR8_CH1N	-	SPI1_MOSI	-	-	-	TMR14_CH1	QSPI_IO1	-	-	-	-	EVENTOUT

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
						I2S1_SD										
PA8	MCO_1	TMR1_CH1	-	-	I2C3_SCL	-	-	USART1_CK	-	-	USB_FS_SOF	SDIO_D1	-	-	-	EVENTOUT
PA9	-	TMR1_CH2	-	-	I2C3_SMBA	-	-	USART1_TX	-	-	USB_FS_VBUS	SDIO_D2	-	-	-	EVENTOUT
PA10	-	TMR1_CH3	-	-	-	-	SPI5_MOSI I2S5_SD	USART1_RX	-	-	OTG_FS_ID	-	-	-	-	EVENTOUT
PA11	-	TMR1_CH4	-	-	-	-	SPI4_MISO	USART1_CTS	USART6_TX	CAN1_RX	OTG_FS_DM	SMC_NE2	-	-	-	EVENTOUT
PA12	-	TMR1_ETR	-	-	-	-	SPI5_MISO	USART1_RTS	USART6_RX	CAN1_TX	OTG_FS_DP	SMC_NE3	-	-	-	EVENTOUT
PA13	JTMS_SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
PA14	JTCK_SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
PA15	JTDI	TMR2_CH1_ETR	-	-	-	SPI1_NSS I2S1_WS	SPI3_NSS I2S3_WS	USART1-TX	-	-	-	-	-	-	-	EVENTOUT

Table 5 GPIOB Multiplexing Function Configuration

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB0	-	TMR1_CH2N	TMR3_CH3	TMR8_CH2N	-	-	SPI5_SCK I2S5_CK	-	-	-		SMC_A24	-	-	-	EVENTOUT
PB1	-	TMR1_CH3N	TMR3_CH4	TMR8_CH3N	-	-	SPI5_NSS I2S5_WS	-	-	QSPI_CLK		SMC_A25	-	-	-	EVENTOUT
PB2	-	-	-	-	-	-	-	-	-	QSPI_CLK	-	-	-	-	-	EVENTOUT
PB3	JTDO_SWO	TMR2_CH2	-	-	-	SPI1_SCK I2S1_CK	SPI3_SCK I2S3_CK	USART1_RX	-	I2C2_SDA	-	-	-	-	-	EVENTOUT
PB4	JTRST	-	TMR3_CH1	-	-	SPI1_MISO	SPI3_MISO	I2S3ext_SD	-	I2C3_SDA	-	SDIO_D0	-	-	-	EVENTOUT
PB5	-	-	TMR3_CH2	-	I2C1_SMBA	SPI1_MOSI I2S1_SD	SPI3_MOSI I2S3_SD	-	-	CAN2_RX		SDIO_D3	-	-	-	EVENTOUT
PB6	-	-	TMR4_CH1	-	I2C1_SCL	-	-	USART1_TX	-	CAN2_TX	QSPI_NCS	SDIO_D0	-	-	-	EVENTOUT
PB7	-	-	TMR4_CH2	-	I2C1_SDA	-	-	USART1_RX	-	-	-	SMC_NL	-	-	-	EVENTOUT
PB8	-	-	TMR4_CH3	TMR10_CH1	I2C1_SCL	-	SPI5_MOSI I2S5_SD	-	CAN1_RX	I2C3_SDA	-	SDIO_D4	-	-	-	EVENTOUT
PB9	-	-	TMR4_CH4	TMR11_CH1	I2C1_SDA	SPI2_NSS I2S2_WS	-	-	CAN1_TX	I2C2_SDA	-	SDIO_D5	-	-	-	EVENTOUT

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB10	-	TMR2_CH3	-	-	I2C2_SCL	SPI2_SCK I2S2_CK	I2S3_MCK	USART3_TX	-	-	-	SDIO_D7	-	-	-	EVENTOUT
NC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PB12	-	TMR1_BKIN	-	-	I2C2_SMBA	SPI2_NSS I2S2_WS	SPI4_NSS I2S4_WS	SPI3_SCK I2S3_CK	USART3_CK	CAN2_RX	-	SMC_D13 SMC_DA13	-	-	-	EVENTOUT
PB13	-	TMR1_CH1N	-	-	-	SPI2_SCK I2S2_CK	SPI4_SCK I2S4_CK	-	USART3_CTS	CAN2_TX	-	-	-	-	-	EVENTOUT
PB14	-	TMR1_CH2N	-	TMR8_CH2N	-	SPI2_MISO	I2S2ext_SD	USART3_RTS	-	TMR12_CH1	SMC_D0	SDIO_D6	-	-	-	EVENTOUT
PB15	RTC_50HZ	TMR1_CH3N	-	TMR8_CH3N	-	SPI2_MOSI I2S2_SD	-	-	-	TMR12_CH2	-	SDIO_CK	-	-	-	EVENTOUT

Table 6 GPIOC Multiplexing Function Configuration

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PC1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PC2	-	-	-	-	-	SPI2_MISO	I2S2ext_SD	-	-	-	-	SMC_NEW	-	-	-	EVENT OUT
PC3	-	-	-	-	-	SPI2_MOSI I2S2_SD	-	-	-	-	-	SMC_A0	-	-	-	EVENT OUT
PC4	-	-	-	-	-	-	-	-	-	-	QSPI_IO2	SMC_NE4	-	-	-	EVENT OUT
PC5	-	-	-	-	-	-	-	USART3_RX	-	-	QSPI_IO3	SMC_NOE	-	-	-	EVENT OUT
PC6	-	-	TMR3_CH1	TMR8_CH1	-	I2S2_MCK	-	-	USART6_TX	-	SMC_D1	SDIO_D6	-	-	-	EVENT OUT
PC7	-	-	TMR3_CH2	TMR8_CH2	-	SPI2_SCK I2S2_CK	I2S3_MCK	-	USART6_RX	-	-	SDIO_D7	-	-	-	EVENT OUT
PC8	-	-	TMR3_CH3	TMR8_CH3	-	-	-	-	USART6_CK	QSPI_IO2	-	SDIO_D0	-	-	-	EVENT OUT
PC9	MCO_2	-	TMR3_CH4	TMR8_CH4	I2C3_SDA	I2S2_CKIN	-	-	-	QSPI_IO0	-	SDIO_D1	-	-	-	EVENT OUT
PC10	-	-	-	-	-	-	SPI3_SCK I2S3_CK	USART3_TX	UART4_TX	QSPI_IO1	-	SDIO_D2	-	-	-	EVENT OUT

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC11	-	-	-	-	-	I2S3ext_SD	SPI3_MISO	USART3_RX	UART4_RX	QSPI_NCS	SMC_D2	SDIO_D3	-	-	-	EVENTOUT
PC12	-	-	-	-	-	-	SPI3_MOSI I2S3_SD	USART3_CK	UART5_TX	-	SMC_D3	SDIO_CK	-	-	-	EVENTOUT
PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Table 7 GPIOD Multiplexing Function Configuration

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PD0	-	-	-	-	-	-	-	-	-	CAN1_RX	-	SMC_D2 SMC_DA2	-	-	-	EVENT OUT
PD1	-	-	-	-	-	-	-	-	-	CAN1_TX	-	SMC_D3 SMC_DA3	-	-	-	EVENT OUT
PD2	-	-	TMR3_E TR	-	-	-	-	-	UART5_RX	-	SMC_NEW	SDIO_CMD	-	-	-	EVENT OUT
PD3	-	-	-	-	-	SPI2_SCK I2S2_CK	-	USART2_CTS	-	QSPI_CLK	-	SMC_CLK	-	-	-	EVENT OUT
PD4	-	-	-	-	-	-	-	USART2_RTS	-	-	-	SMC_NOE	-	-	-	EVENT OUT
PD5	-	-	-	-	-	-	-	USART2_TX	-	-	-	SMC_NEW	-	-	-	EVENT OUT
PD6	-	-	-	-	-	SPI3_MOSI I2S3_SD	-	USART2_RX	-	-	-	SMC_NWAIT	-	-	-	EVENT OUT
PD7	-	-	-	-	-	-	-	USART2_CK	-	-	-	SMC_NE1	-	-	-	EVENT OUT
PD8	-	-	-	-	-	-	-	USART3_TX	-	-	-	SMC_D13 SMC_DA13	-	-	-	EVENT OUT
PD9	-	-	-	-	-	-	-	USART3_RX	-	-	-	SMC_D14 SMC_DA14	-	-	-	EVENT OUT
PD10	-	-	-	-	-	-	-	USART3_CK	-	-	-	SMC_D15 SMC_DA15	-	-	-	EVENT OUT
PD11	-	-	-	-	-	-	-	USART3_CTS	-	QSPI_IO0	-	SMC_A16	-	-	-	EVENT OUT
PD12	-	-	TMR4_C H1	-	-	-	-	USART3_RTS	-	QSPI_IO1	-	SMC_A17	-	-	-	EVENT OUT

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PD13	-	-	TMR4_CH2	-	-	-	-	-	-	QSPI_IO3	-	SMC_A18	-	-	-	EVENTOUT
PD14	-	-	TMR4_CH3	-	-	-	-	-	-	-	-	SMC_D0 SMC_DA0	-	-	-	EVENTOUT
PD15	-	-	TMR4_CH4	-	-	-	-	-	-	-	-	SMC_D1 SMC_DA1	-	-	-	EVENTOUT

Table 8 GPIOE Multiplexing Function Configuration

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PE0	-	-	TMR4_ETR	-	-	-	-	-	-	-	-	SMC_NBL0	-	-	-	EVENTOUT
PE1	-	-	-	-	-	-	-	-	-	-	-	SMC_NBL1	-	-	-	EVENTOUT
PE2	TRACECLK	-	-	-	-	SPI4_SCK I2S4_CK	SPI5_SCK I2S5_CK	-	-	QSPI_IO2	-	SMC_A23	-	-	-	EVENTOUT
PE3	TRACED0	-	-	-	-	-	-	-	-	-	-	SMC_A19	-	-	-	EVENTOUT
PE4	TRACED1	-	-	-	-	SPI4_NSS I2S4_WS	SPI5-NSS I2S5_WS	-	-	-	-	SMC_A20	-	-	-	EVENTOUT
PE5	TRACED2	-	-	TMR9_CH1	-	SPI4_MISO	SPI5_MISO	-	-	-	-	SMC_A21	-	-	-	EVENTOUT
PE6	TRACED3	-	-	TMR9_CH2	-	SPI4_MOSI I2S4_SD	SPI5_MOSI I2S5_SD	-	-	-	-	SMC_A22	-	-	-	EVENTOUT
PE7	-	TMR1_ETR	-	-	-	-	-	-	-	-	QSPI_IO0	SMC_D4 SMC_DA4	-	-	-	EVENTOUT
PE8	-	TMR1_CH1N	-	-	-	-	-	-	-	-	QSPI_IO1	SMC_D5 SMC_DA5	-	-	-	EVENTOUT
PE9	-	TMR1_CH1	-	-	-	-	-	-	-	-	QSPI_IO2	SMC_D6 SMC_DA6	-	-	-	EVENTOUT
PE10	-	TMR1_CH2N	-	-	-	-	-	-	-	-	-	SMC_D7 SMC_DA7	-	-	-	EVENTOUT
PE11	-	TMR1_CH2	-	-	-	SPI4_NSS I2S4_WS	SPI5_NSS I2S5_WS	-	-	-	-	SMC_D8 SMC_DA8	-	-	-	EVENTOUT
PE12	-	TMR1_CH3N	-	-	-	SPI4_SCK I2S4_CK	SPI5_SCK I2S5_CK	-	-	-	-	SMC_D9 SMC_DA9	-	-	-	EVENTOUT

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PE13	-	TMR1_CH3	-	-	-	SPI4_MISO	SPI5_MISO	-	-	-	-	SMC_D10 SMC_DA10	-	-	-	EVENTOUT
PE14	-	TMR1_CH4	-	-	-	SPI4_MOSI I2S4_SD	SPI5_MOSI I2S5_SD	-	-	-	-	SMC_D11 SMC_DA11	-	-	-	EVENTOUT
PE15	-	TMR1_BKIN	-	-	-	-	-	-	-	-	-	SMC_D12 SMC_DA12	-	-	-	EVENTOUT

Table 9 GPIOH Multiplexing Function Configuration

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PH1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

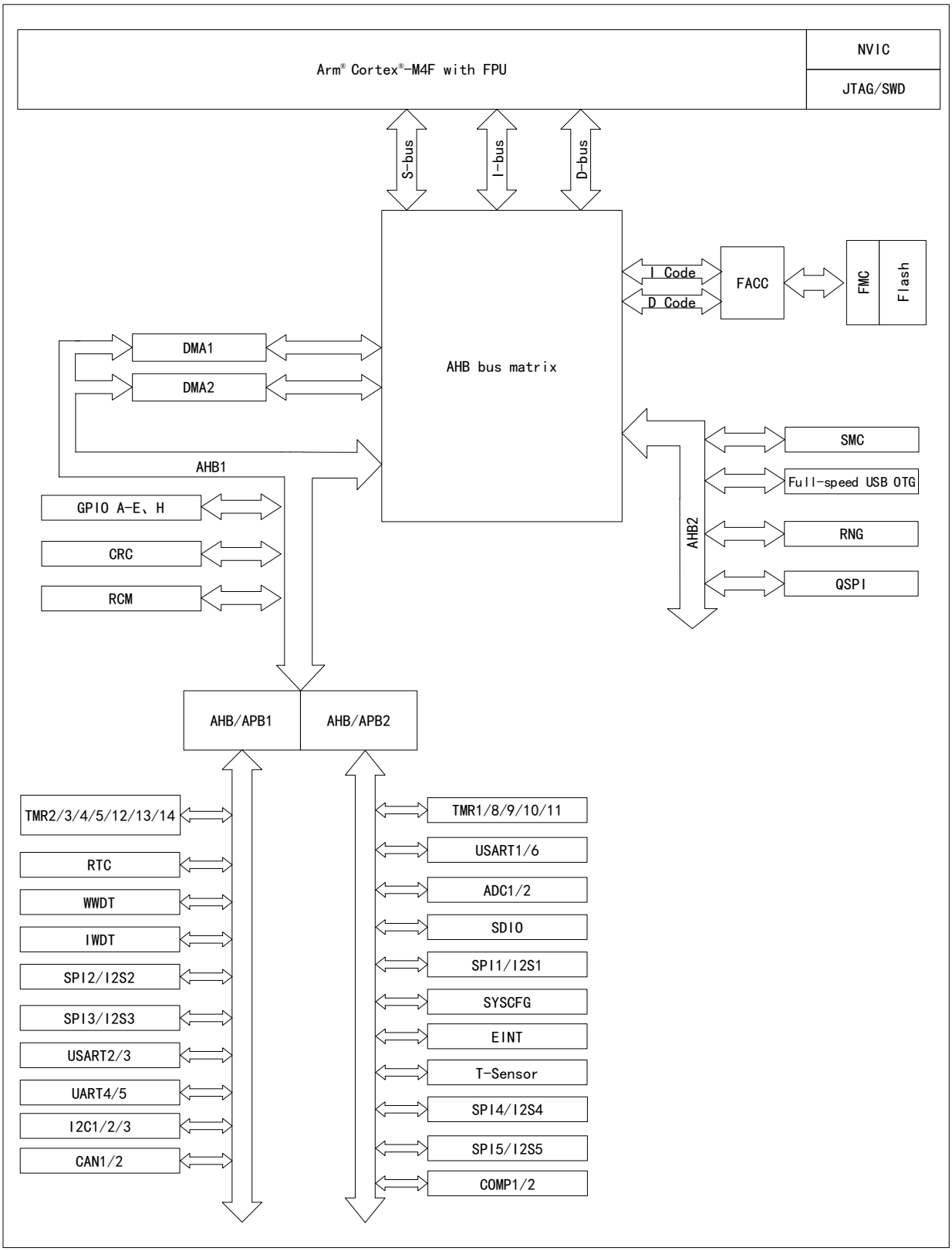
4 Functional Description

This chapter mainly introduces the system architecture, interrupt, on-chip memory, clock, power supply and peripheral features of APM32F411xCxE series products; for information about the Arm® Cortex®-M4F core, please refer to the *Arm® Cortex® -M4F Technical Reference Manual*, which can be downloaded from ARM's website.

4.1 System architecture

4.1.1 System block diagram

Figure 5 APM32F411xCxE System Block Diagram



4.1.2 Address mapping

Table 10 Address Mapping Table of APM32F411xCxE Series

Region	Start address	Peripheral name
Code	0x0000 0000	Code mapping area
Code	0x0008 0000	Reserved
Code	0x0800 0000	FLASH
Code	0x0808 0000	Reserved
CCM	0x1000 0000	CCM(SRAM)
Code	0x1001 0000	Reserve
Code	0x1FFF 0000	System memory area
Code	0x1FFF 7800	OTP area
Code	0x1FFF C000	Option byte
Code	0x1FFF F008	Reserved
SRAM	0x2000 0000	SRAM
APB 1 bus	0x4000 0000	TMR2
APB 1 bus	0x4000 0400	TMR3
APB 1 bus	0x4000 0800	TMR4
APB 1 bus	0x4000 0C00	TMR5
APB 1 bus	0x4000 1800	TMR12
APB 1 bus	0x4000 1C00	TMR13
APB 1 bus	0x4000 2000	TMR14
APB 1 bus	0x4000 2400	Reserved
APB 1 bus	0x4000 2800	RTC
APB 1 bus	0x4000 2C00	WWDT
APB 1 bus	0x4000 3000	IWDT
APB 1 bus	0x4000 3400	I2S2ext
APB 1 bus	0x4000 3800	SPI2/I2S2
APB 1 bus	0x4000 3C00	SPI3/I2S3
APB 1 bus	0x4000 4000	I2S3ext
APB 1 bus	0x4000 4400	USART2
APB 1 bus	0x4000 4800	USART3
APB 1 bus	0x4000 4C00	UART4
APB 1 bus	0x4000 5000	UART5
APB 1 bus	0x4000 5400	I2C1
APB 1 bus	0x4000 5800	I2C2
APB 1 bus	0x4000 5C00	I2C3
APB 1 bus	0x4000 6000	Reserved
APB 1 bus	0x4000 6400	CAN1
APB 1 bus	0x4000 6800	CAN2

Region	Start address	Peripheral name
APB 1 bus	0x4000 6C00	Reserved
APB 1 bus	0x4000 7000	PMU
APB 1 bus	0x4000 7800	Reserved
—	0x4000 8000	Reserved
APB2 bus	0x4001 0000	TMR1
APB2 bus	0x4001 0400	TMR8
APB2 bus	0x4001 0800	Reserved
APB2 bus	0x4001 1000	USART1
APB2 bus	0x4001 1400	USART6
APB2 bus	0x4001 1800	Reserved
APB2 bus	0x4001 2000	ADC1
APB2 bus	0x4001 2400	ADC2
APB2 bus	0x4001 2C00	SDIO
APB2 bus	0x4001 3000	SPI1/I2S1
APB2 bus	0x4001 3400	SPI4/I2S4
APB2 bus	0x4001 3800	SYSCFG
APB2 bus	0x4001 3818	COMP1
APB2 bus	0x4001 381C	COMP2
APB2 bus	0x4001 3C00	EINT
APB2 bus	0x4001 4000	TMR9
APB2 bus	0x4001 4400	TMR10
APB2 bus	0x4001 4800	TMR11
APB2 bus	0x4001 5000	SPI5/I2S5
APB2 bus	0x4001 5400	Reserved
—	0x4001 5800	Reserved
AHB1 bus	0x4002 0000	GPIOA
AHB1 bus	0x4002 0400	GPIOB
AHB1 bus	0x4002 0800	GPIOC
AHB1 bus	0x4002 0C00	GPIOD
AHB1 bus	0x4002 1000	GPIOE
AHB1 bus	0x4002 1400	Reserved
AHB1 bus	0x4002 1C00	GPIOH
AHB1 bus	0x4002 1400	Reserved
AHB1 bus	0x4002 3000	CRC
AHB1 bus	0x4002 3400	Reserved
AHB1 bus	0x4002 3800	RCM
AHB1 bus	0x4002 3C00	FLASH Reg.
AHB1 bus	0x4002 5000	Reserved

Region	Start address	Peripheral name
AHB1 bus	0x4002 6000	DMA1
AHB1 bus	0x4002 6400	DMA2
AHB1 bus	0x4002 6800	Reserved
AHB2 bus	0x5000 0000	USB OTG_FS
AHB2 bus	0x5004 0000	Reserved
AHB2 bus	0x5006 0800	RNG
AHB2 bus	0x6000 0000	SMC
AHB2 bus	0xA000 0000	SMC Reg
AHB2 bus	0xA000 1000	QSPI Reg
AHB2 bus	0xB000 0000	QSPI
Core	0xE000 0000	Core peripheral
—	0xE010 0000	Reserved

4.1.3 Startup configuration

At startup, the user can select one of the following three startup modes by setting the high and low levels of the Boot pin:

- Startup from main memory
- Startup from BootLoader
- Startup from built-in SRAM

To start up from BootLoader, the user can use serial interface to reprogram the user Flash .

4.2 Core

The core of APM32F411xCxE is Arm® Cortex®-M4F with FPU computing unit. Based on this platform, the development cost is low and the power consumption is low. It can provide excellent computing performance and advanced system interrupt response, and is compatible with all ARM tools and software.

4.3 Interrupt controller

4.3.1 Nested Vector Interrupt Controller (NVIC)

It is embedded with a nested vectored interrupt controller (NVIC) able to handle up to 75 maskable interrupt channels (not including 16 interrupt lines of Cortex®-M4F) and 8 priority levels. The interrupt vector entry address can be directly transmitted to the core, so that the interrupt response processing with low delay can give priority to the late higher priority interrupt.

4.3.2 External Interrupt/Event Controller (EINT)

The external interrupt/event controller consists of 21 edge detectors, and each detector includes edge detection circuit and interrupt/event request generation circuit; each detector can

be configured as rising edge trigger, falling edge trigger or both and can be masked independently. Up to 81 GPIO can be connected to 16 external interrupt lines.

4.4 On-chip memory

On-chip memory includes main memory area, SRAM and information block; the information block includes system memory area and option byte; the system memory area stores BootLoader, 96-bit unique device ID and capacity information of main memory area; the system memory area has been written to the program when leaving the factory and cannot be erased.

Table 11 On-chip Memory Area

Memory	Maximum capacity	Function
Main memory area	512KB	Store user programs and data
SRAM	128KB	CPU can access at 0 wait cycle (read/write)
System memory area	30KB	Store BootLoader, 96-bit unique device ID, and main memory area capacity information
Option byte	16Bytes	Configure main memory area read-write protection and MCU working mode

4.4.1 Static Memory Controller (SMC)

APM32F411xCxE series integrates SMC module, and supports PC card, SRAM, PSRAM, NorFlash and NandFlash.

Functional introduction:

- Write FIFO
- The maximum synchronous access frequency is 60MHz.
- Connect to LCD

4.4.2 LCD parallel interface (LCD)

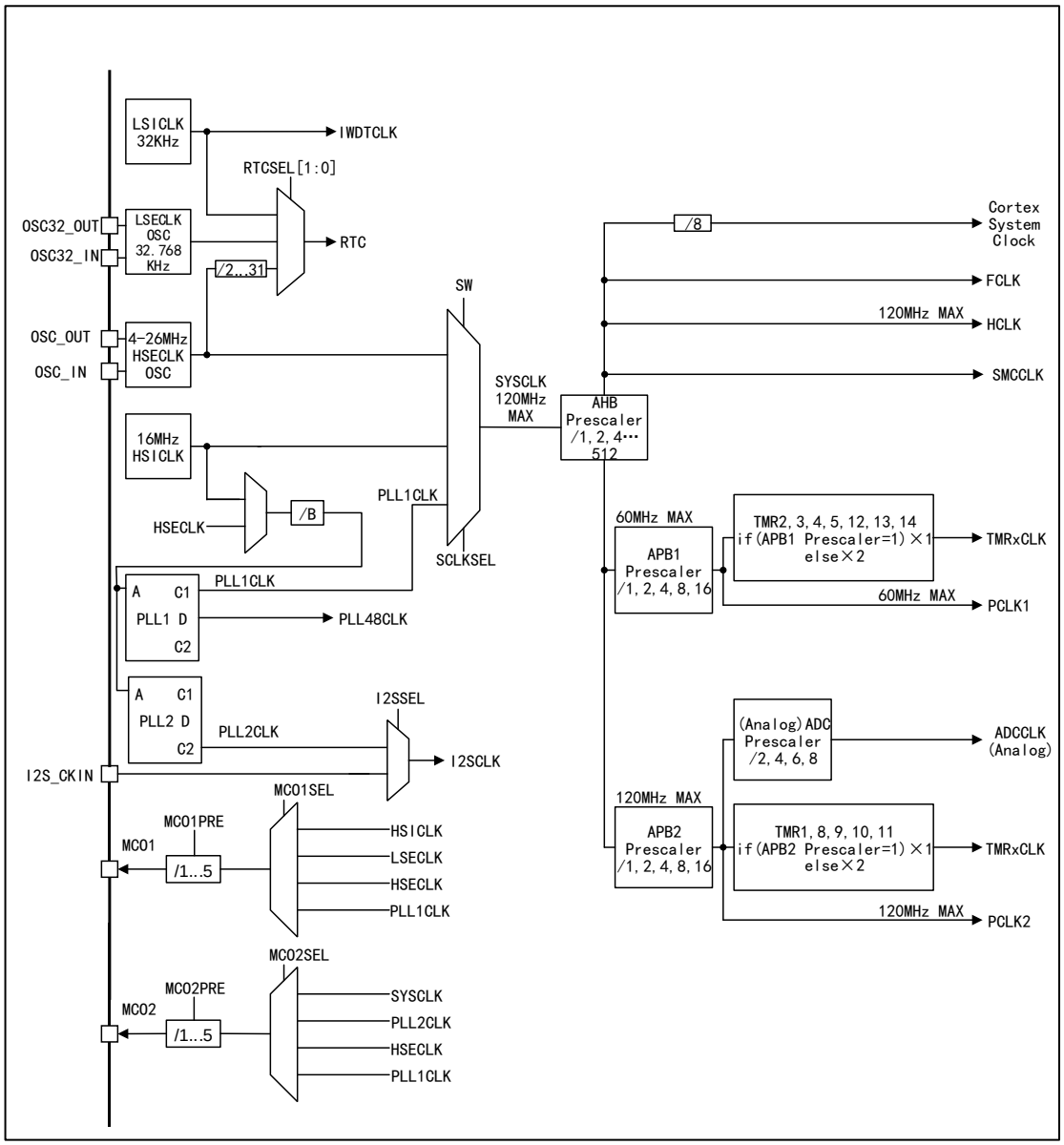
SMC can be configured to seamlessly connect with most graphic LCD controllers, supports the modes of Intel 8080 and Motorola 6800, and can flexibly connect with specific LCD interface. This LCD parallel interface can be used to easily build a simple graphics application environment or the high-performance scheme of the special acceleration controller can be used.

4.5 Clock

4.5.1 Clock tree

Clock tree of APM32F411xCxE is shown in the figure below:

Figure 6 APM32F411xCxE Clock Tree



4.5.2 Clock source

Clock source is divided into high-speed clock and low-speed clock according to the speed; the high-speed clock includes HSICLK and HSECLK, and the low-speed clock includes LSECLK and LSICLK; besides, some modules may have additional clock source pins to obtain the required clock frequency through external circuits.

4.5.3 System clock

HSICLK, PLL1CLK and HSECLK can be selected as system clock; the clock source of PLL1CLK can be HSICLK or HSECLK; the required system clock can be obtained by configuring PLL clock multiplier factor and frequency division factor.

When the product is reset and started, HSICLK is selected as the system clock by default, and then the user can choose one of the above clock sources as the system clock. When HSECLK failure is detected, the system will automatically switch back to the HSICLK, and if an interrupt

is enabled, the software can receive the related interrupt.

4.5.4 Bus clock

AHB, APB1 and APB2 buses are built in. The clock source of AHB is SYSCLK, and the clock source of APB1 and APB2 is HCLK; the required clock can be obtained by configuring the frequency division factor. The maximum frequency of AHB is 120MHz, that of APB2 is 120MHz, and that of APB1 is 60MHz.

4.5.5 Phase-locked loop

APM32F411xCxE series product has two PLL, one is main PLL (PLL1), and the other is PLL (PLL2) specially used to provide specific clock frequency for I2S. Both of them need to generate different clock frequencies by configuring parameters. Please refer to the *User Manual* for specific parameters and configuration registers.

4.6 Power supply and power supply management

4.6.1 Power supply scheme

Table 12 Power Supply Scheme

Name	Voltage range	Description
V_{DD}	1.8～3.6V	Power I/O (see pin distribution diagram for specific IO) and internal voltage regulator through V_{DD} pin.
V_{DDA}/V_{SSA}	1.8～3.6V	Supply power to ADC, reset module, RC oscillator and PLL analog part; when ADC is used, V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} respectively.
V_{BAT}	1.8～3.6V	When V_{DD} is disabled, power RTC, external 32KHz oscillator and backup register through internal power switch.

4.6.2 Voltage regulator

Table 13 Voltage Regulator Operating Mode

Name	Description
Master mode (MR)	Used in run mode
Low-power mode (LPR)	Used in stop mode
Power-down mode	Used in standby mode; then the voltage regulator has high-impedance output, the core circuit is powered down, the power consumption of the voltage regulator is zero, and all data of registers and SRAM will be lost.

Note: The voltage regulator is always in working state after reset, and outputs with high impedance in power-down mode.

4.6.3 Power supply voltage detector

Power-on reset (POR), power-down reset (PDR) and brown-out reset circuits are integrated inside the product. These three circuits are always in working condition. When the power-down reset circuit monitors that the power supply voltage is lower than the specified threshold value ($V_{POR/PDR}$), even for the external reset circuit, the system will remain reset.

The product has a built-in programmable power supply voltage detector (PVD) that can monitor V_{DD} and compare it with V_{PVD} threshold. When V_{DD} is outside the V_{PVD} threshold range and an interrupt is enabled, the MCU can be set to a safe state through the interrupt service program.

4.7 Low-power mode

APM32F411xCxE supports sleep, stop and standby low-power modes, and they have differences in power, wake-up time and wake-up mode. The low-power mode can be selected according to the actual application requirements.

Table 14 Low-power Mode

Mode	Description
Sleep mode	The core stops working, all peripherals are working, and it can be awakened through interrupts/events
Stop mode	Under the condition that SRAM and register data is not lost, the lowest power can be achieved in stop mode; The clock of the internal 1.2V power supply module will stop, HSECLK crystal resonator, HSICLK and PLL will be disabled, and the voltage regulator can be configured in normal mode or low-power mode; Any external interrupt line can wake up MCU, and the external interrupt lines include one of the 16 external interrupt lines, PVD output, and RTC.
Standby mode	The power in this mode is the lowest; The internal voltage regulator is disabled, all 1.2V power supply modules are powered down, HSECLK crystal resonator, and HSICLK clocks are disabled, SRAM and register data disappears, RTC area and backup register contents remain, and the standby circuit still works; The external reset signal on NRST, IWDT reset, rising edge on WKUP pin or RTC event will wake up MCU to exit the standby mode.

4.8 DMA

2 built-in DMA, 16 data streams in total. Each data stream corresponds to 8 channels, but only 1 channel can be used for each data stream at the same time. The peripherals supporting DMA requests are ADC, SPI, USART, I2C, SDIO, and TMRx. Four levels of priority can be configured for DMA channel. Data transmission of "Memory → Memory, Memory → Peripheral, Peripheral → Memory" can be supported (memory includes Flash and SRAM).

4.9 GPIO

GPIO can be configured as general input, general output, multiplexing function and analog input and output. The general input can be configured as floating input, pull-up input and pull-down input; the general output can be configured as push-pull output and open-drain output; the multiplexing function can be used for digital peripherals; and the analog input and output can be used for analog peripherals and low-power mode; the enable and disable pull-up/pull-down resistor can be configured; the speeds of 2MHz, 10MHz, 50MHz and 100MHz can be

configured; the higher the speed is, the greater the power consumption and the noise are.

4.10 Communication peripherals

4.10.1 USART/UART

Up to 6 universal synchronous/asynchronous transmitter receivers are built in the chip. The USART1/6 interfaces can communicate at a rate of 12.5Mbit/s, the USART2 interface can communicate at a rate of 6.25Mbit/s, while other USART/UART interfaces can communicate at a rate of 5.25Mbit/s. All USART/UART interfaces can configure baud rate, parity check bit, stop bit, and data bit length, and they all can support DMA. USART/UART function differences are shown in the table below:

Table 15 USART/UART Function Differences

USART mode/function	USART1	USART2	USART3	UART4	UART5	USART6
Hardware flow control of modem	√	√	√	—	—	√
Smart card mode	√	√	√	—	—	√
IrDA SIR coder-encoder functions	√	√	√	√	√	√
LIN mode	√	√	√	√	√	√
Standard characteristics	√	√	√	√	√	√
SPI host	√	√	√	—	—	√
Maximum baud rate under 16-time oversampling (Mbit/s)	6.25	3.12	2.62	2.62	2.62	6.25
Maximum baud rate under 8-time oversampling (Mbit/s)	12.5	6.25	5.25	5.25	5.25	12.5
APB mapping	APB2	APB1	APB1	APB1	APB1	APB2

Note: √ = support.

4.10.2 I2C

I2C1/2/3 bus interfaces are built-in and they all can work in multiple-master or slave modes, support 7-bit or 10-bit addressing, and support dual-slave addressing in 7-bit slave mode; the communication rate supports standard mode (up to 100kbit/s), fast mode (up to 400kbit/s) and fast mode plus (1Mbit/s); hardware CRC generator/checkers are built in; they can operate with DMA and support SMBus 2.0 version/PMBus.

4.10.3 SPI/I2S

5 SPI interfaces are built-in, support full duplex and half duplex communication in master mode and slave mode, can use DMA controller, and can configure 8 bits or 16 bits per frame. The maximum communication rate of SPI1/4/5 is 50Mbit/s, and that of SPI2/3 is 25Mbit/s. The hardware CRC generation/check supports basic SD card and MMC mode.

All SPI interfaces support DMA operation.

5 I2S are built in (multiplexed with SPI1/2/3/4/5), support half-duplex communication in master mode and slave mode, support synchronous transmission, and can be configured with 16-bit, 24-bit and 32-bit data transmission with 16-bit or 32-bit resolution. The configurable range of audio sampling rate is 8kHz~192kHz; when one or two I2S interfaces are configured as the master mode, the master clock can be output to external DAC or decoder (CODEC) at 256 times the sampling frequency.

4.10.4 QSPI

1 QSPI special communication interface is embedded, which supports DMA operation and can connect external flash through single-line, double-line or four-line SPI mode, and supports 8-bit, 16-bit and 32-bit access. There are 8-byte transmit FIFO and 8-byte receive FIFO inside.

4.10.5 CAN

2 built-in CAN, compatible with 2.0A and 2.0B (active) specification, and able to communicate at a rate of up to 1Mbit/s. It can receive and transmit standard frame of 11-bit identifier and extended frame of 29-bit identifier. It has 3 sending mailboxes, 2 receiving FIFO with three depth levels and 28 adjustable filters.

4.10.6 USB_OTG

One USB_OTG_FS controller is built in the product. It supports both host and slave functions and complies with the On-The-Go supplementary standard of USB 2.0 specification. It can also be configured as "Host only" or "Slave only" mode, and fully complies with USB 2.0 specification. OTG_FS clock (48MHz) is output by specific PLL.

4.10.7 SDIO

The secure digital input/output interface can connect SD card, SD I/O card, multi-media card (MMC), eMMC and CE-ATA card master interfaces, and provide data transmission between AHB system bus and SD memory card, SD I/O card, MMC and CE-ATA device.

4.11 ADC

2 built-in ADC with 12-bit accuracy, up to 16 external channels and 3 internal channels for each ADC. The internal channels measure the temperature sensor voltage, reference voltage and backup voltage respectively. A/D conversion mode for each channel includes single, continuous, scan or intermittent modes, and ADC conversion results can be left aligned or right aligned and stored in 16-bit data register. It supports analog watchdog and DMA.

4.11.1 Temperature sensor

1 temperature sensor (TSensor) is built in, which is internally connected with ADC_IN18 channel. The voltage generated by the sensor changes linearly with temperature, and the converted voltage value can be obtained by ADC and converted into temperature.

Table 16 Calibration Value of T_{sensor}

Calibration Value Name	Description	Memory Address
V_{sensor_CAL1}	At 30℃, Original data collected when V_{DDA}=3.3V	0x1FFF 7A2C - 0x1FFF 7A2D
V_{sensor_CAL2}	At 110℃, Original data collected when V_{DDA}=3.3V	0x1FFF 7A2E - 0x1FFF 7A2F

4.11.2 V_{BAT} detector

Built-in V_{BAT} detector, internally connected to ADC_IN18 channel. When temperature sensor and V_{BAT} conversion are set at the same time, only V_{BAT} conversion will be executed.

4.11.3 Internal reference voltage

Built-in reference voltage V_{REFINT}, internally connected to ADC_IN17 channel; V_{REFINT} can be obtained through ADC; V_{REFINT} provides stable voltage output for ADC and comparator.

Table 17 Internal Reference Voltage Calibration Value

Calibration Value Name	Description	Memory Address
V_{REFINT_CAL}	At 25℃(±5℃), Original data collected when V_{DDA}=3.3V (±10mV)	0x1FFF 7A2A - 0x1FFF 7A2B

4.12 Comparator

With 2 built-in fast rail-to-rail comparators; the internal/external reference voltage, hysteresis, and speed are programmable, and the output polarity is configurable. The reference voltage can be internal reference voltage (V_{REFINT}), and 1/4 or 1/2 or 3/4 of the internal reference voltage, which can generate interrupts, and support MCU entering sleep and stop modes by external interrupt.

4.13 Timer

2 built-in 16-bit advanced timers (TMR1/8), 6 16-bit general-purpose timers (TMR9/10/11/12/13/14), 2 32-bit general-purpose timers (TMR2/5), 1 independent watchdog timer, 1 window watchdog timer and 1 system tick timer.

Watchdog timer can be used to detect whether the program is running normally.

The system tick timer is the peripheral of the core with automatic reloading function. When the counter is 0, it can generate a maskable system interrupt, which can be used for real-time operating system and general delay.

Table 18 Function Comparison between Advanced/General-purpose and System Tick Timers

Timer type	System tick timer	General-purpose timer				Advanced timer
Timer name	Sys Tick Timer	TMR2/5	TMR3/4	TMR9/12	TMR10/11/13/14	TMR1/8
Counter resolution	24 bits	32 bits	16 bits			16 bits

Timer type	System tick timer	General-purpose timer			Advanced timer
Counter type	Down	Up, down, up/down	UP		Up, down, up/down
Prescaler factor	-	Any integer between 1 and 65536			Any integer between 1 and 65536
Generate DMA request	-	Can	No		Can
Capture/compare register	-	4	2	1	4
Complementary output	-	None			Yes
Pin characteristics	-	1-way external trigger signal input pin; 4-way non-complementary channel pin.	2-way non-complementary channel pin	1-way non-complementary channel pin	1-way external trigger signal input pin; 1-way braking input signal pin; 3-pair complementary channel pins; 1-way non-complementary channel pin.
Function Description	Special for real-time operating system. Automatic reloading function supported. When the counter is 0, it can generate a maskable system interrupt. Programmable clock source.	Synchronization or event chaining function is provided. The counter in debug mode can be frozen. Can be used to generate PWM output. Each timer has an independent DMA request mechanism. (Applicable only to TMR2/3/4/5) It can handle incremental encoder signals.			It has complementary PWM output with dead band insertion. When configured as a 16-bit standard timer, it has the same function as the TMRx timer. When configured as a 16-bit PWM generator, it has full modulation capability (0~100%). In debug mode, timers can be frozen, and PWM output is disabled. Synchronization or event chaining function is provided.

Table 19 Function Comparison between IWDT and WWDT

Name	Counter resolution	Counter type	Prescaler factor	Functional Description
Hardware watchdog	12 bits	Down	Any integer between 1 and 256	The clock is provided by an internally independent RC oscillator of 32KHz, which is independent of the master clock, so it can run in stop and standby modes. The whole system can be reset in case of problems. It can provide timeout management for applications as a free-running timer. It can be configured as a software or hardware startup watchdog through option bytes. The counter in debug mode can be frozen.
Window watchdog	7 bits	Down	-	Can be set for free running. The whole system can be reset in case of problems. Driven by the master clock, it has early warning interrupt function; The counter in debug mode can be frozen.

4.14 RTC

1 RTC is built in, and there are LSECLK signal input pins (OSC32_IN、OSC32_OUT), HSECLK signal input pins (OSC_IN and OSC_OUT) and 1 TAMP input signal detection pin (RTC_TAMP1); the clock source can be 32.768kHz external crystal oscillator, resonator or oscillator, LSICLK and HSECLK/128; it is powered by V_{DD} by default; when V_{DD} is powered off, it can be automatically switched to V_{BAT} power supply, and RTC configuration and time data will not be lost; RTC configuration and time data will not be lost in case of system reset, software reset and power-on reset; it supports clock and calendar functions.

4.14.1 Backup domain

20 backup registers are built in, are powered by V_{DD} by default; when V_{DD} is powered off, it can be automatically switched to V_{BAT} power supply, and the data in backup register will not be lost; the data in backup register will not be lost in case of system reset, software reset and power-on reset.

4.15 RNG

A RNG is embedded, and it provides 32-bit random number generated by the integrated simulation.

4.16 CRC

1 CRC (cyclic redundancy check) computing unit is built in, which can generate CRC codes and operate 8-bit, 16-bit and 32-bit data.

5 Electrical Characteristics

5.1 Test conditions of electrical characteristics

5.1.1 Maximum and minimum values

Unless otherwise specified, all products are tested on the production line at T_A=25℃. Its maximum and minimum values can support the worst environmental temperature, power supply voltage and clock frequency.

In the notes at the bottom of each table, it is stated that the data is obtained through comprehensive evaluation, design simulation or process characteristics and is not tested on the production line; on the basis of comprehensive evaluation, after passing the sample test, take the average value and add and subtract three times the standard deviation (average ±3∑) to get the maximum and minimum values.

5.1.2 Typical value

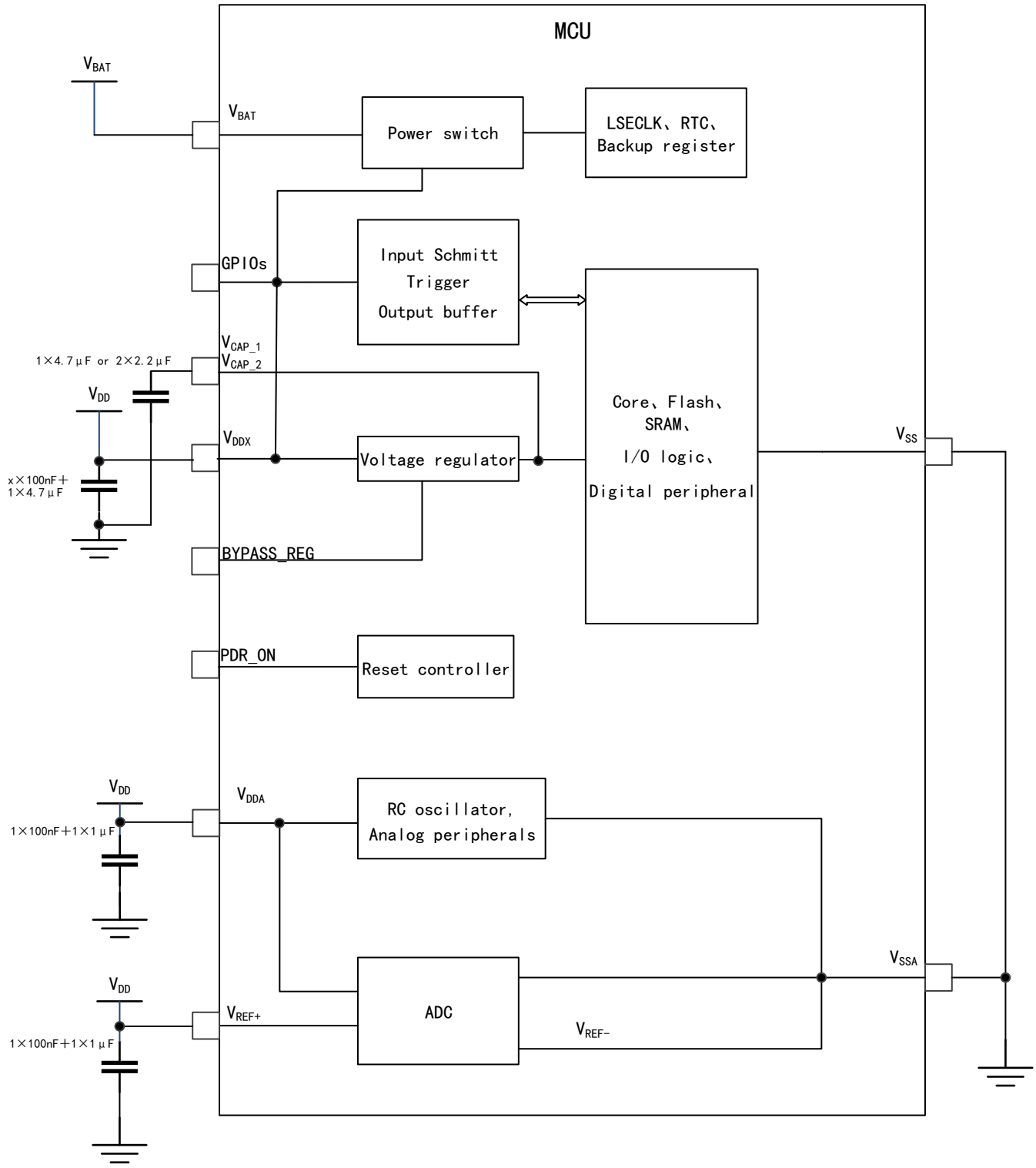
Unless otherwise specified, typical data is measured based on T_A=25℃, V_{DD}=V_{DDA}=3.3V . The data is only used for design guidance.

5.1.3 Typical curve

Unless otherwise specified, typical curves can only be used for design guidance and are not tested.

5.1.4 Power supply scheme

Figure 7 Power Supply Scheme



Notes:

（1） V_{DDx} in the figure means that the number of V_{DD} is x.

（2） 4.7uF is only applicable when using a VCAP.

5.1.5 Load capacitance

Figure 8 Load conditions when measuring pin parameters

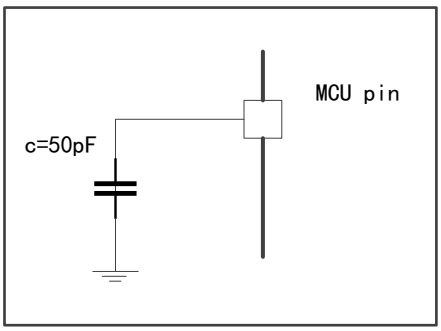


Figure 9 Pin Input Voltage Measurement Scheme

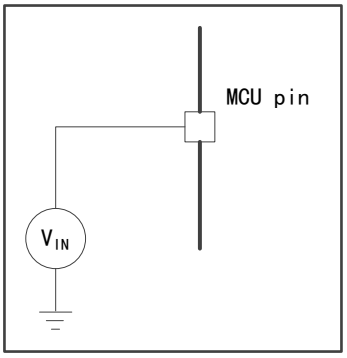
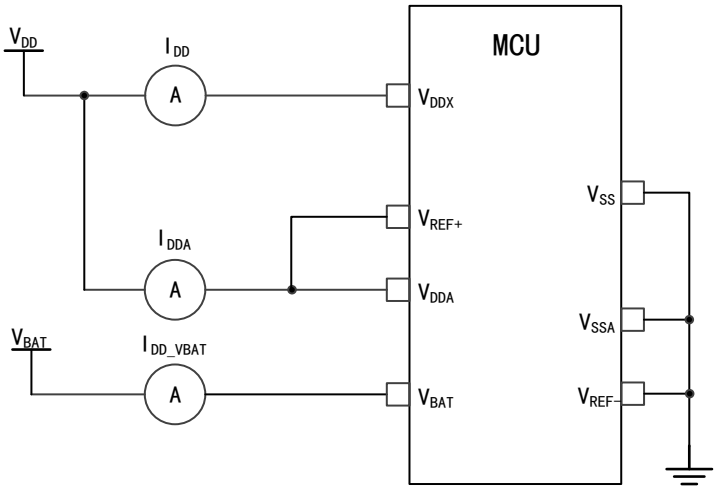


Figure 10 Power Consumption Measurement Scheme



5.2 Test under general operating conditions

Table 20 General Operating Conditions

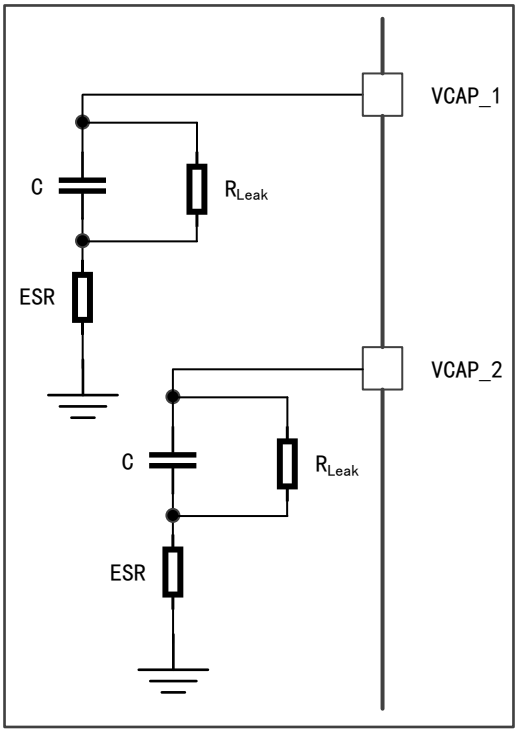
Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f_{HCLK}	Internal AHB clock frequency	-	-	-	120	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	-	-	60	

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f_{PCLK2}	Internal APB2 clock frequency	-	-	-	120	
V_{DD}	Main power supply voltage	-	1.8	-	3.6	V
V_{DDA}	Analog power supply voltage (When ADC is not used)	It must be the same as V_{DD}	1.8	-	2.4	V
	Analog power supply voltage (When ADC is used)		2.4	-	3.6	
V_{BAT}	Power supply voltage of backup domain	-	1.8	-	3.6	V
V_{12}	Using a voltage regulator, 1.2V internal voltage on VCAP_ 1/VCAP_2 pins	VOSSEL[1:0]=01 Max frequency	1.08	1.14	1.20	V
		VOSSEL[1:0]=10 Max frequency	1.20	1.26	1.32	
		VOSSEL[1:0]=11 Max frequency	1.26	1.32	1.38	
T_A	Ambient temperature (temperature number 6)	Maximum power dissipation	-40	-	85	℃

5.3 External capacitors

By connecting the external capacitor C_{EXT} to VCAP_1 and VCAP_2 pins to achieve stability of the main voltage regulator. For cases where only one VCAP pin is supported, a single capacitor can be used instead of two external capacitors C_{EXT}. Among them, ESR is the equivalent series resistance.

Figure 11 External capacitors C_{EXT}



5.3.1 VCAP_1/VCAP_2 Operating conditions

The capacitance C_{EXT} of an external capacitor using a single VCAP pin is 4.7uF. The ESR of an external capacitor using a single VCAP pin is less than 1 Ω. If bypassing the voltage regulator, two 100nF decoupling capacitors can be used instead of two 2.2 μF VCAP capacitors.

5.4 Absolute maximum rated value

If the load on the device exceeds the absolute maximum rated value, it may cause permanent damage to the device. Here, only the maximum load that can be borne is given, and there is no guarantee that the device functions normally under this condition.

5.4.1 Maximum temperature characteristics

Table21 Temperature Characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	-65 ~ +150	℃
T_J	Maximum junction temperature	130	℃

5.4.2 Maximum rated voltage characteristics

All power supply (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the power supply within the external limited range.

Table 22 Maximum Rated Voltage Characteristics

Symbol	Description	Minimum value	Maximum value	Unit
V_{DD} - V_{SS}	External main power supply voltage	-0.3	4.0	V
V_{IN}	Input voltage on FT pins and 3.3V standard I/O	V_{SS}-0.3	V_{DD}+4	
	Input voltage on other pins	V_{SS}-0.3	4.0	
	Input voltage on Boot0	V_{SS}	9.0	
$\lvert \Delta V_{DDx} \rvert$	Voltage difference between different power supply pins	-	50	mV
$\lvert V_{SSx}-V_{SS} \rvert$	Voltage difference between different grounding pins	-	50	

5.4.3 Maximum rated current characteristics

Table 23 Current Characteristics

Symbol	Description	Maximum value	Unit
I_{VDD}	Maximum current through V_{DD}/V_{DDA} power line (supply current) (1)	100	mA
I_{VSS}	Maximum current through V_{SS} ground line (outflow current) (1)	-100	
ΣI_{VDD}	Total current through V_{DD}/V_{DDA} power line (supply current) (1)	160	
ΣI_{VSS}	Total current through V_{SS} ground line (outflow current) (1)	-160	
I_{IO}	Sink current on any I/O and control pin	25	
	Source current on any I/O and control pin	-25	
ΣI_{IO}	Total Sink current on any I/O and control pin	120	
	Total Source current on any I/O and control pin	-120	
$I_{INJ(PIN)}$ (2)	Injection current of 5T pin	-5/+0	
	Injection current of other pins		
$\Sigma I_{INJ(PIN)}$(2)	Total injection current on all I/O and control pins (4)	±25	

Note:

(1) All power supply (VDD, V_{DDA}) and ground (V_{SS}, V_{SSA}) must always be within the allowed range.

(2) The outflow current will interfere with the analog performance of the device.

(3) I/O cannot be injected positively: when $V_{IN}<V_{SS}$, $I_{INJ(PIN)}$ cannot exceed the maximum allowable input voltage value.

(4) Correct distribution of current consumption across all arbitrary I/O and control pins.

(5) When the current is injected into several I/O ports at the same time, the maximum value of ΣIINJ(PIN) is the sum of instantaneous absolute value of inflow current and outflow current.

5.4.4 Electrostatic discharge (ESD)

Table 24 ESD Absolute Maximum Ratings

Symbol	Parameter	Condition	Range	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	TA=+25 ℃, conforming to ANSI/ESDA/JEDEC JS-001-2017	±4000	V

Symbol	Parameter	Condition	Range	Unit
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging device model)	TA=+25 ℃, conforming to ANSI/ESDA/JEDEC JS-002-2018	500	

Note: The samples are measured by a third-party testing organization and are not tested in production.

5.4.5 Static latch-up (LU)

Table 25 Static Latch-up

Symbol	Parameter	Condition	Type
LU	Class of static latch-up	T A=+105℃, conforming to JEDEC JESD78F-2022	Class II A

Note: The samples are measured by a third-party testing organization and are not tested in production.

5.5 On-chip memory

5.5.1 Flash characteristics

Table 26 Flash Memory Characteristics

Symbol	Parameter		Condition	Minimum value	Typical value	Maximum value	Unit
t_{prog}	8/16/32-bit programming time		T_A = -40~85℃ V_{DD}=1.8~3.6V	70	77.7	85	μs
t_{ERASE1}	Page (16KB) erase time	8 bits	T_A = -40~85℃ V_{DD}=1.8~3.6V	55	58.7	65	ms
		16 bits		55	58.7	65	
		32 bits		55	58.7	65	
t_{ERASE2}	Page (64KB) erase time	8 bits		220	234.9	25	
		16 bits		220	234.9	250	
		32 bits		220	234.8	250	
t_{ERASE3}	Page (128KB) erase time	8 bits		450	469.7	500	
		16 bits		450	469.7	500	
		32 bits		450	469.7	500	
t_{ME}	Mass erase time	8 bits	T_A = -40~85℃ V_{DD}=1.8~3.6V	-	9.1	10	ms
		16 bits		-	9.1	10	
		32 bits		-	9.1	10	
V_{prog}	Voltage of 8-bit programming		T_A = -40~85℃	1.8	-	3.6	V
	Voltage of 16-bit programming			2.1	-	3.6	
	Voltage of 32-bit programming			2.7	-	3.6	
t_{RET}	Data saving time		T_A=125℃	10.77	-	-	years
N_{RW}	Erase cycle		T_A=85°C	100K	-	-	cycles

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.6 Clock

5.6.1 Characteristics of external clock source

5.6.1.1 High-speed external clock generated by crystal resonator

For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer.

Table 27 HSECLK4~26MHz Oscillator Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f_{OSC_IN}	Oscillator frequency	-	4	-	26	MHz
R_F	Feedback resistance	-	-	200	-	kΩ
$I_{DD(HSECLK)}$	HSECLK current consumption	V_{DD}=3.3V, C_L=10pF@8MHz	-	-	0.5	mA
$t_{SU(HSECLK)}$	Start Time	V_{DD} is stable	-	2	-	ms

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.6.1.2 Low-speed external clock generated by crystal resonator

For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer.

Table 28 LSECLK Oscillator Characteristics (f_{LSECLK} =32.768KHz)

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f_{OSC_IN}	Oscillator frequency	-	-	32.768	-	KHz
$I_{DD(LSECLK)}$	LSECLK current consumption	-	-	-	1	μA
$t_{SU(LSECLK)}$(1)	Start Time	V_{DD} is stable	-	2	-	s

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

(1) $t_{SU(LSEC\ LK)}$ is the startup time, which is measured from the time when LSECLK is enabled by software to the time when stable oscillation at 32.768KHz is obtained. This value is measured by using a standard crystal resonator, which may vary widely with crystal manufacturer.

5.6.2 Characteristics of internal clock source

5.6.2.1 High-speed internal (HSICLK) RC oscillator

Table 29 HSICLK Oscillator Characteristics

Symbol	Parameter	Condition		Minimum value	Typical value	Maximum value	Unit
f_{HSICLK}	Frequency	-		-	16	-	MHz
$A_{CC(HSICLK)}$	Accuracy of HSICLK oscillator	Factory calibration	V_{DD}=2-3.6V, T_A=-40~85℃	-2	-	2.5	%
$I_{DDA(HSICLK)}$	Power consumption of HSICLK oscillator	-		-	60	80	μA
$t_{SU(HSICLK)}$	Startup time of HSICLK oscillator	V_{DD}=3.3V, T_A=-40~85℃		-	2.2	4	μs

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.6.2.2 Low-speed internal (LSICLK) RC oscillator

Table 30 LSICLK Oscillator Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f_{LSICLK}	Frequency	V_{DD} =1.8-3.6V, T_A=-40~85℃	17	32	47	KHz
$I_{DD(LSICLK)}$	Power consumption of LSICLK oscillator	-	-	0.4	0.6	μA
$t_{SU(LSICLK)}$	Startup time of LSICLK oscillator	V_{DD}=1.8-3.6V, T_A=-40~85℃	-	15	40	μs

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.6.3 PLL characteristics

Table 31 PLL1 Characteristics

Symbol	Parameter	Condition	Value			Unit
			Minimum value	Typical value	Maximum value	
f_{PLL1_IN}	PLL1 input clock	V_{DD}=1.8-3.6V, T_A=-40~85℃	0.95	1	2.1	MHz
	PLL1 input clock duty cycle	-	45	-	55	%
f_{PLL1_OUT}	PLL1 frequency multiplier output clock	V_{DD}=3.3V, T_A=-40~85℃	10	-	120	MHz
Jitter	period jitter	System clock 10M~120MHz	-	±200	-	ps
t_{LOCK1}	PLL1 phase locking time	-	30	-	200	μs

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

Table 32 PLL2 Characteristics

Symbol	Parameter	Condition	Value			Unit
			Minimum value	Typical value	Maximum value	
f_{PLL2_IN}	PLL2 input clock	V_{DD}=1.8-3.6V，T_A=-40~85℃	0.95	1	2.1	MHz
	PLL2 input clock duty cycle	-	45	-	60	%
f_{PLL2_OUT}	PLL2 frequency multiplier output clock	V_{DD}=1.8-3.6V，T_A=-40~85℃	20	-	120	MHz
Jitter	period jitter	System clock 10M~120MHz	-	±200	-	ps
t_{LOCK1}	PLL phase locking time	-	75	-	200	μs

5.7 Power supply and power supply management

5.7.1 Test of Embedded Reset and Power Control Module Characteristics

Table 33 Embedded Reset and Power Control Block Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
$V_{POR/PDR}$	Power-on/power-down reset threshold	Falling edge	1.66	1.68	1.72	V
		Rising edge	1.71	1.72	1.76	V
V_{BOR1}	Under-voltage threshold level 1	Falling edge	2.19	2.22	2.27	V
		Rising edge	2.29	2.31	2.32	V
V_{BOR2}	Under-voltage threshold level 2	Falling edge	2.49	2.53	2.59	V
		Rising edge	2.58	2.60	2.61	V
V_{BOR3}	Under-voltage threshold level 3	Falling edge	2.82	2.86	2.92	V
		Rising edge	2.91	2.93	2.96	V
$V_{BORhyst}$	BOR hysteresis	-	-	100	-	mV
$V_{PDRhyst}$	PDR hysteresis	-	-	40	-	mV
$T_{RSTTEMPO}$	Reset duration	-	1.2	-	9	ms

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

Table 34 Programmable Power Supply Voltage Detector Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{PVD}	Programmable power supply voltage detector voltage level selection	PLS[2:0]=000 (rising edge)	2.09	-	2.21	V
		PLS[2:0]=000 (falling edge)	1.98	-	2.11	V
		PLS[2:0]=000 (PVD hysteresis)	100	-	110	mV
		PLS[2:0]=001 (rising edge)	2.23	-	2.39	V

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
		PLS[2:0]=001 (falling edge)	2.13	-	2.28	V
		PLS[2:0]=001 (PVD hysteresis)	100	-	120	mV
		PLS[2:0]=010 (rising edge)	2.39	-	2.52	V
		PLS[2:0]=010 (falling edge)	2.29	-	2.41	V
		PLS[2:0]=010 (PVD hysteresis)	100	-	120	mV
		PLS[2:0]=011 (rising edge)	2.54	-	2.59	V
		PLS[2:0]=011 (falling edge)	2.44	-	2.58	V
		PLS[2:0]=011 (PVD hysteresis)	90	-	100	mV
		PLS[2:0]=100 (rising edge)	2.70	-	2.85	V
		PLS[2:0]=100 (falling edge)	2.59	-	2.74	V
		PLS[2:0]=100 (PVD hysteresis)	110	-	120	mV
		PLS[2:0]=101 (rising edge)	2.86	-	3.01	V
		PLS[2:0]=101 (falling edge)	2.65	-	2.92	V
		PLS[2:0]=101 (PVD hysteresis)	90	-	110	mV
		PLS[2:0]=110 (rising edge)	2.96	-	3.12	V
		PLS[2:0]=110 (falling edge)	2.85	-	3.00	V
		PLS[2:0]=110 (PVD hysteresis)	110	-	120	mV
		PLS[2:0]=111 (rising edge)	3.07	-	3.21	V
		PLS[2:0]=111 (falling edge)	2.95	-	3.09	V
		PLS[2:0]=111 (PVD hysteresis)	110	-	130	mV

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.8 Power

5.8.1 Power consumption test environment

(1) The values are measured by executing Dhrystone 2.1, with the Keil.V5 compilation environment and the L0 compilation optimization level.

(2) All I/O pins are in analog input mode and are connected to a static level at V_{DD} or V_{SS} (no load)

(3) Unless otherwise specified, all peripherals are disabled

(4) The relationship between Flash wait cycle setting and f_{HCLK}:

- 0~30MHz: 0 wait cycle
- 30~60MHz: 1 wait cycle
- 60~90MHz: 2 wait cycles
- 90~120MHz: 3 wait cycles

(5) When the peripherals are enabled: $f_{PCLK1}=f_{HCLK}/4$, $f_{PCLK2}=f_{HCLK}/2$

5.8.2 Power consumption in operation mode

Table 35 Power in Run Mode when the Program is Executed in Flash (ART is enabled)

Parameter	Condition	f_{HCLK}	Typical value (1) (T_A=25℃)				Maximum value (1) (T_A=85℃)			
			V_{DD}=1.8V		V_{DD}=3.6V		V_{DD}=1.8V		V_{DD}=3.6V	
			I_{DDA} (μA)	I_{DD} (mA)	I_{DDA} (μA)	I_{DD} (mA)	I_{DDA} (μA)	I_{DD} (mA)	I_{DDA} (μA)	I_{DD} (mA)
Power consumption in operation mode	HSECLK bypass, PLL enable, disabling HSICLK, enabling all peripherals (2)	120MHz	573.47	32.39	597.82	32.36	616.28	33.74	646.85	34.47
		100MHz	526.17	26.68	532.69	26.91	583.02	28.44	589.86	28.56
		84MHz	693.94	22.49	700.11	23.18	745.43	24.26	752.26	24.35
		64MHz	593.41	15.59	599.35	15.99	646.22	16.61	653.51	16.98
		50MHz	526.22	12.30	532.48	12.70	584.69	13.05	589.71	13.84
		20MHz	479.82	5.76	486.34	6.19	539.42	6.65	545.95	6.98
	HSECLK bypass, PLL enable, disabling HSICLK, disabling all peripherals (2)	120MHz	574.10	19.95	580.15	19.58	629.81	20.45	634.52	22.25
		100MHz	526.14	14.70	532.42	14.93	583.93	15.94	590.01	16.28
		84MHz	693.58	12.47	699.77	13.00	745.12	14.27	751.66	14.17
		64MHz	593.03	8.64	599.47	8.98	645.61	9.45	653.36	9.88
		50MHz	525.91	6.83	532.02	7.26	583.32	7.56	589.55	8.08
		20MHz	479.91	3.31	485.87	3.73	539.27	4.12	545.34	4.51
	HSICLK, PLL off, enabling all peripherals (2)	16MHz	107.58	4.45	117.57	4.58	121.66	5.49	132.31	5.47
		1MHz	107.79	3.62	117.57	3.74	121.80	4.67	132.79	4.75
	HSICLK, PLL off, disabling all peripherals (2)	16MHz	107.84	2.35	117.46	2.36	122.71	3.21	132.66	3.27
		1MHz	107.74	2.31	117.27	2.32	121.97	3.19	132.61	3.25

Notes:

(1) The data is obtained from a comprehensive evaluation and is not tested in production.

(2) When the analog peripherals such as ADC, HSECLK, LSECLK, HSICLK and LSICLK are enabled, extra power consumption needs to be considered.

Table 36 Power in Run Mode when the Program is Executed in Flash (ART is disabled)

Parameter	Condition	f_{HCLK}	Typical value (1) (T_A=25℃)				Maximum value (1) (T_A=85℃)			
			V_{DD}=1.8V		V_{DD}=3.6V		V_{DD}=1.8V		V_{DD}=3.6V	
			I_{DDA} (μA)	I_{DD} (mA)	I_{DDA} (μA)	I_{DD} (mA)	I_{DDA} (μA)	I_{DD} (mA)	I_{DDA} (μA)	I_{DD} (mA)
Power consumption	HSECLK 8M multiplier, PLL	120MHz	574.10	29.32	579.91	29.96	6.28.60	31.09	635.59	31.70
		100MHz	526.87	24.75	532.63	25.39	582.57	26.30	589.86	27.16

Parameter	Condition	f_{HCLK}	Typical value (1) (T_A=25℃)				Maximum value (1) (T_A=85℃)			
			V_{DD}=1.8V		V_{DD}=3.6V		V_{DD}=1.8V		V_{DD}=3.6V	
			I_{DDA} (μA)	I_{DD} (mA)	I_{DDA} (μA)	I_{DD} (mA)	I_{DDA} (μA)	I_{DD} (mA)	I_{DDA} (μA)	I_{DD} (mA)
in operation mode	enable, disabling HSICLK, enabling all peripherals (2)	84MHz	693.79	21.23	699.70	21.73	745.58	22.52	752.26	23.10
		64MHz	593.55	14.95	599.17	15.40	656.83	16.03	653.51	16.49
		50MHz	526.19	11.81	532.60	12.27	582.11	12.71	589.86	13.32
		20MHz	480.20	5.5421	486.28	6.00	540.03	6.40	546.26	6.83
	HSECLK 8M multiplier, PLL enable, disabling HSICLK, disabling all peripherals (2)	120MHz	574.25	15.09	580.03	15.69	629.05	16.49	634.98	17.04
		100MHz	526.49	12.85	532.73	13.48	583.63	14.09	589.71	14.73
		84MHz	693.89	11.02	699.86	11.59	744.97	12.18	751.05	13.00
		64MHz	592.99	7.94	599.08	8.45	647.28	8.76	653.21	9.35
		50MHz	526.16	6.35	532.19	6.80	583.17	7.18	589.55	7.78
		20MHz	480.05	3.11	486.22	3.54	540.48	3.93	547.32	4.31
	HSICLK, PLL off, enabling all peripherals (2)	16MHz	107.34	4.83	117.53	4.99	122.26	6.18	132.46	6.31
		1MHz	107.77	4.01	117.55	4.16	121.91	5.31	132.11	5.50
	HSICLK, PLL off, disabling all peripherals (2)	16MHz	107.42	2.67	117.62	2.89	121.86	3.85	133.56	3.97
		1MHz	107.78	2.66	117.61	2.87	122.41	3.86	132.66	3.93

Notes:

(1) The data is obtained from a comprehensive evaluation and is not tested in production.

(2) When the analog peripherals such as ADC, HSECLK, LSECLK, HSICLK and LSICLK are enabled, extra power consumption needs to be considered.

Table 37 Power in Run Mode when the Program is Executed in SRAM (ART is disabled)

Parameter	Condition	f_{HCLK}	Typical value (1) (T_A=25℃)				Maximum value (1) (T_A=85℃)			
			V_{DD}=1.8V		V_{DD}=3.6V		V_{DD}=1.8V		V_{DD}=3.6V	
			I_{DDA} (μA)	I_{DD} (mA)	I_{DDA} (μA)	I_{DD} (mA)	I_{DDA} (μA)	I_{DD} (mA)	I_{DDA} (μA)	I_{DD} (mA)
Power consumption in operation mode	HSECLK 8M multiplier, PLL enable, disabling HSICLK, enabling all peripherals (2)	120MHz	574.70	33.63	580.07	33.90	628.29	36.51	634.83	36.39
		100MHz	526.51	27.95	532.54	28.39	581.96	29.69	588.95	31.09
		84MHz	693.70	24.07	699.77	24.26	743.45	25.88	750.74	25.85
		64MHz	593.46	17.06	599.19	17.49	646.37	18.14	653.06	18.53
		50MHz	526.26	12.89	532.48	13.28	582.11	13.75	589.40	14.78
		20MHz	480.11	6.04	486.12	6.44	538.96	6.86	544.74	7.22
	HSECLK 8M multiplier, PLL	120MHz	574.24	19.44	580.15	19.65	627.23	21.70	634.52	22.31
		100MHz	526.17	16.11	532.75	16.48	582.72	17.47	588.95	18.65

Parameter	Condition	f_{HCLK}	Typical value (1) (T_A=25℃)				Maximum value (1) (T_A=85℃)			
			V_{DD}=1.8V		V_{DD}=3.6V		V_{DD}=1.8V		V_{DD}=3.6V	
			I_{DDA} (μA)	I_{DD} (mA)	I_{DDA} (μA)	I_{DD} (mA)	I_{DDA} (μA)	I_{DD} (mA)	I_{DDA} (μA)	I_{DD} (mA)
	enable, disabling HSICLK, disabling all peripherals (2)	84MHz	693.48	14.05	699.64	14.19	743.60	15.45	751.20	15.64
		64MHz	593.09	10.04	599.25	10.52	646.68	11.03	651.69	11.37
		50MHz	526.22	7.47	532.42	7.45	581.81	8.14	588.03	8.90
		20MHz	480.29	3.63	586.23	4.02	537.60	4.39	545.65	4.73
	HSICLK, PLL off, enabling all peripherals (2)	16MHz	107.91	4.63	117.67	4.71	121.25	5.42	132.20	5.52
		1MHz	107.80	3.80	117.30	3.87	121.72	4.56	131.88	4.66
	HSICLK, PLL off, disabling all peripherals (2)	16MHz	104.76	2.47	117.43	2.54	121.51	3.23	132.22	3.28
		1MHz	107.57	2.44	117.36	2.52	121.98	3.18	131.42	3.27

Notes:

(1) The data is obtained from a comprehensive evaluation and is not tested in production.

(2) When the analog peripherals such as ADC, HSECLK, LSECLK, HSICLK and LSICLK are enabled, extra power consumption needs to be considered.

5.8.3 Power consumption in sleep mode

Table 38 Power in Sleep Mode when the Program is Executed in Flash (ART is disabled)

Parameter	Condition	f_{HCLK}	Typical value (1) (T_A=25℃)				Maximum value (1) (T_A=85℃)			
			V_{DD}=1.8V		V_{DD}=3.6V		V_{DD}=1.8V		V_{DD}=3.6V	
			I_{DDA} (μA)	I_{DD} (mA)	I_{DDA} (μA)	I_{DD} (mA)	I_{DDA} (μA)	I_{DD} (mA)	I_{DDA} (μA)	I_{DD} (mA)
Power consumption in sleep mode	HSECLK 8M multiplier, PLL enable, disabling HSICLK, enabling all peripherals (2)	120MHz	574.27	22.65	580.16	23.03	629.36	24.17	635.28	24.54
		100MHz	526.40	18.96	532.86	19.35	583.32	20.36	588.49	20.76
		84MHz	693.76	16.25	699.67	16.64	744.82	17.50	751.35	17.83
		64MHz	593.11	11.33	599.44	11.69	646.83	12.31	653.21	12.62
		50MHz	526.14	8.95	531.85	9.31	583.17	9.88	588.79	10.18
		20MHz	479.27	4.27	486.03	4.60	538.51	5.09	545.95	5.37
	HSECLK 8M multiplier, PLL enable, disabling HSICLK, disabling all peripherals (2)	120MHz	573.47	7.65	585.70	8.01	616.28	8.75	646.85	9.05
		100MHz	521.50	6.46	552.07	6.81	585.70	7.53	616.28	7.83
		84MHz	686.60	5.65	711.06	6.00	738.57	6.62	769.15	6.92
		64MHz	585.70	4.01	610.16	4.35	646.85	4.79	677.42	5.06
		50MHz	521.50	3.24	545.96	3.57	585.70	3.99	616.28	4.30
		20MHz	472.58	1.72	493.98	2.06	524.56	2.47	555.13	2.74

Parameter	Condition	f_{HCLK}	Typical value (1) (T_A=25℃)				Maximum value (1) (T_A=85℃)			
			V_{DD}=1.8V		V_{DD}=3.6V		V_{DD}=1.8V		V_{DD}=3.6V	
			I_{DDA} (μA)	I_{DD} (mA)	I_{DDA} (μA)	I_{DD} (mA)	I_{DDA} (μA)	I_{DD} (mA)	I_{DDA} (μA)	I_{DD} (mA)
	HSICLK, PLL off, enabling all peripherals (2)	16MHz	107.86	3.35	117.34	3.37	121.62	4.13	132.41	4.15
		1MHz	107.81	2.52	117.37	2.54	121.49	3.27	133.59	3.32
	HSICLK, PLL off, disabling all peripherals (2)	16MHz	107.63	1.08	117.33	1.09	121.36	1.83	132.54	1.85
		1MHz	107.56	1.05	117.69	1.06	121.43	1.80	131.53	1.81

Notes:

(1) The data is obtained from a comprehensive evaluation and is not tested in production.

(2) When the analog peripherals such as ADC, HSECLK, LSECLK, HSICLK and LSICLK are enabled, extra power consumption needs to be considered.

5.8.4 Power consumption in stop mode

Table 39 Power in Stop Mode

Condition		Typical value (1)		Maximum value (1)	
		V_{DD}=3.6V，T_A=25℃		V_{DD}=3.6V，T_A=85℃	
		$I_{DDA(μA)}$	$I_{DD(μA)}$	$I_{DDA(μA)}$	$I_{DD(μA)}$
Flash is in stop mode, all oscillators are disabled, and no independent watchdog	Using the main voltage regulator	113.77	114.60	333.09	334.88
	Using a low-power regulator	21.91	22.14	195.73	197.03
Flash is in power-down mode, all oscillators are disabled, and no independent watchdog	Using the main voltage regulator	105.09	105.89	320.78	322.56
	Using a low-power regulator	13.41	13.60	184.89	186.27
	Using low-power and low-voltage regulators	10.04	10.23	150.98	152.15

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

5.8.5 Power consumption in standby mode

Table 40 Power in Standby Mode

Condition		Typical value (1)		Maximum value (1)	
		V_{DD}=3.6V，T_A=25℃		V_{DD}=3.6V，T_A=85℃	
		$I_{DDA(μA)}$	$I_{DD(μA)}$	$I_{DDA(μA)}$	$I_{DD(μA)}$
Power supply current in standby mode	The low-speed oscillator and RTC are enabled	2.07	2.22	3.74	3.94
	The low-speed oscillator and RTC are disabled	1.35	1.49	2.90	3.10

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

5.8.6 Peripheral power consumption

Peripheral power consumption = current that enables the peripheral clock-current that disables the peripheral clock.

Table 41 Power of Peripheral

Parameter	Peripheral Clock	Typical value (1) T_A=25℃, V_{DD}=3.3V	Unit
AHB1 (up to 120MHz)	DMA1	0.46	μA/MHz
	DMA2	0.49	
	GPIOA	0.27	
	GPIOB	0.24	
	GPIOC	0.27	
	GPIOD	0.21	
	GPIOE	0.20	
	GPIOH	0.08	
	CRC	0.06	
AHB2 (up to 120MHz)	OTG_FS	1.97	
	QSPI	2.92	
	RNG	0.34	
AHB3 (up to 120MHz)	SMC	0.55	
APB1 (up to 60MHz)	TMR2	0.41	
	TMR3	0.33	
	TMR4	0.37	
	TMR5	0.38	
	TMR12	0.21	
	TMR13	0.13	
	TMR14	0.14	
	WWDT	0.05	
	SPI2/I2S2	0.11	
	SPI3/I2S3	0.12	
	USART2	0.09	
	USART3	0.09	
	UART4	0.08	
	UART5	0.08	
	I2C1	0.10	
	I2C2	0.09	

Parameter	Peripheral Clock	Typical value (1) T_A=25℃, V_{DD}=3.3V	Unit
	I2C3	0.10	
	CAN1	0.14	
	CAN2	0.14	
	PMU	0.03	
APB2 (up to 120MHz)	SDIO	0.34	
	TMR1	0.74	
	TMR8	0.73	
	TMR9	0.32	
	TMR10	0.20	
	TMR11	0.21	
	ADC1	0.18	
	ADC2	0.24	
	SPI1/I2S1	0.12	
	SPI4/I2S4	0.11	
	SPI5/I2S5	0.11	
	USART1	0.19	
	USART6	0.20	
	SYSCFG	0.09	

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.8.7 Backup Domain Power Consumption

Table 42 V_{BAT} Power

Symbol	Parameter	Condition	Typical value (1), T_A=25℃			Maximum value (1)	Unit
			V_{BAT}=1.8V	V_{BAT}=2.4V	V_{BAT}=3.3V	V_{BAT}=3.6V, T_A=85℃	
I_{DD_VBAT}	LSECLK and RTC are enabled	The low-speed oscillator and RTC are enabled	0.948	1.076	1.365	2.130	μA
		The low-speed oscillator and RTC are disabled	0.004	0.008	0.037	0.533	

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

5.9 Wake-up time in low-power mode

The measurement of wake-up time in low-power mode is from the start of wake-up event to the time when the user program reads the first instruction, in which V_{DD}=V_{DDA}.

Table 43 Wake-up Time in Low-power Mode

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
$t_{WUSLEEP}$	Wake up from sleep mode	-	34	39.7	47.2	ns
t_{WUSTOP}	Wake up from the stop mode	The main voltage regulator is in run mode	13.1	13.7	14.8	μs
		The mainvoltage regulator is in low-power mode, and Flash is in deep power-down mode	104	106.0	108	
		The voltage regulator is in low-power mode	15.4	18.8	23.6	
		The voltage regulator is in low-power mode, and Flash is in deep power-down mode	102	111.2	118	
$t_{WUSTDBY}$	Wake up from standby mode	-	160	188.5	224	
$t_{WUFLASH}$	Wake up from FLASH stop mode	-	-	-	8	μs
	Wake up from FLASH deep power-down mode	-	-	-	100	

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.10 I/O port characteristics

Table 44 DC Characteristics (T_A=-40℃-85℃, V_{DD}=2~3.6V)

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{IL}	Low-level input voltage	5T, 5Tf, STD and NRST I/O	-	-	$0.3V_{DD}$	V
		BOOT0 pin	-	-	$0.1V_{DD+0.1}$	
V_{IH}	High-level input voltage	5T, 5Tf, STD and NRST I/O	$0.7V_{DD}$	-	-	V
		BOOT0 pin	$0.17V_{DD+0.7}$	-	-	
V_{hys}	Schmidt trigger hysteresis	5T, 5Tf, STD and NRST I/O	-	$10\%V_{DD}$	-	mV
		BOOT0 pin	-	100	-	
I_{lkg}	Input leakage current	$V_{SS} \leqslant V_{IN} \leqslant V_{DDA}$	-	-	±1	μA
		5T，5Tf，STD I/O， $V_{IN} \leqslant$ 5V	-	-	3	
R_{PU}	Weak pull-up equivalent resistance	Except PA10, $V_{IN}=V_{SS}$	30	40	50	kΩ
		PA10	7	10	14	
R_{PD}		Except PA10, $V_{IN}=V_{DD}$	30	40	50	

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
	Weak pull-down equivalent resistance	PA10	7	10	14	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

Table 45 AC Characteristics (T_A=25℃)

SPEED[1:0]	Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
00	$f_{max(IO)out}$	Maximum frequency	C_L=50pF,V_{DD}>2.7V	-	-	4	MHz
			C_L=50pF,V_{DD}>1.8V	-	-	2	
			C_L=10pF,V_{DD}>2.7V	-	-	8	
			C_L=10pF,V_{DD}>1.8V	-	-	4	
	$t_{f(IO)out}$/$t_{r(IO)out}$	Fall time of output from high to low level and rise time of output from low to high level	C_L=50 pF,V_{DD}=1.8 V-3.6V	-	-	100	ns
01	$f_{max(IO)out}$	Maximum frequency	C_L=50pF,V_{DD}>2.7V	-	-	25	MHz
			C_L=50pF,V_{DD}>1.8V	-	-	12.5	
			C_L=10pF,V_{DD}>2.7V	-	-	50	
			C_L=10pF,V_{DD}>1.8V	-	-	20	
	$t_{f(IO)out}$/$t_{r(IO)out}$	Fall time of output from high to low level and rise time of output from low to high level	C_L=30pF,V_{DD}>2.7V	-	-	10	ns
			C_L=30pF,V_{DD}>1.8V	-	-	20	
			C_L=10pF,V_{DD}>2.7V	-	-	8	
			C_L=10pF,V_{DD}>1.8V	-	-	17	
10	$f_{max(IO)out}$	Maximum frequency	C_L=30pF,V_{DD}>2.7V	-	-	50	MHz
			C_L=30pF,V_{DD}>1.8V	-	-	25	
			C_L=10pF,V_{DD}>2.7V	-	-	100	
			C_L=10pF,V_{DD}>1.8V	-	-	50	
	$t_{f(IO)out}$/$t_{r(IO)out}$	Fall time of output from high to low level and rise time of output from low to high level	C_L=30pF,V_{DD}>2.7V	-	-	6	ns
			C_L=30pF,V_{DD}>1.8V	-	-	10	
			C_L=10pF,V_{DD}>2.7V	-	-	4	
			C_L=10pF,V_{DD}>1.8V	-	-	6	

SPEED[1:0]	Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
11	$f_{max(IO)out}$	Maximum frequency	C_L=30pF,V_{DD}>2.7V	-	-	100	MHz
			C_L=30pF,V_{DD}>1.8V	-	-	50	
			C_L=10pF,V_{DD}>2.7V	-	-	4	
			C_L=10pF,V_{DD}>1.8V	-	-	6	
	$t_{f(IO)out}$/$t_{r(IO)out}$	Fall time of output from high to low level and rise time of output from low to high level	C_L=30pF,V_{DD}>2.7V	-	-	2.5	ns
			C_L=30pF,V_{DD}>1.8V	-	-	4	
			C_L=10pF,V_{DD}>2.7V	10	-	-	
			C_L=10pF,V_{DD}>1.8V	-	-	4	
-	$t_{EINTIpw}$	Pulse width of external signal detected by EINT controller	-	-	-	2	

Figure 12 I/O AC Characteristics Definition

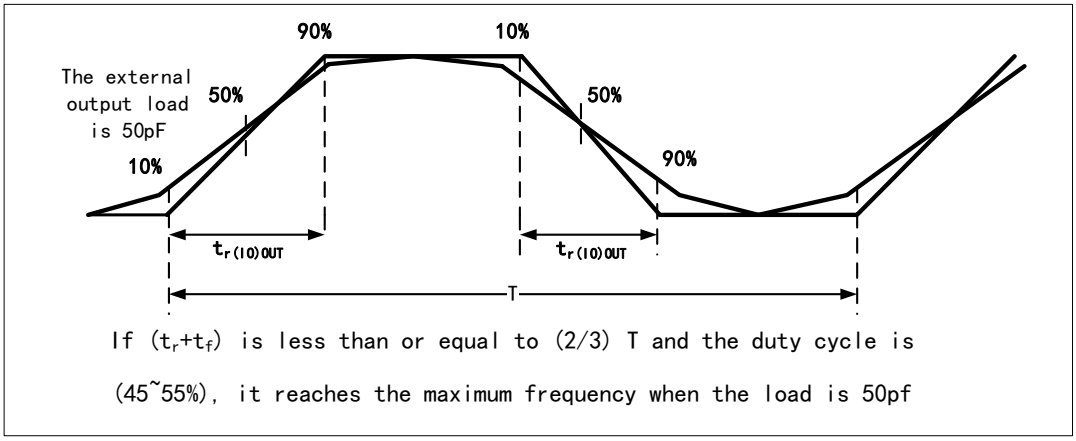


Table 46 Output Drive Voltage Characteristics (T_A=25℃)

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
V_{OL}	I/O pin outputs low voltage	$\|I_{IO}\|$=20mA, 2.7 V < V_{DD} < 3.6 V	-	1.3	V
V_{OH}	I/O pin outputs high voltage		V_{DD}-1.3	-	
V_{OL}	I/O pin outputs low voltage	CMOS port, $\|I_{IO}\|$=8mA, 2.7 V < V_{DD} < 3.6 V	-	0.4	
V_{OH}	I/O pin outputs high voltage		2.4	-	
V_{OL}	I/O pin outputs low voltage	TTL port, $\|I_{IO}\|$=8mA, 2.7 V < V_{DD} < 3.6 V	-	0.4	
V_{OH}	I/O pin outputs high voltage		V_{DD}-0.4	-	
V_{OL}	I/O pin outputs low voltage	$\|I_{IO}\|$=6mA, 2.7 V < V_{DD} < 3.6 V	-	0.4	
V_{OH}	I/O pin outputs high voltage		V_{DD}-0.4	-	

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
V_{OL}	I/O pin outputs low voltage	$\|I_{IO}\|$=4mA, 2.7 V < V_{DD} < 3.6 V	-	0.4	
V_{OH}	I/O pin outputs high voltage		V_{DD}-0.4	-	

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.11 NRST pin characteristics

CMOS process is adopted for the NRST pin input drive, which is connected to a permanent pull-up resistor R_{PU}.

Table 47 NRST Pin Characteristics (T_A=40~85℃, V_{DD}=2~3.6V)

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
R_{PU}	Weak pull-up equivalent resistance	V_{IN}=V_{SS}	30	40	50	kΩ
$V_{F(NRST)}$	NRST input filter pulse	-	-	-	100	ns
$V_{NF(NRST)}$	NRST input unfiltered pulse	V_{DD}＞2.7V	300	-	-	
T_{NRST_OUT}	Generated reset pulse duration	Reset internal source	20	-	-	μs

5.12 Communication peripheral

5.12.1 I2C peripheral characteristics

To achieve the maximum frequency of I2C in standard mode, f_{PCLK1} must be greater than 2MHz. To achieve maximum frequency of I2C in fast mode, f_{PCLK1} must be greater than 4MHz.

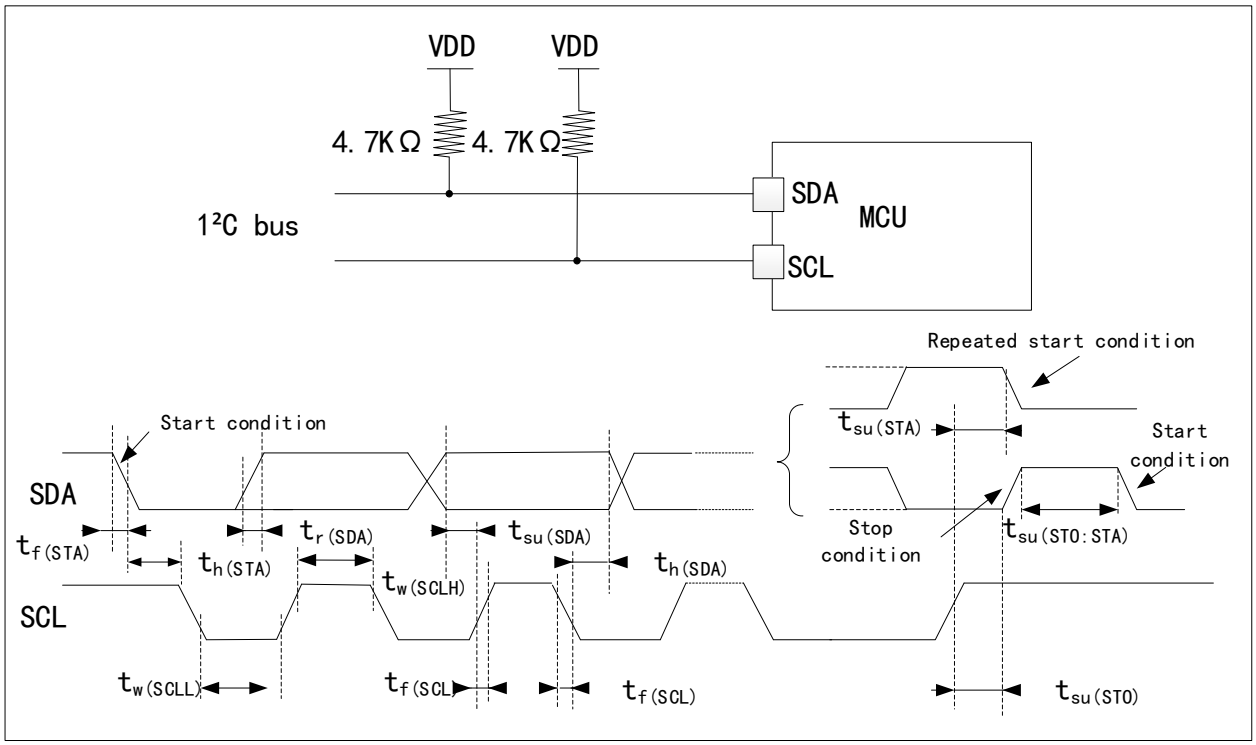
Table 48 I2C Interface Characteristics (T_A=25℃, V_{DD}=3.3V)

Symbol	Parameter	Standard I2C		Fast I2C		Unit
		Minimum value	Maximum value	Minimum value	Maximum value	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	μs
$t_{w(SCLH)}$	SCL clock high time	4	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0	3450	0	900	
$t_{r(SDA)}$/$t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$/$t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4	-	0.6	-	μs
$t_{su(STA)}$	Setup time of repeated start condition	4.7	-	0.6	-	
$t_{su(STO)}$	Setup time of stop condition	4	-	0.6	-	

Symbol	Parameter	Standard I2C		Fast I2C		Unit
		Minimum value	Maximum value	Minimum value	Maximum value	
$t_{w(STO:STA)}$	Time from stop condition to start condition (the bus is idle)	4.7	-	1.3	-	
C_b	Capacitive load of each bus	-	400	-	400	pF

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

Figure 13 Bus AC Waveform and Measurement Circuit



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.12.2 SPI peripheral characteristics

Table 49 SPI Characteristics (T_A=25℃,V_{DD}=3.3V)

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master device receive/full duplex mode, SPI1/4/5, 2.7V<V_{DD}<3.6V	-	-	42	MHz
		Master device reception/full duplex mode, SPI1/4/5, 3.0V<V_{DD}<3.6V	-	-	50	
		Master device transmit mode, SPI1/4/5,	-	-	50	

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
		1.8V<V_{DD}<3.6V				
		Master mode, SPI1/2/3/4/5, 1.8V<V_{DD}<3.6V	-	-	25	
		Slave device receive/full duplex mode, SPI1/4/5, 2.7V<V_{DD}<3.6V	-	-	38	
		Slave device transmit mode, SPI1/4/5, 1.8V<V_{DD}<3.6V	-	-	50	
		Slave mode, SPI1/2/3/4/5, 1.8V<V_{DD}<3.6V	-	-	25	
$t_{r(SCK)}$ $t_{f(SCK)}$	SP clock rise and fall time	Load capacitance: C=15pF	-	-	8	ns
$t_{su(NSS)}$	NSS setup time	Slave Mode	$4T_{PCLK}$	-	-	
$t_{h(NSS)}$	NSS hold time	Slave Mode	$2T_{PCLK}$	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, f_{PCLK}=36MHz, Prescaler factor=4	50	-	60	
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master Mode	6.5	-	-	
		Slave Mode	2.5	-	-	
$t_{h(MI)}$ $t_{h(SI)}$	Data input hold time	Master Mode	2.5	-	-	
		Slave Mode	4	-	-	
$t_{a(SO)}$	Data output access time	Slave mode, f_{PCLK}= 20MHz	-	-	$3T_{PCLK}$	
$t_{dis(SO)}$	Disable time of data output	Slave Mode	-	-	16.5	
$t_{v(SO)}$	Effective time of data output	Slave mode (after enabling the edge)	-	-	20.5	
$t_{v(MO)}$	Effective time of data output	Master mode (after enabling the edge)	-	-	4.5	
$t_{h(SO)}$	Data output hold time	Slave mode (after enabling the edge)	18	-	-	
$t_{h(MO)}$		Master mode (after enabling the edge)	0	-	--	

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

Figure 14 SPI Timing Diagram - Slave Mode and CPHA=0

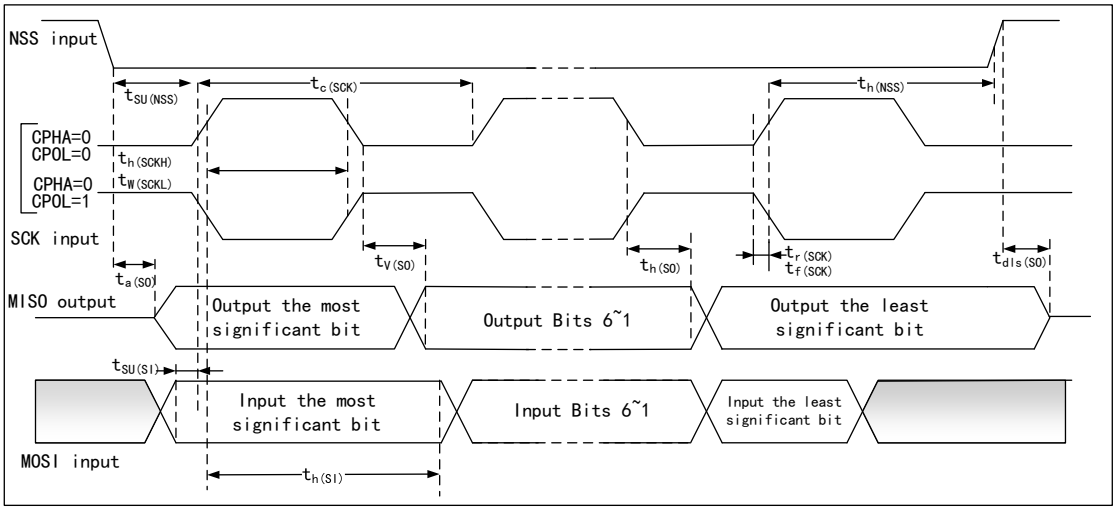
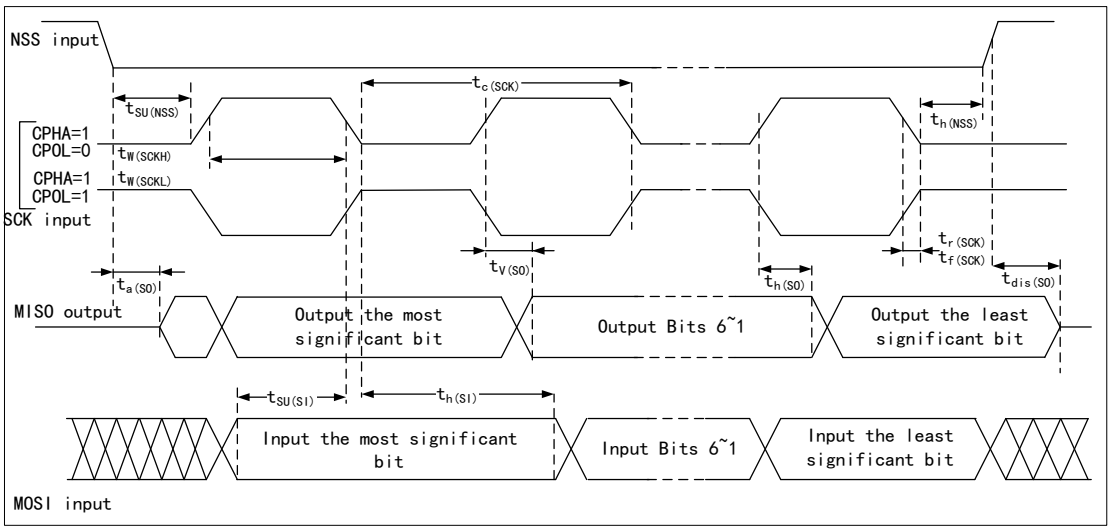
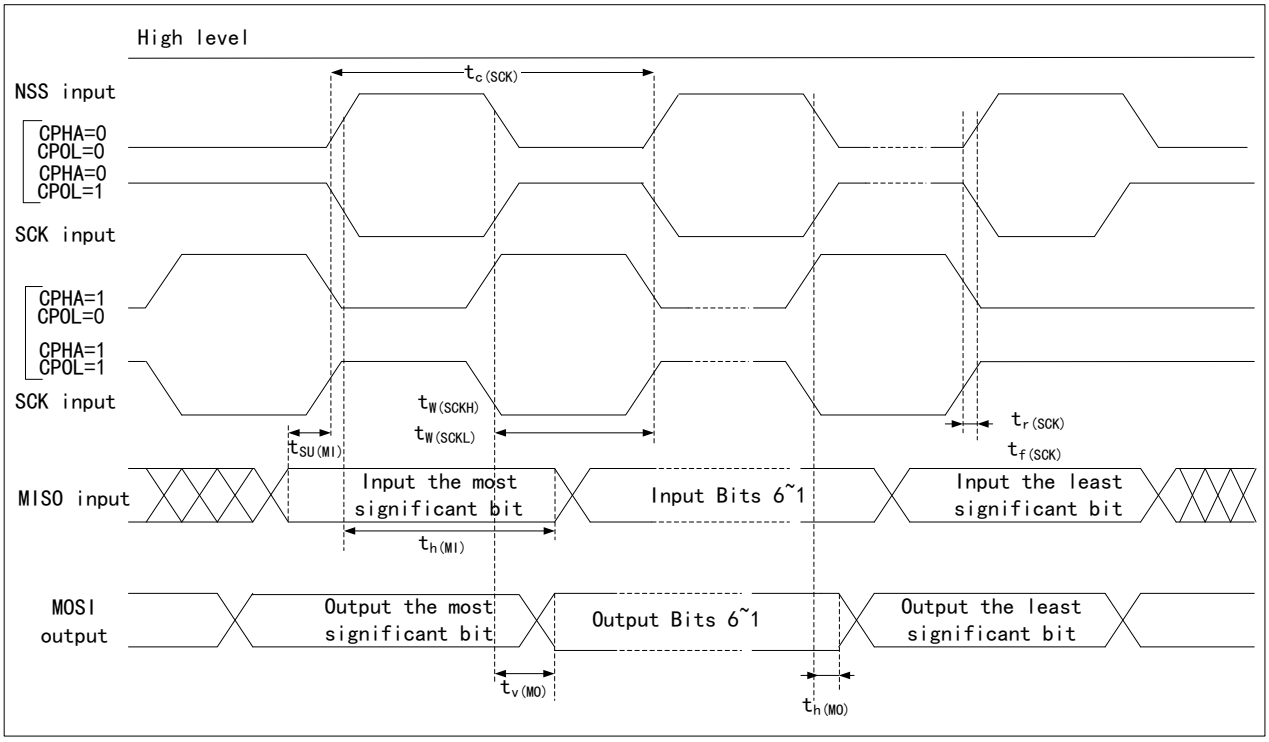


Figure 15 SPI Timing Diagram - Slave Mode and CPHA=1



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 16 SPI Timing Diagram - Master Mode



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.13 ADC

Test parameter description:

- Sampling rate: The number of conversion of analog quantity to digital quantity by ADC per second
- Sample rate=ADC clock/(number of sampling periods + number of conversion periods)

5.13.1 12-bit ADC characteristics

Table 50 12-bit ADC Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{DDA}	Supply voltage	-	1.8	-	3.6	V
I_{DDA}	ADC power	-	-	1.6	1.8	mA
f_{ADC}	ADC frequency	V_{DDA}=1.8~2.4V	0.6	15	18	MHz
		V_{DDA}=2.4~3.6V	0.6	30	36	
C_{ADC}	Internal sampling and holding capacitance	-	-	4	7	pF
R_{ADC}	Sampling resistor	-	-	-	6000	Ω

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
t_S	Sampling time	f_{ADC}=30MHz	0.1	-	16	μs
		-	3	-	480	$1/f_{ADC}$
T_{CONV}	Sampling and conversion time	f_{ADC}=30MHz,12-bit resolution	0.5	-	16.4	μs
		f_{ADC}=30MHz, 10-bit resolution	0.43	-	16.34	μs
		f_{ADC}=30MHz, 8-bit resolution	0.37	-	16.27	μs
		f_{ADC}=30MHz, 6-bit resolution	0.3	-	16.2	μs
I_{Vref}	ADC Vref DC low power in conversion mode	-	-	300	500	μA

Table 51 12-bit ADC Accuracy

Symbol	Parameter	Condition	Typical value	Maximum value	Unit
E_T	Composite error	f_{ADC}=30MHz, V_{DDA}=2.4V-3.6V V_{REF}=1.8V-3.6V T_A=-40℃~85℃	±2	±5	LSB
E_O	Offset error		±1.5	±2.5	
E_G	Gain error		±1.5	±4	
E_D	Differential linear error		±1	±2	
E_L	Integral linear error		±1.5	±3	

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

Table 52 12-bit ADC Accuracy

Symbol	Parameter	Condition	Typical value	Maximum value	Unit
E_T	Composite error	f_{ADC}=36MHz, V_{DDA}=2.4V-3.6V V_{REF}=1.8V-3.6V T_A=-40℃~85℃	±4	±7	LSB
E_O	Offset error		±5	±6	
E_G	Gain error		±3	±6	
E_D	Differential linear error		±2	±3	
E_L	Integral linear error		±3	±6	

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.13.2 Temperature Sensor Characteristics

Table 53 Temperature Sensor Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
Slope(1)	Average slope	V_{DD} = 2.4-3.6V， T_A = -40~85℃	1.88	-	2.53	mV/ºC
V_{25}	Vaoltage in 25ºC	V_{DD} =2.4-3.6V	0.75	0.76	0.79	V

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
T_{S_temp}(2)	ADC sampling time when reading temperature	-	10	-	-	μs

Note:

(1) It is guaranteed by design and will not be tested in production.

(2) The minimum sampling time can be determined by the application through multiple loops.

5.13.3 Test of built-in reference voltage characteristics

Table 54 Built-in Reference Voltage Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{REFINT}	Built-in Reference Voltage	-40℃ < T_A < +85℃	1.19	-	1.20	V
$T_{S\_vrefint}$	Sampling time of ADC when reading out internal reference voltage	-	10	-	-	μs
V_{RERINT}	Built-in reference voltage extends to temperature range	V_{DD}=3V	-	3	5	mV
T_{coeff}	temp. coefficient	-	-	30	50	ppm/℃

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.14 Comparator

表格 55 COMP1 Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{REF}	Reference voltage	V_{DD}=3.3V，T_A=25℃	-	1.65	-	V
V_r	Rising edge		-	1.65	-	
V_f	Falling edge		-	1.65	-	
V_{OFFSET}	Offset error		-	-1.70	-	
V_{hyst}	Hysteresis voltage		-	1.20	-	

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

表格 56 COMP2 Characteristics

Symbol	Parameter		Condition	Minimum value	Typical value	Maximum value	Unit
V_{REF}	Reference voltage	Low speed mode	V_{DD}=3.3V，T_A=25℃	-	1.65	-	V
		High speed mode		-	1.65	-	
V_r	Rising edge	Low speed mode		-	1.65	-	
		High speed mode		-	1.65	-	
V_f	Rising edge	Low speed mode		-	1.65	-	

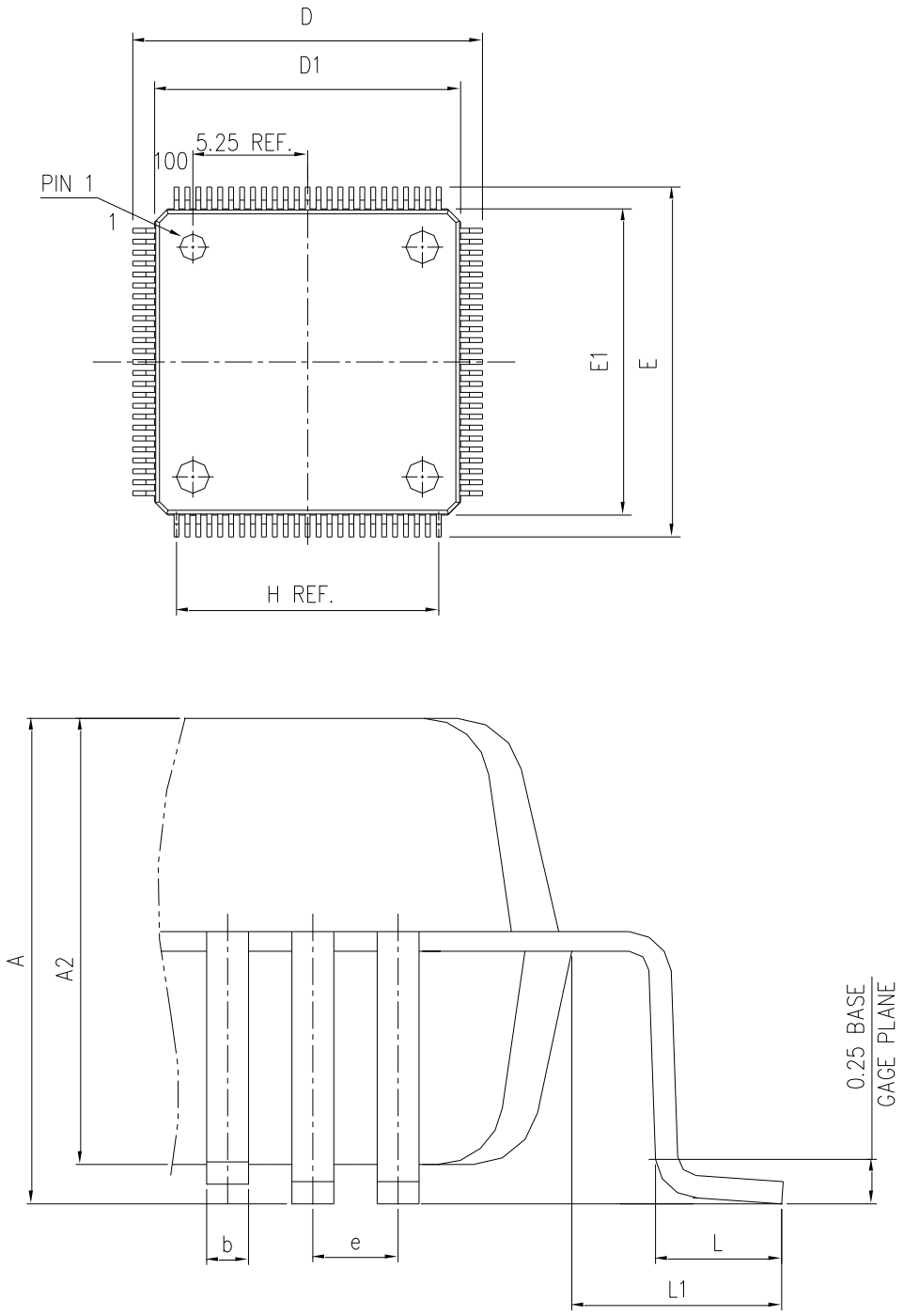
Symbol	Parameter		Condition	Minimum value	Typical value	Maximum value	Unit
		High speed mode		-	1.65	-	
V_{OFFSET}	Offset error	Low speed mode		-	-1.40	-	
		High speed mode		-	-1.30	-	
V_{hyst}	Hysteresis voltage	Low speed mode		-	1.60	-	
		High speed mode		-	1.70	-	

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

6 Package Information

6.1 LQFP100 package information

Figure 17 LQFP100 Package Diagram



（1） The figure is not drawn to scale.

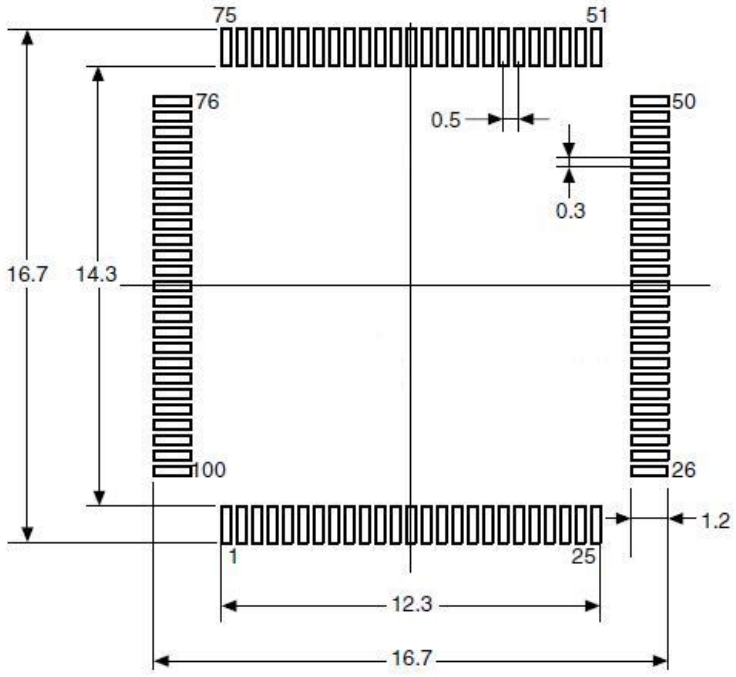
（2） All pins should be soldered to the PCB.

Table 57 LQFP100 Package Data

DIMENSION LIST（FOOTPRINT: 2.00）			
S/N	**SYM**	**DIMENSIONS**	**REMARKS**
1	A	MAX. 1.600	OVERALL HEIGHT
2	A2	1.400±0.050	PKG THICKNESS
3	D	16.000±0.200	LEAD TIP TO TIP
4	D1	14.000±0.100	PKG LENGTH
5	E	16.000±0.200	LEAD TIP TO TIP
6	E1	14.000±0.100	PKG WIDTH
7	L	0.600±0.150	FOOT LENGTH
8	L1	1.000 REF	LEAD LENGTH
9	e	0.500 BASE	LEAD PITCH
10	H（REF）	（12.00）	CUM LEAD PITCH
11	b	0.22±0.050	LEAD WIDTH

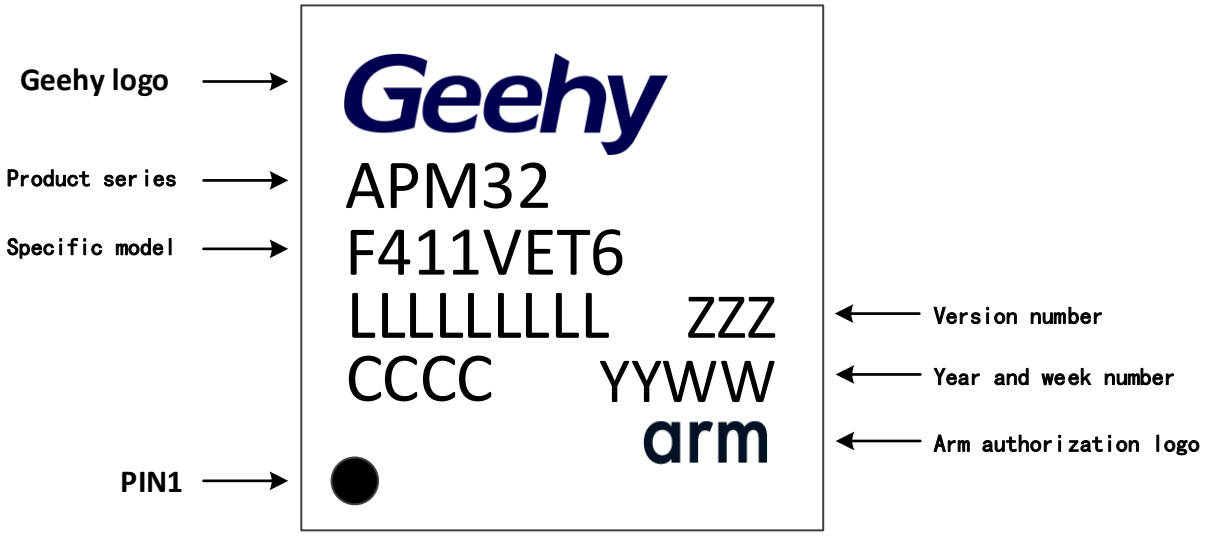
Note: Dimensions are marked in millimeters.

Figure 18 LQFP100 - 100 Pins, 14 x 14mm Welding Layout Recommendations



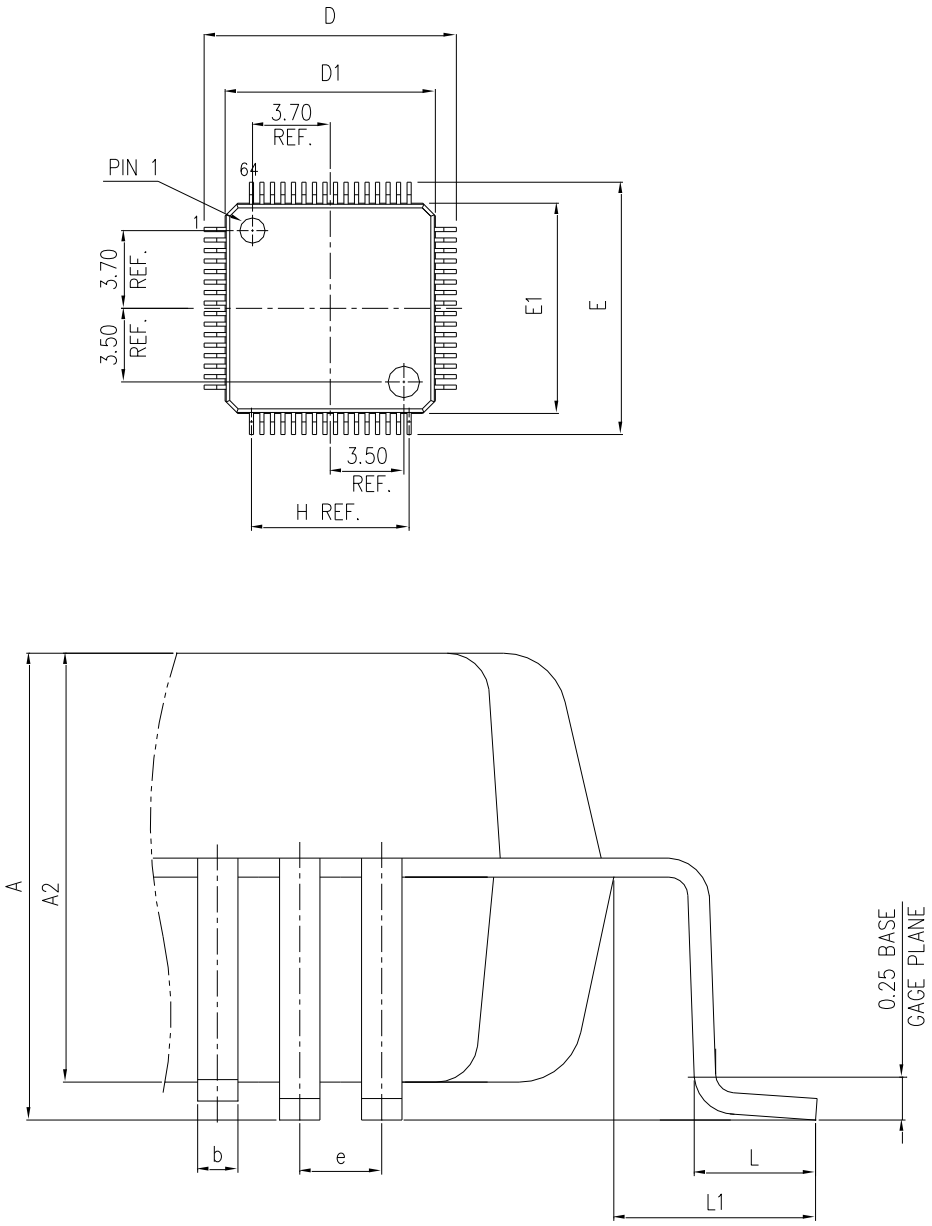
Note: Dimensions are marked in millimeters.

Figure 19 LQFP100 - 100 Pins, 14 x 14mm Diagram



6.2 LQFP64 package information

Figure 20 LQFP64 Package Diagram



（1） The figure is not drawn to scale.

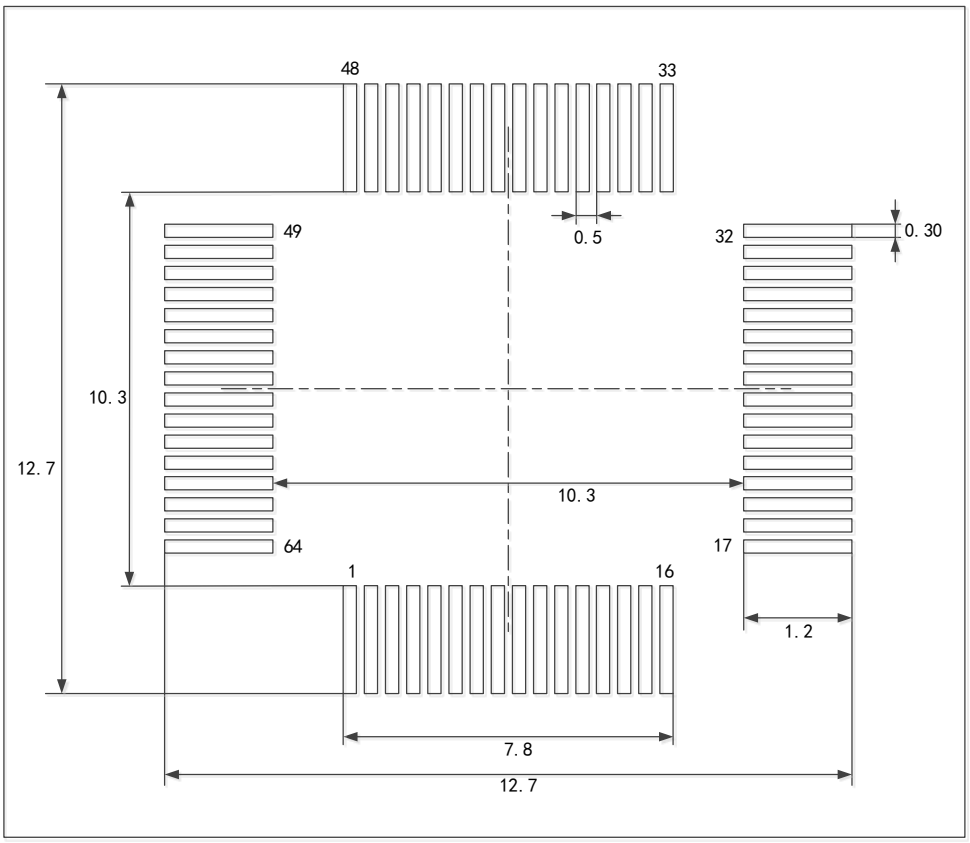
（2） All pins should be soldered to the PCB.

Table 58 LQFP64 Package Data

S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX.1.600	OVERALLHEIGHT
2	A2	1.400±0.050	PKGTHICKNESS
3	D	12.000±0.200	LEADTIPTOTIP
4	D1	10.000±0.100	PKGLENGTH
5	E	12.000±0.200	LEADTIPTOTIP
6	E1	10.000±0.100	PKGWIDTH
7	L	0.600±0.150	FOOTLENGTH
8	L1	1.000REF.	LEADLENGTH
9	e	0.500BASE	LEADPITCH
10	H(REF.)	(7.500)	GUM.LEADPITCH
11	b	0.220±0.050	LEADWIDTH

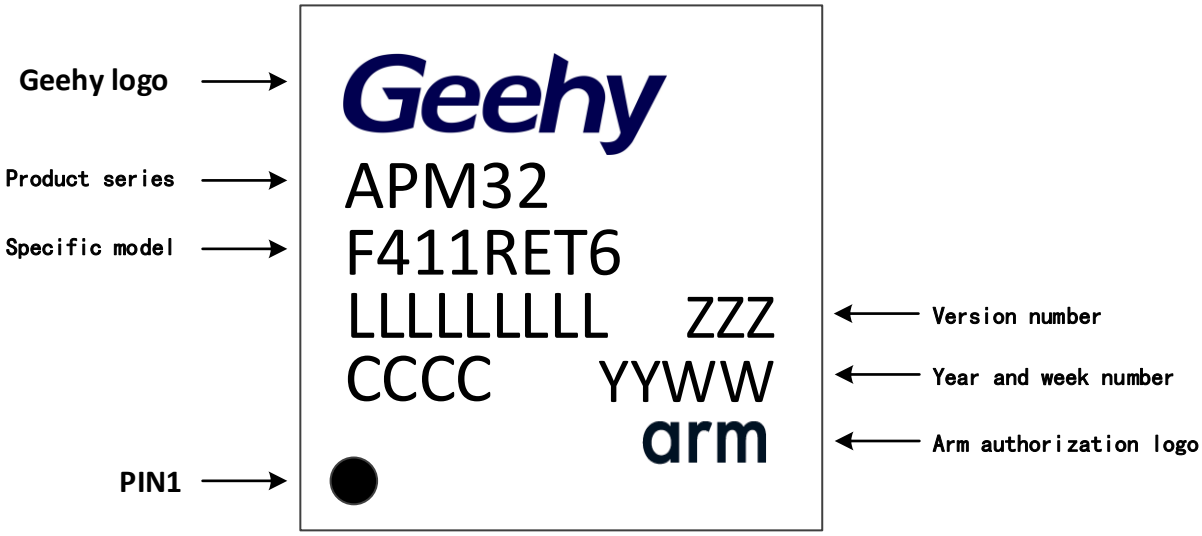
Note: Dimensions are marked in millimeters.

Figure 21 LQFP64 Welding Layout Recommendations



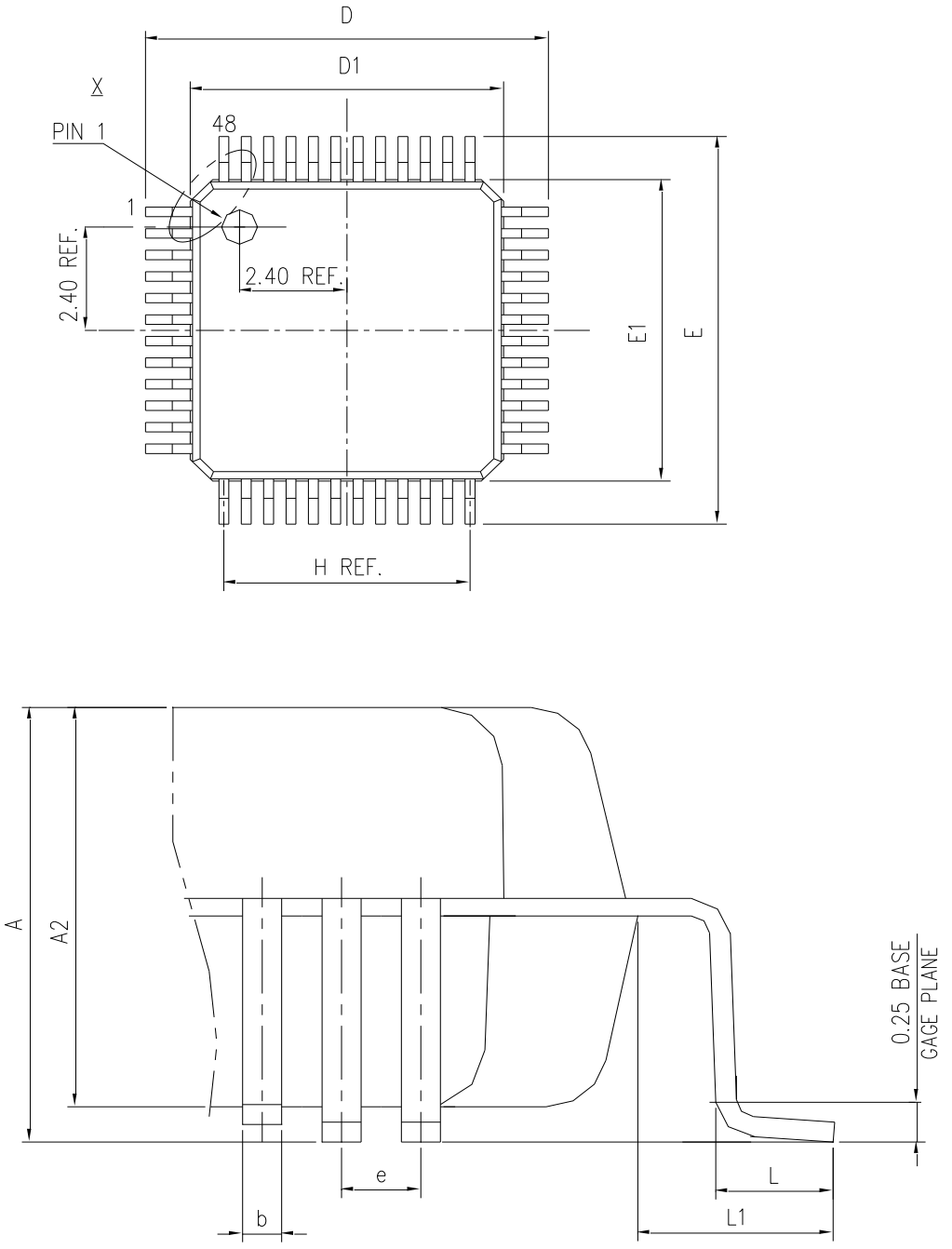
Note: Dimensions are marked in millimeters.

Figure 22 LQFP64 - 64 Pins, 10 x 10mm Diagram



6.3 LQFP48 package information

Figure 23 LQFP48 Package Diagram



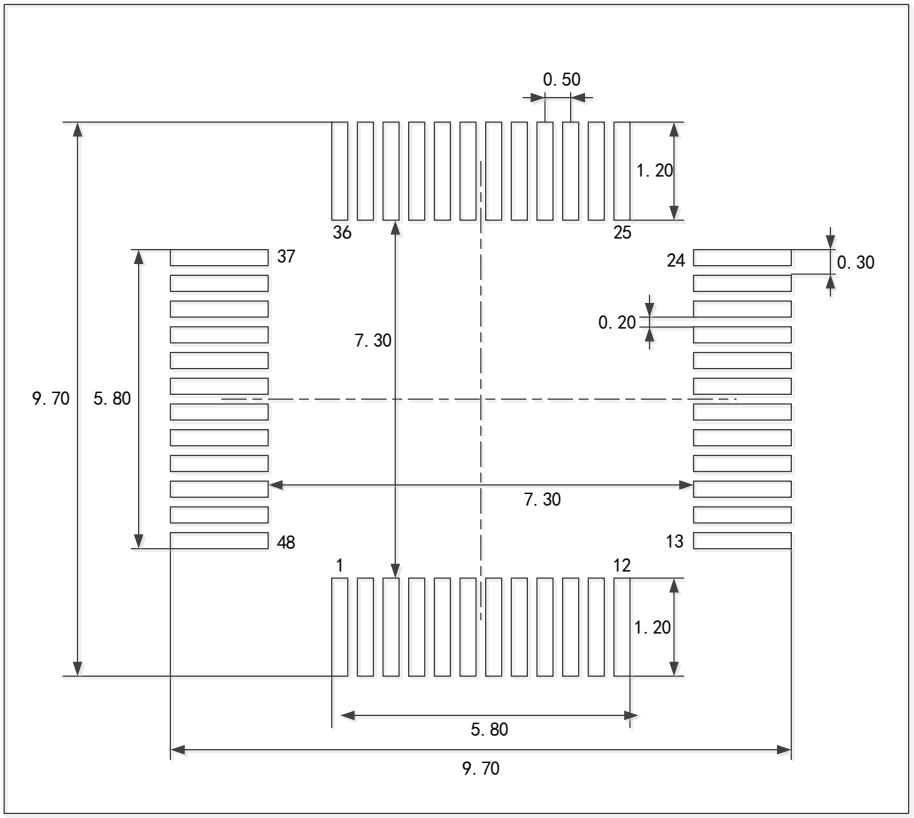
Note: The figure is not drawn to scale.

Table 59 LQFP48 Package Data

S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX.1.60	OVERALLHEIGHT
2	A2	1.40±0.05	PKGTHICKNESS
3	D	9.00±0.20	LEADTIPTOTIP
4	D1	7.00±0.10	PKGLENGTH
5	E	9.00±0.20	LEADTIPTOTIP
6	E1	7.00±0.10	PKGWIDTH
7	L	0.60±0.15	FOOTLENGTH
8	L1	1.00REF.	LEADLENGTH
9	e	0.50BASE	LEADPITCH
10	H(REF.)	（5.50）	GUM.LEADPITCH
11	b	0.22±0.050	LEADWIDTH

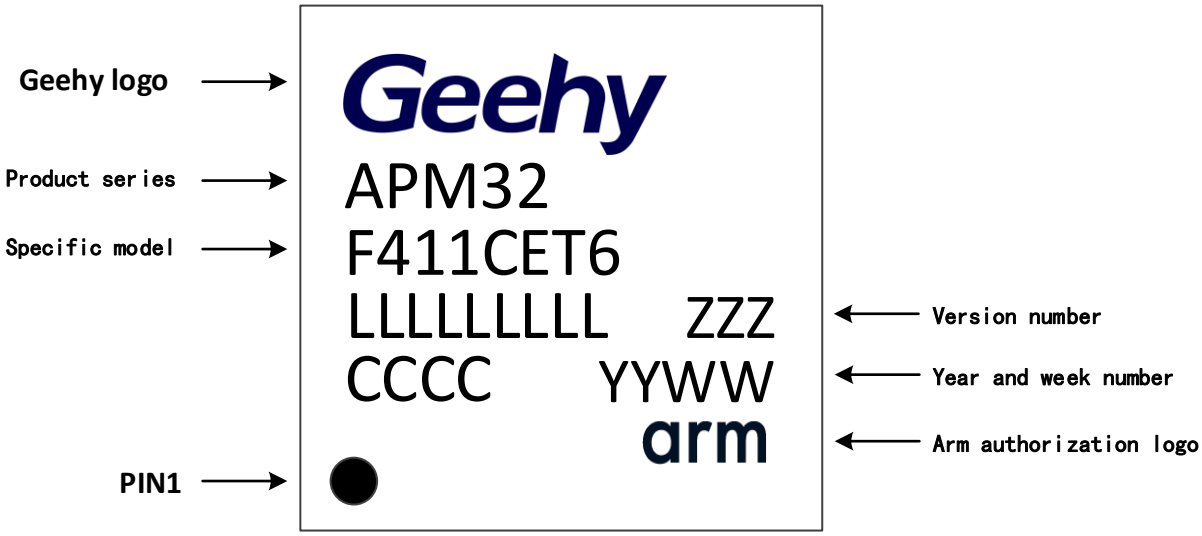
Note: Dimensions are marked in millimeters.

Figure 24 LQFP48 Welding Layout Recommendations



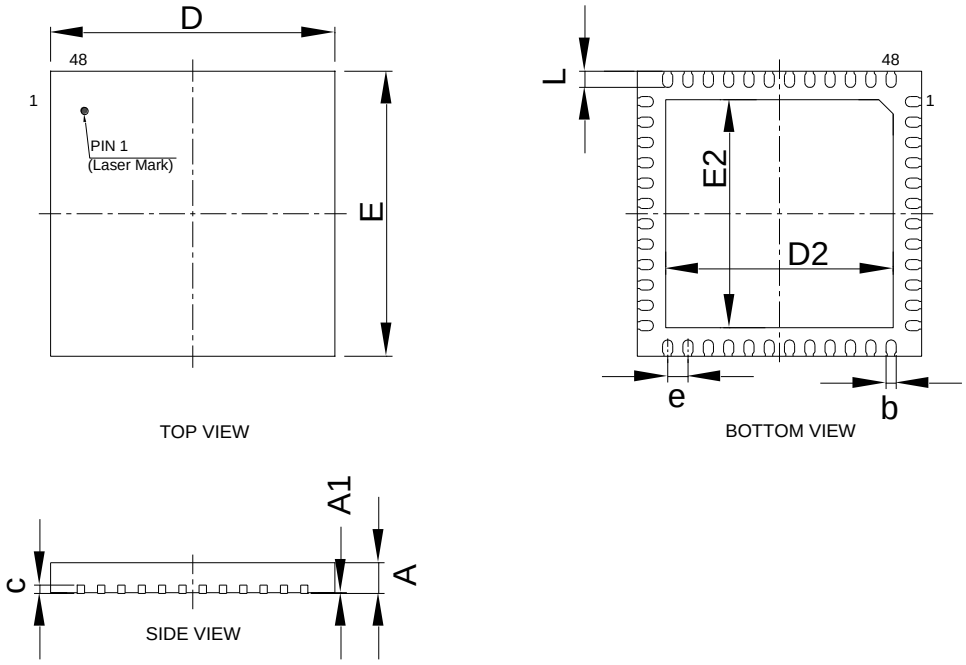
Note: Dimensions are marked in millimeters.

Figure 25 LQFP48 - 48 Pins, 10 x 10mm Diagram



6.4 QFN48 package information

Figure 26 QFN48 Package Diagram



Note: The figure is not drawn to scale.

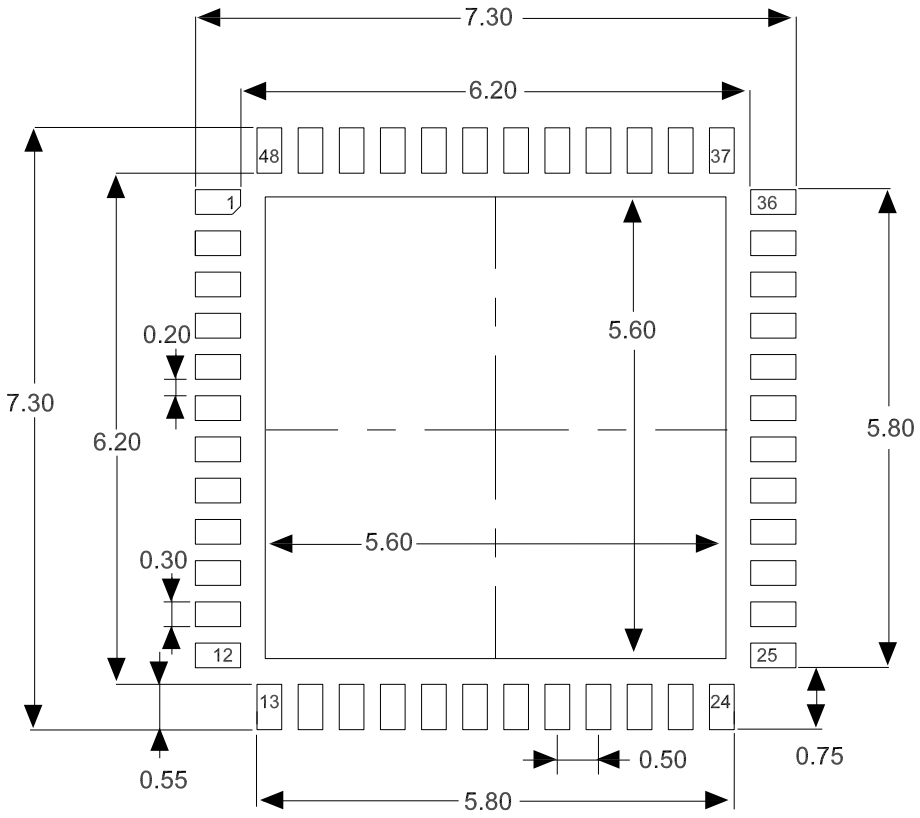
Table 60 QFN48 Package Data

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.20	0.25	0.30

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
c	0.203REF		
e	0.50BSC		
D	6.90	7.00	7.10
D2	5.50	5.60	5.70
E	6.90	7.00	7.10
E2	5.50	5.60	5.70
L	0.35	0.40	0.45

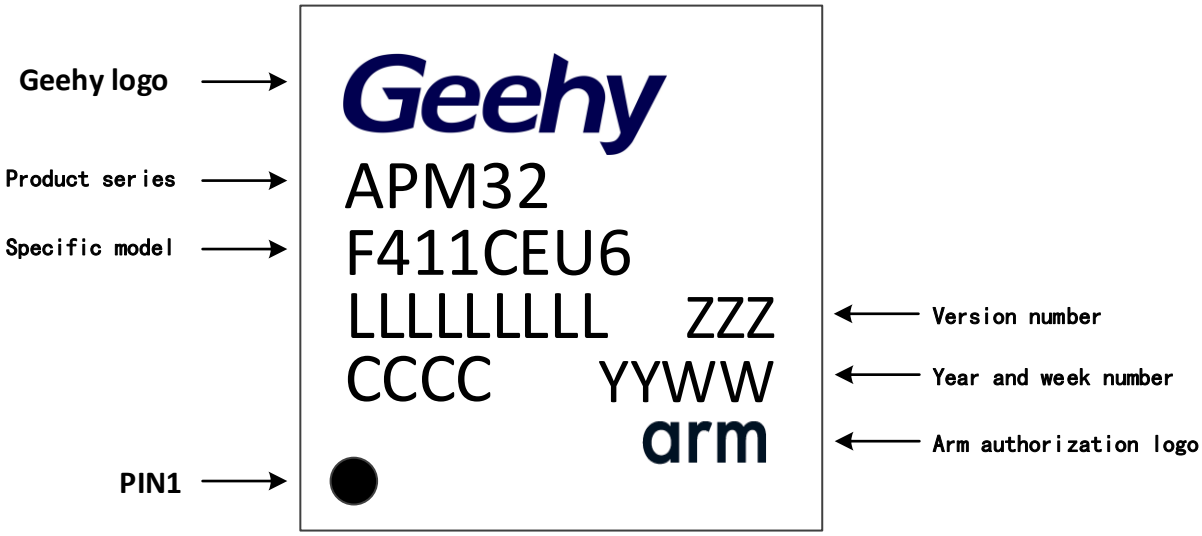
Note: Dimensions are marked in millimeters.

Figure 27 QFN48 Welding Layout Recommendations



Note: Dimensions are marked in millimeters.

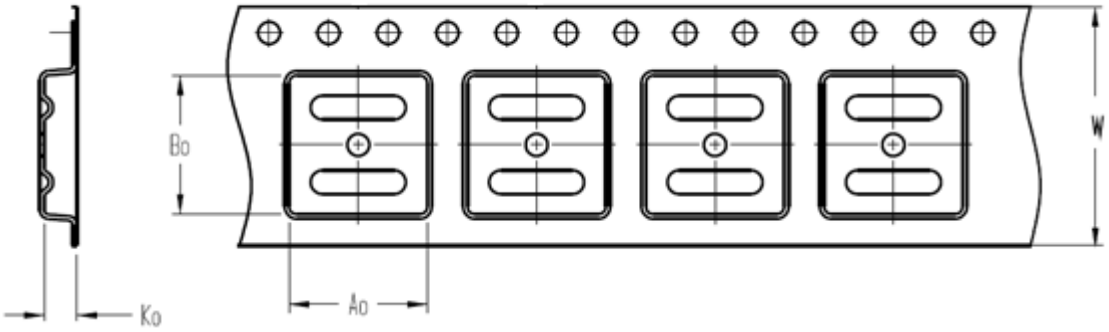
Figure 28 QFN448 - 48 Pins, 10 x 10mm Diagram



7 Packaging Information

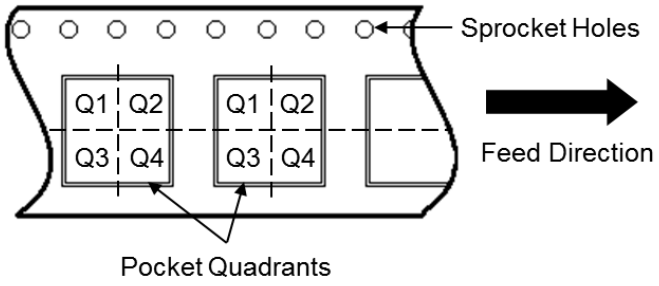
7.1 Reel packaging

Figure 29 Reel Packaging Specification Drawing

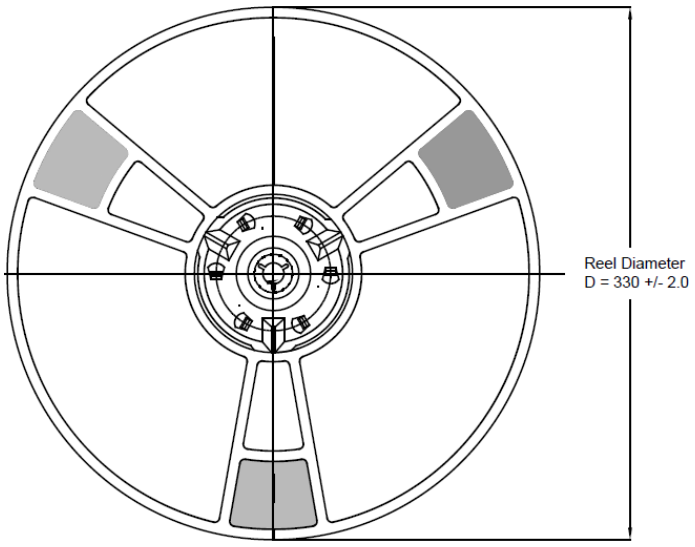


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape

Quadrant Assignments for PIN1 Orientation in Tape



Reel Dimensions



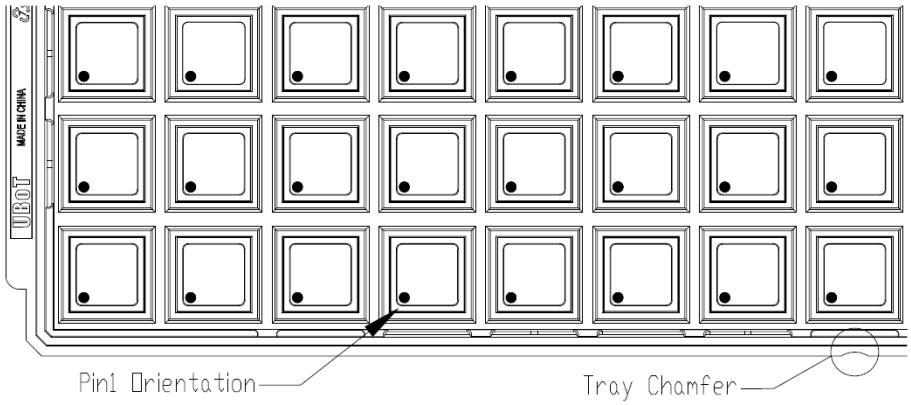
All photos are for reference only, and the appearance is subject to the product.

Table 61 Reel Packaging Parameter Specification Table

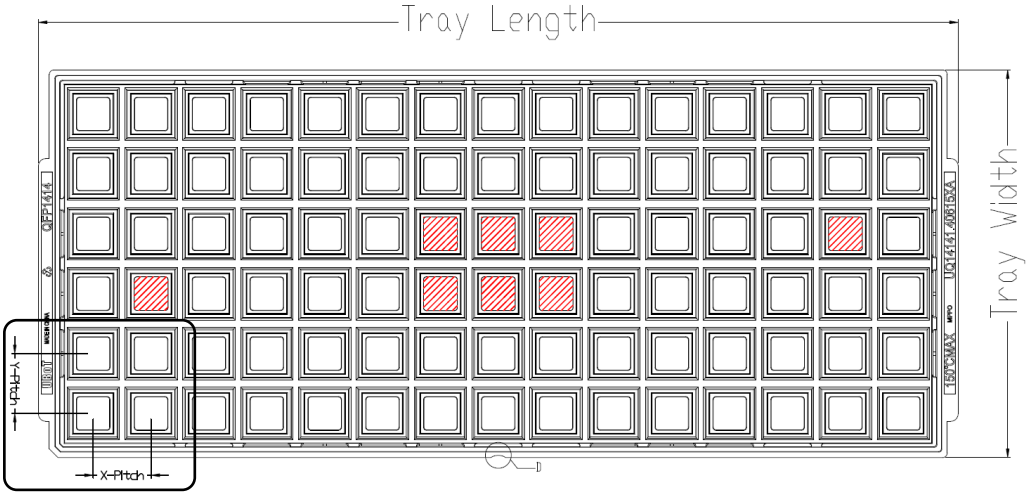
Device	Package Type	Pins	SPQ	Reel Diameter（mm）	A0（mm）	B0（mm）	K0（mm）	W（mm）	Pin1 Quadrant
APM32F411RCT6	LQFP	64	1000	330	12.35	12.35	2.2	24	Q1
APM32F411RET6	LQFP	64	1000	330	12.35	12.35	2.2	24	Q1
APM32F411CCT6	LQFP	48	2000	330	9.3	9.3	2.2	16	Q1
APM32F411CET6	LQFP	48	2000	330	9.3	9.3	2.2	16	Q1
APM32F411CCU6	QFN	48	2500	330	7.4	7.4	1.4	16	Q1
APM32F411CEU6	QFN	48	2500	330	7.4	7.4	1.4	16	Q1

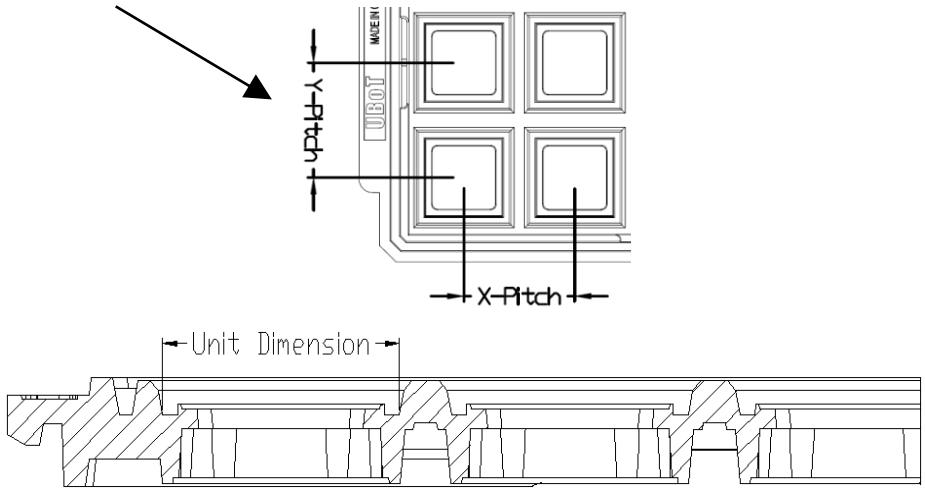
7.2 Tray packaging

Figure 30 Tray Packaging Diagram



Tray Dimensions





All photos are for reference only, and the appearance is subject to the product

Table 62 Tray Packaging Parameter Specification Table

Device	Package Type	Pins	SPQ	X-Dimension（mm）	Y-Dimension（mm）	X-Pitch（mm）	Y-Pitch（mm）	Tray Length（mm）	Tray Width（mm）
APM32F411VCT6	LQFP	100	900	16.6	16.6	20.3	21	322.6	135.9
APM32F411VET6	LQFP	100	900	16.6	16.6	20.3	21	322.6	135.9
APM32F411RCT6	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32F411RET6	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32F411CCT6	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32F411CET6	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32F411CCU6	QFN	48	2600	7.25	7.25	11.8	12.8	322.6	135.9
APM32F411CEU6	QFN	48	2600	7.25	7.25	11.8	12.8	322.6	135.9

8 Ordering Information

Figure 31 APM32F411xCxE Series Ordering Information Diagram

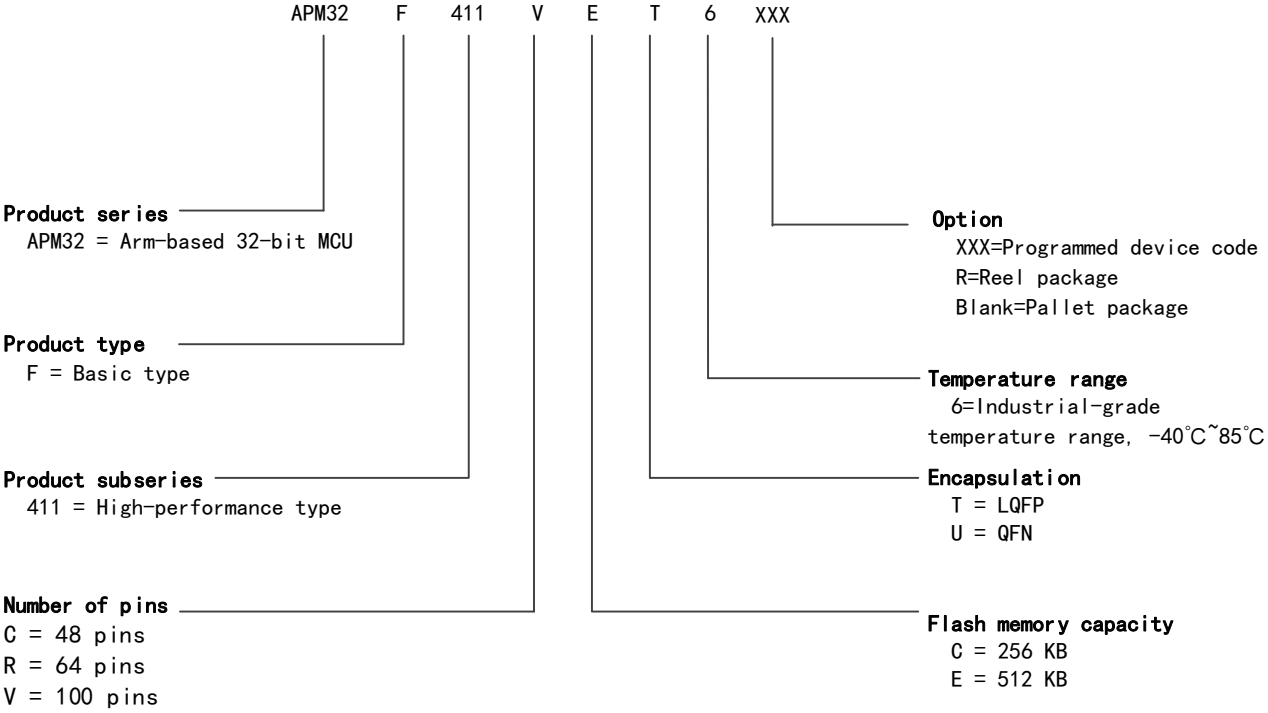


Table 63 Ordering Information Table

Order Code	FLASH(KB)	SRAM(KB)	SPQ	Package	Packaging	Temperature range
APM32F411RCT6	256	128	1600	LQFP64	Tray	-40℃ ~ 85℃
APM32F411RET6	512	128	1600	LQFP64	Tray	-40℃ ~ 85℃
APM32F411CCT6	256	128	2500	LQFP48	Tray	-40℃ ~ 85℃
APM32F411CET6	512	128	2500	LQFP48	Tray	-40℃ ~ 85℃
APM32F411CCU6	256	128	2600	QFN48	Tray	-40℃ ~ 85℃
APM32F411CEU6	512	128	2600	QFN48	Tray	-40℃ ~ 85℃
APM32F411VCT6	256	128	900	LQFP100	Reel	-40℃ ~ 85℃
APM32F411VET6	512	128	900	LQFP100	Reel	-40℃ ~ 85℃
APM32F411RCT6	256	128	1600	LQFP64	Reel	-40℃ ~ 85℃
APM32F411RET6	512	128	1600	LQFP64	Reel	-40℃ ~ 85℃
APM32F411CCT6	256	128	2500	LQFP48	Reel	-40℃ ~ 85℃
APM32F411CET6	512	128	2500	LQFP48	Reel	-40℃ ~ 85℃
APM32F411CCU6	256	128	2600	QFN48	Reel	-40℃ ~ 85℃
APM32F411CEU6	512	128	2600	QFN48	Reel	-40℃ ~ 85℃

Note: SPQ= Smallest Packaging Quantity

9 Commonly Used Function Module Denomination

Table 64 Commonly Used Function Module Denomination

Full name	Abbreviation
Reset management unit	RMU
Clock management unit	CMU
Reset and clock management	RCM
External Interrupt	EINT
General-purpose IO	GPIO
Multiplexing IO	AFIO
Wake-up controller	WUPT
Independent watchdog timer	IWDT
Window watchdog timer	WWDT
Timer	TMR
CRC controller	CRC
Power Management Unit	PMU
DMA controller	DMA
Analog-to-digital converter	ADC
Comparator	COMP
Static memory controller	SMC
Four-line serial peripheral interface	QSPI
Real-time clock	RTC
Controller local area network	CAN
I2C Interface	I2C
Serial peripheral interface	SPI
Universal asynchronous transmitter receiver	UART
Universal synchronous and asynchronous transmitter receiver	USART
Secure digital input/output	SDIO

10 Revision History

Table 65 Document Revision History

Date	Version	Change History
2023.10	1.0	New
2023.12	1.1	(1) Modify the power scheme diagram (2) Modify the voltage Vprog parameter for 8-bit programming (3) Modify the built-in reference voltage range (4) Modify pin information (5) Modify product information
2024.01	1.2	(1) Modifying COMP pin information
2024.03	1.3	(1) Modify CAN chapter description (2) Modify pin information
October, 2024	1.4	Add flash storage time and erase cycle

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