Datasheet

APM32A091RCT7

Arm® Cortex® -M0+ based 32-bit MCU

Version: V1.0

1 Product characteristics

Core

- 32-bit Arm® Cortex ® -M0+ core
- Up to 48MHz working frequency

On-chip memory

- Flash：256KB
- SRAM：32KB

Clock

- HSECLK: 4~32MHz external crystal/ ceramic oscillator supported
- LSECLK: 32.768KHz crystal/ceramic oscillator supported
- HSICLK: 8MHz RC oscillator
- HSICLK48: 48MHz RC oscillator
- HSICLK14: 14MHz RC oscillator
- LSICLK: 40KHz RC oscillator supported
- PLL: Phase locked loop, 2~16 times of frequency supported

Reset and power management

- V_{DD} range: 2.0～3.6V
- V_{DDA} range: V_{DD}～3.6V
- V_{BAT} range of RTC and backup domain power supply: 1.65V～3.6V
- V_{DDIO2} range of some I/O power supply: 1.65V～3.6V
- Power-on/power-down reset (POR/PDR) supported
- Programmable power supply voltage detector supported

Low-power mode

- Sleep, stop and standby modes supported

DMA

- Two DMAs,12 channels in total, 7 channels for DMA1 and 5 channels DMA2

Debugging interface

- SWD

I/O

- Up to 52 I/Os
- All I/Os can be mapped to external interrupt vector
- Up to 32 FT I/Os

Communication peripherals

- 2 I2C interfaces (1Mbit/s), all of which support SMBus/PMBus
- 8 USARTs, all support master synchronous SPI and modem control, 3 of which support ISO7816 interface, LIN, IrDA, automatic baud rate detection and wake-up
- 2 SPI (18Mbps) interfaces, both support I2S interface multiplexing
- 1 CAN
- 1 HDMI CEC

Analog peripherals

- 1 12-bit ADC, support up to 16 external channels
- 1 12-bit DAC, support 2 channels
- 2 programmable analog comparators
- Up to 18 capacitive sensing channels, can be used for proximity, touch key, linear or rotation sensors

Timer

- 1 16-bit advanced timer TMR1 that can provide 7-channel PWM output, support dead zone generation and braking input functions
- 1 32-bit general-purpose timer TMR2, 5 16-bit general-purpose timers TMR3/14/15/16/17, each with up to 4 independent channels to support input capture, output comparison, PWM, pulse count and other functions
- 2 16-bit basic timers TMR6/7
- 2 watchdog timers: one independent watchdog IWDT and one window watchdog WWDT
- 1 24-bit autodecrement SysTick Timer

RTC

- Support calendar function
- Alarm and periodic wake-up from stop/standby mode

CRC computing unit

96-bit unique device ID (UID)

Contents

2 Product information

See the following table for APM32A091RCT7 product functions and peripheral configuration.

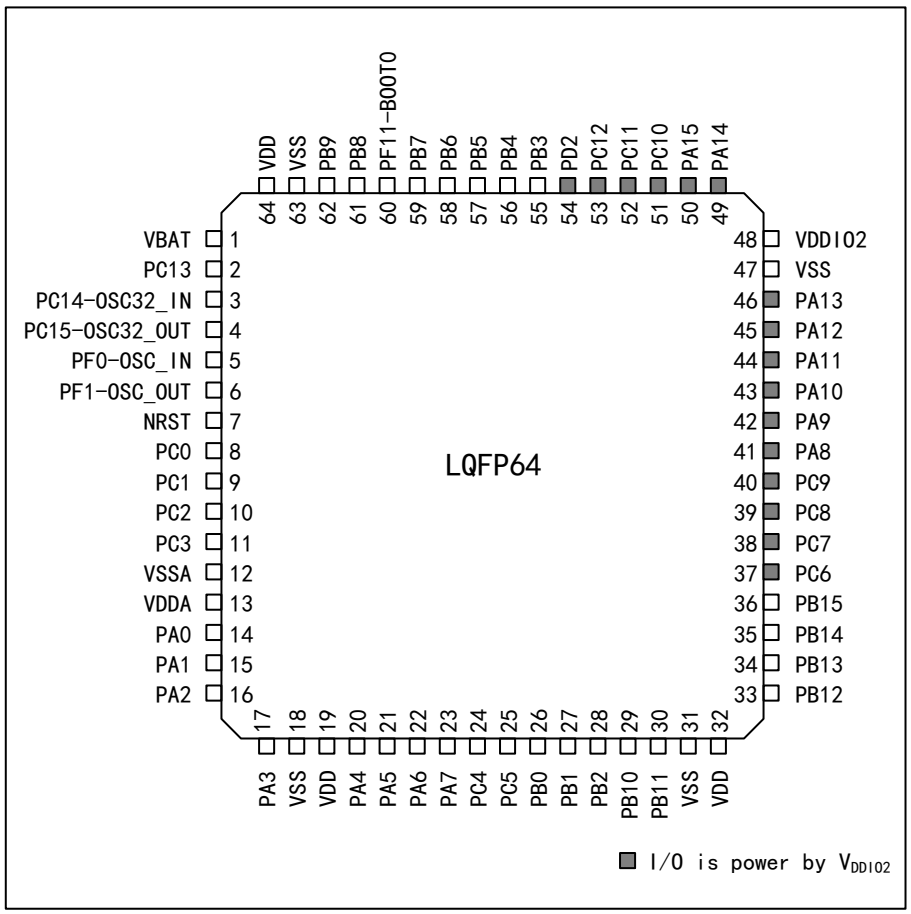
Table 1 Functions and Peripherals of APM32A091RCT7 Series Chips

Product		**APM32A091**
Model		RCT7
Package		LQFP64
Core and maximum working frequency		Arm® 32-bit Cortex®-M0+@48MHz
Operating voltage		2.0~3.6V
Flash(KB)		256
SRAM(KB)		32
GPIOs		52
Communication interface	USART	8
	SPI/I2S	2/2
	I2C	2
	CAN	1
	CEC	1
Timer	16-bit advanced	1
	16-bit general	5
	32-bit general	1
	16-bit basic	2
	System tick timer	1
	Watchdog	2
Real-time clock		1
12-bit ADC	Unit	1
	External channel	16
	Internal channel	3
12-bit DAC	Unit	1
	Channel	2
Analog comparator		2
Capacitive Sensor Channel		18
Operating temperature		Ambient temperature: -40℃ to 105℃ Junction temperature: -40℃ to 125℃

3 Pin information

3.1 Pin distribution

Figure 1 Distribution Diagram of APM32A091RCT7 Series LQFP64 Pins



3.2 Pin function description

Table 2 Legends/Abbreviations Used in Output Pin Table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in parentheses below the pin name, the pin functions during and after reset are the same as the actual pin name	
Pin type	P	Power pin
	I	Only input pin
	I/O	I/O pin
I/O structure	5T	FT I/O
	STDA	I/O with 3.3V standard, directly connected to ADC
	STD	I/O with 3.3 V tolerance
	B	Dedicated Boot0 pin
	RST	Bidirectional reset pin with built-in pull-up resistor

Name		Abbreviation	Definition
Note		Unless otherwise specified in the notes, all I/O is set as floating input during and after reset	
Pin function	Default multiplexing function	Function directly selected/enabled through peripheral register	
	Additional function	Function selected through GPIO multiplexing function register	

Table 3 Description of APM32A091RCT7 by Pin Number

Name (Function after reset)	Type	Structure	Default multiplexing function	Additional function	LQFP 64
VBAT	P	-	Backup power supply		1-
PC13	I/O	STD	-	WKUP2, RTC_TAMP1, RTC_TS, RTC_OUT	2
PC14-OSC32_IN (PC14)	I/O	STD	-	OSC32_IN	3
PC15-OSC32_OUT (PC15)	I/O	STD	-	OSC32_OUT	4
PF0-OSC_IN (PF0)	I/O	5T	CRS_SYNC, I2C1_SDA	OSC_IN	5
PF1-OSC_OUT (PF1)	I/O	5T	I2C1_SCL	OSC_OUT	6
NRST	I/O	RST	-	-	7
PC0	I/O	STDA	EVENTOUT, USART6_TX, USART7_TX	ADC_IN10	8
PC1	I/O	STDA	EVENTOUT, USART6_RX, USART7_RX	ADC_IN11	9
PC2	I/O	STDA	SPI2_MISO, I2S2_MCK, EVENTOUT, USART8_TX	ADC_IN12	10
PC3	I/O	STDA	SPI2_MOSI, I2S2_SD, EVENTOUT, USART8_RX	ADC_IN13	11
VSSA	P	-	Analog ground		12
VDDA	P	-	Analog power supply		13
PA0	I/O	STDA	USART2_CTS, TMR2_CH1_ETR, COMP1_OUT,	RTC_TAMP2, WKUP1,	14

Name (Function after reset)	Type	Structure	Default multiplexing function	Additional function	LQFP 64
			TSC_G1_IO1, USART4_TX	ADC_IN0, COMP1_INM6	
PA1	I/O	STDA	USART2_RTS, TMR2_CH2, TMR15_CH1N, TSC_G1_IO2, USART4_RX, EVENTOUT	ADC_IN1, COMP1_INP	15
PA2	I/O	STDA	USART2_TX, COMP2_OUT, TMR2_CH3, TMR15_CH1, TSC_G1_IO3	ADC_IN2, COMP2_INM6, WKUP4	16
PA3	I/O	STDA	USART2_RX, TMR2_CH4, TMR15_CH2, TSC_G1_IO4	ADC_IN3, COMP2_INP	17
VSS	P	-	Ground		18
VDD	P	-	Digital power supply		19
PA4	I/O	STDA	SPI1_NSS, I2S1_WS, TMR14_CH1, TSC_G2_IO1, USART2_CK, USART6_TX	COMP1_INM4, COMP2_INM4, ADC_IN4, DAC_OUT1	20
PA5	I/O	STDA	SPI1_SCK, I2S1_CK, CEC, TMR2_CH1_ETR, TSC_G2_IO2, USART6_RX	COMP1_INM5, COMP2_INM5, ADC_IN5, DAC_OUT2	21
PA6	I/O	STDA	SPI1_MISO, I2S1_MCK, TMR3_CH1, TMR1_BKIN, TMR16_CH1, COMP1_OUT, TSC_G2_IO3, EVENTOUT, USART3_CTS	ADC_IN6	22
PA7	I/O	STDA	SPI1_MOSI, I2S1_SD,	ADC_IN7	23

Name (Function after reset)	Type	Structure	Default multiplexing function	Additional function	LQFP 64
			TMR3_CH2, TMR14_CH1, TMR1_CH1N, TMR17_CH1, COMP2_OUT, TSC_G2_IO4, EVENTOUT		
PC4	I/O	STDA	EVENTOUT, USART3_TX	ADC_IN14	24
PC5	I/O	STDA	TSC_G3_IO1, USART3_RX	ADC_IN15, WKUP5	25
PB0	I/O	STDA	TMR3_CH3, TMR1_CH2N, TSC_G3_IO2, EVENTOUT, USART3_CK	ADC_IN8	26
PB1	I/O	STDA	TMR3_CH4, USART3_RTS TMR14_CH1, TMR1_CH3N, TSC_G3_IO3	ADC_IN9	27
PB2	I/O	5T	TSC_G3_IO4	-	28
PB10	I/O	5T	SPI2_SCK, I2S2_CK, I2C2_SCL, USART3_TX, CEC, TSC_SYNC, TMR2_CH3	-	29
PB11	I/O	5T	USART3_RX, TMR2_CH4, EVENTOUT, TSC_G6_IO1, I2C2_SDA	-	30
VSS	P	-	Ground		31
VDD	P	-	Digital power supply		32
PB12	I/O	5T	TMR1_BKIN, TMR15_BKIN, SPI2_NSS, I2S2_WS, USART3_CK,	-	33

Name (Function after reset)	Type	Structure	Default multiplexing function	Additional function	LQFP 64
			TSC_G6_IO2, EVENTOUT		
PB13	I/O	5Tf	SPI2_SCK, I2S2_CK, I2C2_SCL, USART3_CTS TMR1_CH1N, TSC_G6_IO3	-	34
PB14	I/O	5Tf	SPI2_MISO, I2S2_MCK, I2C2_SDA, USART3_RTS TMR1_CH2N, TMR15_CH1, TSC_G6_IO4	-	35
PB15	I/O	5T	SPI2_MOSI, I2S2_SD, TMR1_CH3N, TMR15_CH1N TMR15_CH2	WKUP7, RTC_REFIN	36
PC6	I/O	5T	TMR3_CH1, USART7_TX	-	37
PC7	I/O	5T	TMR3_CH2, USART7_RX	-	38
PC8	I/O	5T	TMR3_CH3, USART8_TX	-	39
PC9	I/O	5T	TMR3_CH4, USART8_RX	-	40
PA8	I/O	5T	USART1_CK, TMR1_CH1, EVENTOUT, MCO, CRS_SYNC	-	41
PA9	I/O	5T	USART1_TX, TMR1_CH2, TMR15_BKIN, TSC_G4_IO1, MCO, I2C1_SCL	-	42
PA10	I/O	5T	USART1_RX, TMR1_CH3,	-	43

Name (Function after reset)	Type	Structure	Default multiplexing function	Additional function	LQFP 64
			TMR17_BKIN, TSC_G4_IO2, I2C1_SDA		
PA11	I/O	5T	CAN_RX, USART1_CTS, TMR1_CH4, COMP1_OUT, TSC_G4_IO3, EVENTOUT, I2C2_SCL	-	44
PA12	I/O	5T	CAN_TX, USART1_RTS TMR1_ETR, COMP2_OUT, TSC_G4_IO4, EVENTOUT, I2C2_SDA	-	45
PA13	I/O	5T	IR_OUT, SWDIO	-	46
VSS	P	-	Ground		47
$V_{DDIO}2$	P	-	Digital power supply		48
PA14	I/O	5T	USART2_TX, SWCLK	-	49
PA15	I/O	5T	SPI1_NSS, I2S1_WS, USART2_RX, USART4_RTS, TMR2_CH1_ETR, EVENTOUT	-	50
PC10	I/O	5T	USART3_TX, USART4_TX	-	51
PC11	I/O	5T	USART3_RX, USART4_RX	-	52
PC12	I/O	5T	USART3_CK, USART4_CK, USART5_TX	-	53
PD2	I/O	5T	USART3_RTS TMR3_ETR, USART5_RX	-	54
PB3	I/O	5T	SPI1_SCK, I2S1_CK, TMR2_CH2,	-	55

Name (Function after reset)	Type	Structure	Default multiplexing function	Additional function	LQFP 64
			TSC_G5_IO1, EVENTOUT, USART5_TX		
PB4	I/O	5T	SPI1_MISO, I2S1_MCK, TMR17_BKIN, TMR3_CH1, TSC_G5_IO2, EVENTOUT, USART5_RX	-	56
PB5	I/O	5T	SPI1_MOSI, I2S1_SD, I2C1_SMBA, TMR16_BKIN, TMR3_CH2, USART5_CK_RTS	WKUP6	57
PB6	I/O	5Tf	I2C1_SCL, USART1_TX, TMR16_CH1N TSC_G5_IO3	-	58
PB7	I/O	5Tf	I2C1_SDA, USART1_RX, USART4_CTS TMR17_CH1N TSC_G5_IO4	-	59
PF11-BOOT0	I	B	-	Startup selection	60
PB8	I/O	5Tf	I2C1_SCL, CEC, TMR16_CH1, TSC_SYNC, CAN_RX	-	61
PB9	I/O	5Tf	SPI2_NSS, I2S2_WS, I2C1_SDA, IR_OUT,TMR17_CH1EVENTOUT, CAN_TX	-	62
VSS	P	-	Ground		63
V_{DD}	P	-	Digital power supply		64

Note:

（1） PC13, PC14 and PC15 are powered through power switch. Since the switch only sinks limited current (3mA), the use of GPIO from PC13 to PC15 in output mode is limited:

- The speed shall not exceed 2MHz when the heavy load is 30pF;
- Not used for current source (eg. driving LED).

（2） After reset, PA13 and PA14 are configured as SWDIO and SWCLK multiplexing functions, and the internal pull-up of SWDIO pin and the internal pull-down of SWCLK pin are activated.

3.3 GPIO Multiplexing Function Configuration

Table 4 GPIOA Multiplexing Function Configuration

Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	—	USART2_CTS	TMR2_CH1_ETR	TSC_G1_IO1	USART4_TX	—	—	COMP1_OUT
PA1	EVENTOUT	USART2_RTS	TMR2_CH2	TSC_G1_IO2	USART4_RX	TMR15_CH1N	—	—
PA2	TMR15_CH1	USART2_TX	TMR2_CH3	TSC_G1_IO3	—	—	—	COMP2_OUT
PA3	TMR15_CH2	USART2_RX	TMR2_CH4	TSC_G1_IO4	—	—	—	—
PA4	SPI1_NSS,I2S1_WS	USART2_CK	—	TSC_G2_IO1	TMR14_CH1	USART6_TX	—	—
PA5	SPI1_SCK,I2S1_CK	CEC	TMR2_CH1_ETR	TSC_G2_IO2	—	USART6_RX	—	—
PA6	SPI1_MISO,I2S1_MCK	TMR3_CH1	TMR1_BKIN	TSC_G2_IO3	USART3_CTS	TMR16_CH1	EVENTOUT	COMP1_OUT
PA7	SPI1_MOSI,I2S1_SD	TMR3_CH2	TMR1_CH1N	TSC_G2_IO4	TMR14_CH1	TMR17_CH1	EVENTOUT	COMP2_OUT
PA8	MCO	USART1_CK	TMR1_CH1	EVENTOUT	CRS_SYNC	—	—	—
PA9	TMR15_BKIN	USART1_TX	TMR1_CH2	TSC_G4_IO1	I2C1_SCL	MCO	—	—
PA10	TMR17_BKIN	USART1_RX	TMR1_CH3	TSC_G4_IO2	I2C1_SDA	—	—	—
PA11	EVENTOUT	USART1_CTS	TMR1_CH4	TSC_G4_IO3	CAN_RX	I2C2_SCL	—	COMP1_OUT
PA12	EVENTOUT	USART1_RTS	TMR1_ETR	TSC_G4_IO4	CAN_TX	I2C2_SDA	—	COMP2_OUT
PA13	SWDIO	IR_OUT	—	—	—	—	—	—
PA14	SWCLK	USART2_TX	—	—	—	—	—	—
PA15	SPI1_NSS,I2S1_WS	USART2_RX	TMR2_CH1_ETR	EVENTOUT	USART4_RTS	—	—	—

Table 5 GPIOB Multiplexing Function Configuration

Name	AF0	AF1	AF2	AF3	AF4	AF5
PB0	EVENTOUT	TMR3_CH3	TMR1_CH2N	TSC_G3_IO2	USART3_CK	—
PB1	TMR14_CH1	TMR3_CH4	TMR1_CH3N	TSC_G3_IO3	USART3_RTS	—
PB2	—	—	—	TSC_G3_IO4	—	—
PB3	SPI1_SCK,I2S1_CK	EVENTOUT	TMR2_CH2	TSC_G5_IO1	USART5_TX	—
PB4	SPI1_MISO,I2S1_MCK	TMR3_CH1	EVENTOUT	TSC_G5_IO2	USART5_RX	TMR17_BKIN
PB5	SPI1_MOSI,I2S1_SD	TMR3_CH2	TMR16_BKIN	I2C1_SMBA	USART5_CK_RTS	—
PB6	USART1_TX	I2C1_SCL	TMR16_CH1N	TSC_G5_IO3	—	—
PB7	USART1_RX	I2C1_SDA	TMR17_CH1N	TSC_G5_IO4	USART4_CTS	—
PB8	CEC	I2C1_SCL	TMR16_CH1	TSC_SYNC	CAN_RX	—
PB9	IR_OUT	I2C1_SDA	TMR17_CH1	EVENTOUT	CAN_TX	SPI2_NSS,I2S2_WS
PB10	CEC	I2C2_SCL	TMR2_CH3	TSC_SYNC	USART3_TX	SPI2_SCK,I2S2_CK
PB11	EVENTOUT	I2C2_SDA	TMR2_CH4	TSC_G6_IO1	USART3_RX	—
PB12	SPI2_NSS,I2S2_WS	EVENTOUT	TMR1_BKIN	TSC_G6_IO2	USART3_CK	TMR15_BKIN
PB13	SPI2_SCK,I2S2_CK	—	TMR1_CH1N	TSC_G6_IO3	USART3_CTS	I2C2_SCL
PB14	SPI2_MISO,I2S2_MCK	TMR15_CH1	TMR1_CH2N	TSC_G6_IO4	USART3_RTS	I2C2_SDA
PB15	SPI2_MOSI,I2S2_SD	TMR15_CH2	TMR1_CH3N	TMR15_CH1N	—	—

Table 6 GPIOC Multiplexing Function Configuration

Name	AF0	AF1	AF2
PC0	EVENTOUT	USART7_TX	USART6_TX
PC1	EVENTOUT	USART7_RX	USART6_RX
PC2	EVENTOUT	SPI2_MISO,I2S2_MCK	USART8_TX
PC3	EVENTOUT	SPI2_MOSI,I2S2_SD	USART8_RX
PC4	EVENTOUT	USART3_TX	—
PC5	TSC_G3_IO1	USART3_RX	—
PC6	TMR3_CH1	USART7_TX	—
PC7	TMR3_CH2	USART7_RX	—
PC8	TMR3_CH3	USART8_TX	—
PC9	TMR3_CH4	USART8_RX	—
PC10	USART4_TX	USART3_TX	—
PC11	USART4_RX	USART3_RX	—
PC12	USART4_CK	USART3_CK	USART5_TX
PC13	—	—	—
PC14	—	—	—
PC15	—	—	—

Table 7 GPIOD Multiplexing Function Configuration

Name	AF0	AF1	AF2
PD2	TMR3_ETR	USART3_RTS	USART5_RX

Table 8 GPIOF Multiplexing Function Configuration

Name	AF0	AF1	AF2
PF0	CRS_SYNC	I2C1_SDA	-
PF1	-	I2C1_SCL	-

4 Functional description

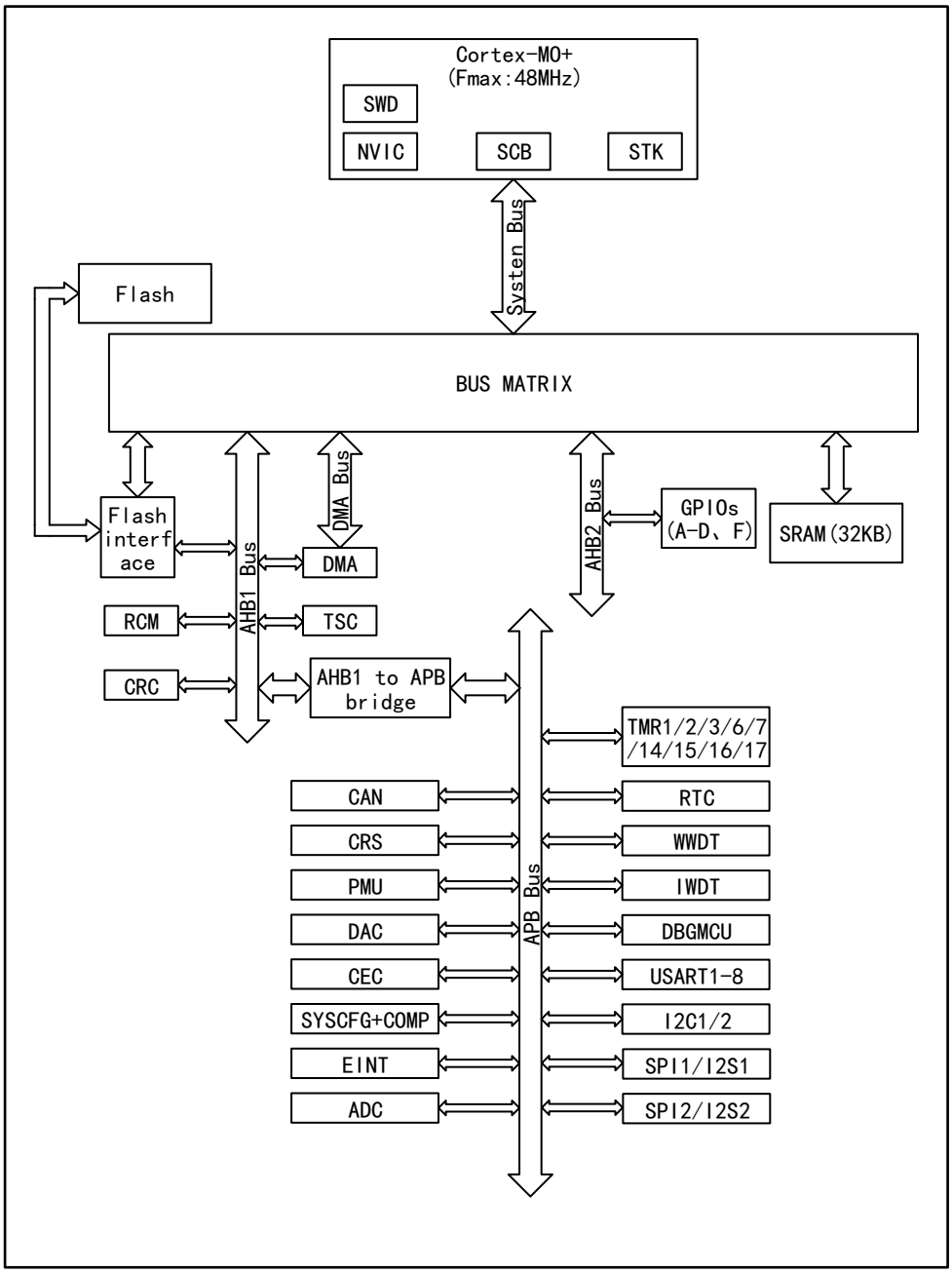
This chapter mainly introduces the system architecture, interrupt, on-chip memory, clock, power supply and peripheral features of APM32A091RCT7 series products; for information about the Arm® Cortex®-M0+ core, please refer to the Arm® Cortex®-M0+ technical reference manual, which can be downloaded from Arm's website.

Currently, the APM32A091RCT7 model has passed the AEC-Q100-Rev-H Grade2 standard.

4.1 System architecture

4.1.1 System Block Diagram

Figure 2 APM32A091RCT7 System Block Diagram



4.1.2 Address mapping

Table 9 APM32A091RCT7 Storage Mapping Table

Region	Start address	Peripheral Name
Code	0x0000 0000	Code mapping area
Code	0x0004 0000	Reserved
Code	0x0800 0000	Main memory area

Region	Start address	Peripheral Name
Code	0x0804 0000	Reserved
Code	0x1FFF D800	BootLoader
Code	0x1FFF F800	Option byte
Code	0x1FFF FC00	Reserved
SRAM	0x2000 0000	SRAM
—	0x2000 8000	Reserved
APB bus	0x4000 0000	TMR2
APB bus	0x4000 0400	TMR3
APB bus	0x4000 0800	Reserved
APB bus	0x4000 1000	TMR6
APB bus	0x4000 1400	TMR7
APB bus	0x4000 1800	Reserved
APB bus	0x4000 2000	TMR14
APB bus	0x4000 2400	Reserved
APB bus	0x4000 2800	RTC
APB bus	0x4000 2C00	WWDT
APB bus	0x4000 3000	IWDT
APB bus	0x4000 3400	Reserved
APB bus	0x4000 3800	SPI2/I2S2
APB bus	0x4000 3C00	Reserved
APB bus	0x4000 4400	USART2
APB bus	0x4000 4800	USART3
APB bus	0x4000 4C00	USART4
APB bus	0x4000 5000	USART5
APB bus	0x4000 5400	I2C1
APB bus	0x4000 5800	I2C2
APB bus	0x4000 5C00	Reserved
APB bus	0x4000 6000	CAN RAM
APB bus	0x4000 6100	Reserved
APB bus	0x4000 6400	CAN
APB bus	0x4000 6800	Reserved
APB bus	0x4000 6C00	CRS
APB bus	0x4000 7000	PMU
APB bus	0x4000 7400	DAC
APB bus	0x4000 7800	CEC
APB bus	0x4000 7C00	Reserved
—	0x4000 8000	Reserved
APB bus	0x4001 0000	SYSCFG+COMP
APB bus	0x4001 0400	EINT
APB bus	0x4001 0800	Reserved

Region	Start address	Peripheral Name
APB bus	0x4001 1400	USART6
APB bus	0x4001 1800	USART7
APB bus	0x4001 1C00	USART8
APB bus	0x4001 2000	Reserved
APB bus	0x4001 2400	ADC
APB bus	0x4001 2800	Reserved
APB bus	0x4001 2C00	TMR1
APB bus	0x4001 3000	SPI1/I2S1
APB bus	0x4001 3400	Reserved
APB bus	0x4001 3800	USART1
APB bus	0x4001 3C00	Reserved
APB bus	0x4001 4000	TMR15
APB bus	0x4001 4400	TMR16
APB bus	0x4001 4800	TMR17
APB bus	0x4001 4C00	Reserved
APB bus	0x4001 5800	DBGMCU
APB bus	0x4001 5C00	Reserved
—	0x4001 8000	Reserved
AHB1 bus	0x4002 0000	DMA
AHB1 bus	0x4002 0400	Reserved
AHB1 bus	0x4002 1000	RCM
AHB1 bus	0x4002 1400	Reserved
AHB1 bus	0x4002 2000	Flash interface
AHB1 bus	0x4002 2400	Reserved
AHB1 bus	0x4002 3000	CRC
AHB1 bus	0x4002 3400	Reserved
AHB1 bus	0x4002 4000	TSC
—	0x4002 4400	Reserved
AHB2 bus	0x4800 0000	GPIOA
AHB2 bus	0x4800 0400	GPIOB
AHB2 bus	0x4800 0800	GPIOC
AHB2 bus	0x4800 0C00	GPIOD
AHB2 bus	0x4800 1000	Reserved
AHB2 bus	0x4800 1400	GPIOF
—	0x4800 1800	Reserved
Core	0xE000 E010	STK
Core	0xE000 E100	NVIC
Core	0xE000 ED00	SCB
—	0xE010 0000	Reserved

4.1.3 Startup configuration

At startup, the user can select one of the following three startup modes by setting the high and low levels of the Boot pin or configuring nBOOT bits:

- Startup from main memory
- Startup from BootLoader
- Startup from built-in SRAM

The user can use USART or I2C interface to reprogram the user Flash if boot from BootLoader.

4.2 Core

The core of APM32A091RCT7 is Arm® Cortex®-M0+. Based on this platform, the development cost is low and the power consumption is low. It can provide excellent computing performance and advanced system interrupt response, and is compatible with all Arm tools and software.

4.3 Interrupt controller

4.3.1 Nested Vector Interrupt Controller (NVIC)

It embeds a nested vectored interrupt controller (NVIC) able to handle up to 32 maskable interrupt channels (not including16 interrupt lines of Cortex-M3) and 4 priority levels. The interrupt vector entry address can be directly transmitted to the core, so that the interrupt response processing with low delay can give priority to the late higher priority interrupt.

4.3.2 External Interrupt/Event Controller (EINT)

The external interrupt/event controller consists of 32 edge detectors, and each detector includes edge detection circuit and interrupt/event request generation circuit; each detector can be configured as rising edge trigger, falling edge trigger or both and can be masked independently. Up to 52 GPIOs can be connected to the 16 external interrupt lines.

4.4 On-chip memory

On-chip memory includes main memory area, SRAM and information block; the information block includes system memory area and option byte; the system memory area stores BootLoader, 96-bit unique device ID and capacity information of main memory area; the system memory area has been written into the program and cannot be erased.

Table 10 On-chip Memory Area

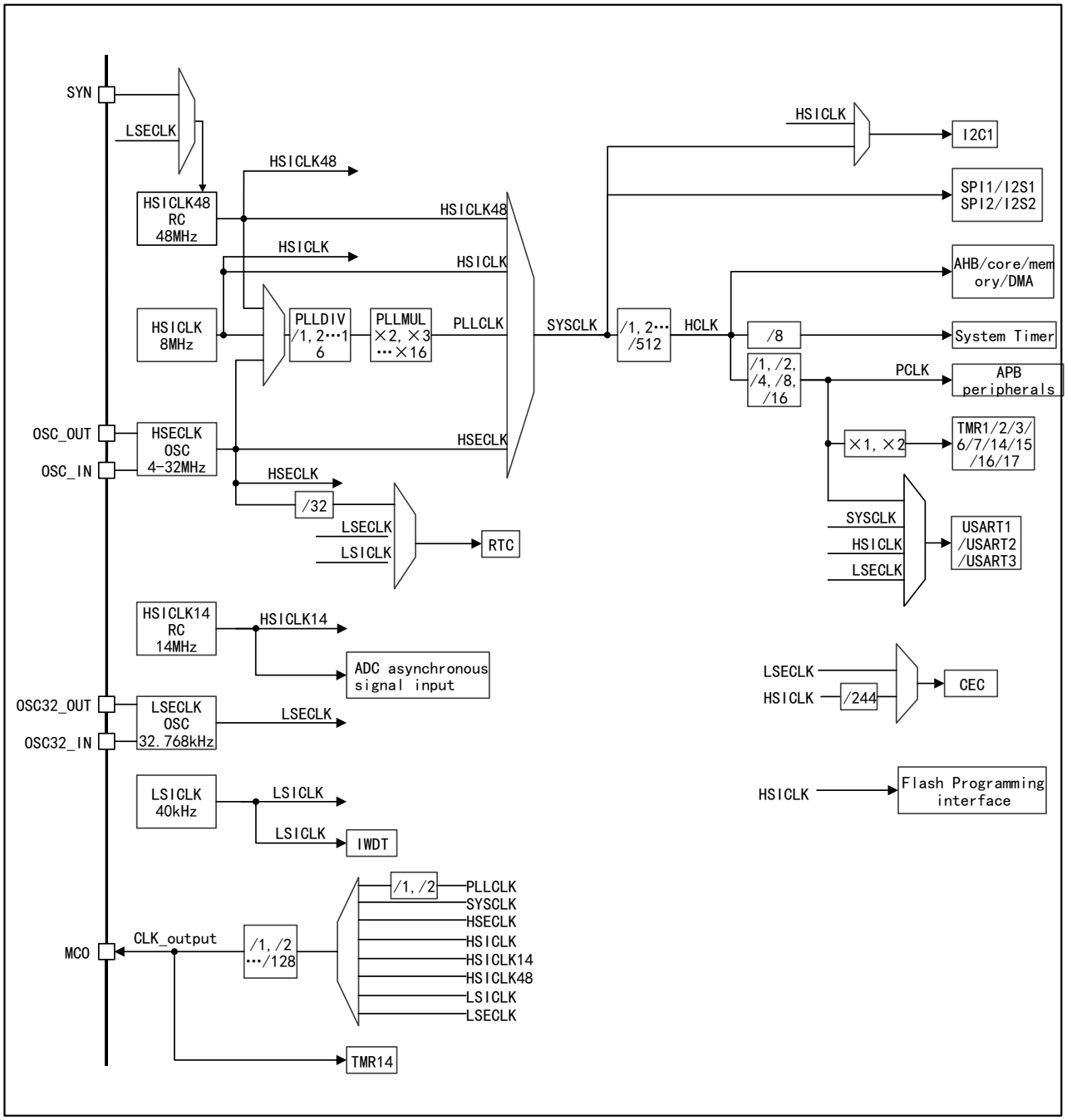
Memory	Maximum capacity	Function
Main memory area	256 KB	Store user programs and data.
SRAM	32 KB	CPU can access at 0 waiting cycle (read/write).
System memory area	8KB	Store BootLoader, 96-bit unique device ID, and main memory area capacity information

Memory	Maximum capacity	Function
Option byte	16Bytes	Configure main memory area read-write protection and MCU working mode

4.5 Clock

Clock tree of APM32A091RCT7 is shown in the figure below:

Figure 3 APM32A091RCT7 Clock Tree



4.5.1 Clock source

Clock source is divided into high-speed clock and low-speed clock according to the speed; the

high-speed clock includes HSICLK48, HSICLK14, HSICLK and HSECLK, and the low-speed clock includes LSECLK and LSICLK; clock source is divided into internal clock and external clock according to the chip inside/outside; the internal clock includes HSICLK48, HSICLK14, HSICLK and LSICLK, and the external clock includes HSECLK and LSECLK, among which HSICLK48, HSICLK14 and HSICLK are calibrated by the factory.

4.5.2 System clock

HSICLK, HSICLK48, PLLCLK and HSECLK can be selected as system clock; the clock source of PLLCLK can be one of HSICLK, HSICLK48 and HSECLK; the required system clock can be obtained by configuring PLL clock multiplier factor and frequency division factor.

When the product is reset and started, HSICLK is selected as the system clock by default, and then the user can choose one of the above clock sources as the system clock by himself. When HSECLK failure is detected, the system will automatically switch to the HSICLK, and if an interrupt is enabled, the software can receive the related interrupt.

4.5.3 Bus clock

AHB, APB1 and ABP2 are built in. The clock source of AHB is SYSCLK and the clock source of APB1 and APB2 is AHB_CLK; the required clock frequency can be obtained by configuring the frequency division factor.

4.5.4 CRS

Clock Recovery System (CRS) is an embedded module for automatic calibration of 48MHz internal oscillator. The automatic calibration is based on external synchronization signals. Calibration can be completed faster at startup by combining automatic and manual operation.

4.6 Reset and power management

4.6.1 Power supply scheme

Table 11 Power Supply Scheme

Name	Voltage range	Instruction
V_{DD}/V_{DDIO1}	2.0~3.6V	I/Os (see pin distribution diagram for specific IO) and internal voltage regulator are powered through V_{DD} pin.
V_{DDIO2}	1.65-3.6V	I/Os (see pin distribution diagram for specific IO) are powered through V_{DDIO2} pin.
V_{DDA}	V_{DD}~3.6V	The V_{DDA} supplies power to the ADC, reset module, RC oscillator and PLL, and the voltage level of V_{DDA} must always be greater than or equal to the voltage level of V_{DD}, which should be given priority.
V_{BAT}	1.65-3.6V	When V_{DD} is powered off, RTC, external 32KHz oscillator and backup register are supplied through V_{BAT} pin.

4.6.2 Voltage regulator

Table 12 Regulator Operating Mode

Name	Instruction
Master mode (MR)	Used in run mode
Low-power mode (LPR)	Used in stop mode
Power-down mode	Used in standby mode, when the voltage regulator has high impedance output, the core circuit is powered down, the power consumption of the voltage regulator is zero, and all data of registers and SRAM will be lost.

Note: The voltage regulator is always in working state after reset, and outputs with high impedance in power-down mode.

4.6.3 Power supply voltage monitor

Power-on reset (POR) and power-down reset (PDR) circuits are integrated inside the product. These two circuits are always in working condition. When the power-down reset circuit monitors that the power supply voltage is lower than the specified threshold value ($V_{POR/PDR}$), even if the external reset circuit is used, the system will remain reset.

The product has a built-in programmable voltage regulator (PVD) that can monitor V_{DD} and compare it with V_{PVD} threshold. When V_{DD} is outside the V_{PVD} threshold range and the interrupt is enabled, the MCU can be set to a safe state through the interrupt service program.

4.7 Low-power mode

APM32A091RCT7 supports three low-power modes, namely, sleep mode, stop mode and standby mode, and there are differences in power, wake-up time and wake-up mode among these three modes. The low-power mode can be selected according to the actual application requirements.

Table13 Low-power Mode

Mode	Instruction
Sleep mode	The core stops working, all peripherals are working, and it can be woken up through interrupts/events
Stop mode	Under the condition that SRAM and register data are not lost, the stop mode can achieve the lowest power consumption; The clock of the internal 1.5V power supply module will stop, HSECLK crystal resonator, HSICLK and PLL will be prohibited, and the voltage regulator can be configured in normal mode or low power mode; Any external interrupt line can wake up MCU, and the external interrupt lines include one of the 16 external interrupt lines, PVD output, RTC, I2C1, USART1, USART2, USART3, analog comparator and CEC.
Standby mode	The power consumption in this mode is the lowest; Internal voltage regulator is turned off, all 1.5V power supply modules are powered off, HSECLK crystal resonator, HSICLK and PLL clocks are turned off, SRAM and register data disappear, RTC area and backup register contents remain, and standby circuit still works; The external reset signal on NRST, IWDT reset, rising edge on WKUP pin or RTC event will wake MCU out of standby mode.

4.8 DMA

2 built-in DMAs; DMA1 supports 7 channels and DMA2 supports 5 channels. Each channel supports multiple DMA requests, but only one DMA request is allowed to enter the DMA channel at the same time. The peripherals supporting DMA requests are ADC, SPI, USART, I2C, and TMRx. Four levels of DMA channel priority can be configured. Data transmission of "Memory → Memory, Memory → Peripheral, Peripheral → Memory" can be supported (memory includes Flash and SRAM).

4.9 GPIO

GPIO can be configured as general input, general output, multiplexing function and analog input and output. The general input can be configured as floating input, pull-up input and pull-down input; the general output can be configured as push-pull output and open-drain output; the multiplexing function can be used for digital peripherals; and the analog input and output can be used for analog peripherals and low-power mode; the enable and disable pull-up/pull-down resistor can be configured; the speed of 2MHz, 10MHz and 50MHz can be configured; the higher the speed is, the greater the power and the noise will be.

4.10 Communication peripherals

4.10.1 USART

Up to 8 general-purpose synchronous/asynchronous transmitter receivers are embedded in the chip, and the communication rate can support 6Mbit/s at most. All USART interfaces can be provided by DMA controller. The functions of USART interfaces are shown in the following table.

Table 14 USART Function Differences

USART mode/function	USART1/2/3	USART4	USART5/6/7/8
Hardware flow control of modem	√	√	-
Multi-buffer communication (DMA)	√	√	√
Multi-processor communication	√	√	√
Synchronous mode	√	√	√
Half duplex (single-line mode)	√	√	√
Smart card mode	√	-	-
IrDASIR codec module	√	-	-
LIN mode	√	-	-
Dual clock domain and wake-up from stop mode	√	-	-
Receiver timeout interrupt	√	-	-
Modbus communication	√	-	-
Automatic baud rate detection	√	-	-

USART mode/function	USART1/2/3	USART4	USART5/6/7/8
Drive enable	√	√	√

Note: √ = support.

4.10.2 I2C

I2C1/2 can work in master mode and slave mode, and supports 7-bit and 10-bit addressing modes. I2C1/2 supports standard mode (up to 100kbit/s) or fast mode (up to 400kbit/s). In addition, I2C1 has built-in programmable analog and digital noise filters, and also supports ultra-fast mode (up to 1 Mbit/s).

In addition, I2C1 also provides hardware support for SMBus 2.0 and PMBus 1.1: ARP function, master notification protocol, hardware CRC(PEC) generation/verification, timeout verification and alarm protocol management.

I2C supports DMA function.

4.10.3 SPI/I2S

2 built-in SPIs, support full duplex and half duplex communication in master mode and slave mode, can use DMA controller, and can configure 4~16 bits per frame, and communicate at a rate of up to 18Mbit/s.

2 built-in I2S (multiplexed with SPI), support half duplex communication in master mode and slave mode, support synchronous transmission, and can be configured with 16-bit, 24-bit and 32-bit data transfer with 16-bit or 32-bit resolution. The configurable range of audio sampling rate is 8kHz~48kHz; when one or two I2S interfaces are configured as the master mode, the master clock can be output to external DAC or decoder (CODEC) at 256 times of sampling frequency.

4.10.4 CAN

A built-in CAN, conforming to CAN2.0A and CAN2.0B (active) specifications, the highest bit rate supporting 1Mbit/s, sending and receiving frame format supporting standard frame grid with 11-bit identifier and extended frame with 29-bit identifier, and allocating 256Bytes dedicated SRAM for sending and receiving data.

4.11 Analog peripherals

4.11.1 ADC

1 built-in ADC with 12-bit accuracy, up to 16 external channels and 3 internal channels for each ADC. The internal channels measure the temperature sensor voltage, reference voltage and V_{BAT} voltage respectively. It can be configured with the resolution, the sampling time is programmable, and it support self-calibration. The startup mode supports software trigger and hardware trigger. The conversion mode supports single conversion, continuous conversion and intermittent conversion, and the conversion channel selection supports single channel conversion and scanning conversion of a certain sequence of channels. It supports analog

watchdog and DMA.

4.11.1.1 Temperature sensor

A temperature sensor is built in, which is internally connected with ADC_IN16 channel. The voltage generated by the sensor changes linearly with temperature, and the converted voltage value can be obtained by ADC and converted into temperature.

4.11.1.2 Internal reference voltage

Built-in reference voltage V_{REFINT}, internally connected to ADC_IN17 channel, which can be obtained through ADC; V_{REFINT} provides stable voltage output for ADC.

4.11.1.3 V_{BAT} Monitor

The built-in V_{BAT} monitor is internally connected to a 2-divider bridge, and $V_{BAT}/2$ is connected to ADC_IN18 channel, and can be obtained through ADC.

4.11.2 DAC

Two built-in 12-bit DACs, and each corresponding to an output channel, which can be configured in 8-bit and 12-bit modes, and the DMA function is supported. The waveform generation supports noise wave and triangle wave. The conversion mode supports independent or simultaneous conversion and the trigger mode supports external signal trigger and internal timer update trigger.

4.11.3 Comparator

Two built-in fast rail-to-rail comparators, the internal/external reference voltage, hysteresis, speed and support are programmable, and the output polarity support is configurable. The reference voltage can be selected from external I/O, DAC output pin, internal reference voltage (V_{REFINT}), and 1/4 or 1/2 or 3/4 of the internal reference voltage, which can generate interrupts, and support MCU entering sleep and stop modes by external interrupts.

4.11.4 Touch sensing controller

Built-in touch sensing controller can detect the change of capacitance, which can be applied to touch keys. When a finger touches a key, capacitance will be introduced, which will cause the capacitance change, so as to judge whether there is an eye-catching key. The touch sensing is compatible with slider, touch key, linear and rotary.

Up to 24 GPIOs support capacitance sensor function, which are divided into 6 groups. In practical application, each sampling capacitor occupies one GPIO port, so up to 18 capacitance sensor channels are supported. See the table below for specific pin distribution.

Table 15 Applicable Pin Distribution of Touch Sensors

Group No.	Capacitance Sensor Signal Name	Pin name
G1	TSC_G1_IO1	PA0
G1	TSC_G1_IO2	PA1
G1	TSC_G1_IO3	PA2

Group No.	Capacitance Sensor Signal Name	Pin name
G1	TSC_G1_IO4	PA3
—		
G2	TSC_G2_IO1	PA4
G2	TSC_G2_IO2	PA5
G2	TSC_G2_IO3	PA6
G2	TSC_G2_IO4	PA7
—		
G3	TSC_G3_IO1	PC5
G3	TSC_G3_IO2	PB0
G3	TSC_G3_IO3	PB1
G3	TSC_G3_IO4	PB2
—		
G4	TSC_G4_IO1	PA9
G4	TSC_G4_IO2	PA10
G4	TSC_G4_IO3	PA11
G4	TSC_G4_IO4	PA12
—		
G5	TSC_G5_IO1	PB3
G5	TSC_G5_IO2	PB4
G5	TSC_G4_IO3	PB6
G5	TSC_G4_IO4	PB7
—		
G6	TSC_G6_IO1	PB11
G6	TSC_G6_IO2	PB12
G6	TSC_G6_IO3	PB13
G6	TSC_G6_IO4	PB14

Table 16 Number of Touch Sensor Channels Supported in Practical Application

Group No.	Number of Channels for Each Group of Capacitance Sensors
G1	3
G2	3
G3	3

Group No.	Number of Channels for Each Group of Capacitance Sensors
G4	3
G5	3
G6	3
Total Number of Capacitance Sensor Channels	18

4.12 Timer

A built-in 16-bit advanced timer (TMR1), 6 general-purpose timers (TMR2/3/14/15/16/17), two basic timers (TMR6/7), an independent watchdog timer, a window watchdog timer and a system tick timer.

Watchdog timer can be used to detect whether the program is running normally.

The system tick timer is the peripheral of the core with automatic reloading function. When the counter is 0, it can generate a maskable system interrupt, which can be used for real-time operating system and general delay.

Table 17 Function Comparison between Advanced/General-purpose/Basic and System Tick Timers

Timer type	**System tick timer**	**Basic timer**		**General-purpose timer**						**Advanced timer**
Timer name	Sys Tick Timer	TMR6	TMR7	TMR2	TMR3	TMR14	TMR15	TMR16	TMR17	TMR1
Counter resolution	24 bits	16 bits		32 bits	16 bits					16 bits
Counter type	Down	Up		Up, down, up/down						Up, down, up/down
Prescaler factor	-	Any integer between 1 and 65536		Any integer between 1 and 65536						Any integer between 1 and 65536
General DMA request	-	OK		OK	Not OK	OK	OK	OK		OK
Capture/Comparison channel	-	-		4	1	2	1	1		4
Complementary outputs	-	No		No	No	Yes	Yes	Yes		Yes
Function Instruction	Special for real-time operating system	Used to generate DAC trigger signals.		Synchronization or event chaining function provided Timers in debug mode can be frozen.						It has complementary PWM output with dead band insertion

Timer type	System tick timer	Basic timer	General-purpose timer	Advanced timer
	Automatic reloading function supported When the counter is 0, it can generate a maskable system interrupt Can program the clock source	Can be used as a 16-bit general-purpose timebase counter.	Can be used to generate PWM output Except TMR14, each timer has independent DMA request mechanism. It can handle incremental encoder signals	When configured as a 16-bit standard timer, it has the same function as the TMRx timer. When configured as a 16-bit PWM generator, it has full modulation capability (0~100%). In debug mode, the timer can be frozen, and PWM output is disabled. Synchronization or event chaining function provided.

Table 18 Independent Watchdog and Window Watchdog Timers

Name	Counter resolution	Counter type	Prescaler factor	Functional Description
Independent watchdog	12-bit	Down	Any integer between 1 and 256	The clock is provided by an internally independent RC oscillator of 40KHz, which is independent of the master clock, so it can run in stop and standby modes. The whole system can be reset in case of problems. It can provide timeout management for applications as a free-running timer. It can be configured as a software or hardware startup watchdog through option bytes. Timers in debug mode can be frozen.
Window watchdog	7-bit	Down	-	Can be set for free running. The whole system can be reset in case of problems. Driven by the master clock, it has early interrupt warning function; Timers in debug mode can be frozen.

4.13 RTC

A built-in RTC with LSECLK signal input pins (OSC32_IN, OSC32_OUT), three TAMP input signal detection pins (RTC_TAMP1/2/3), one reference clock input signal (RTC_REFIN), one output timestamp event output pin (RTC_TS), and one signal output pin RTC_OUT (it can be configured as calibration signal output or alarm clock signal output).

The external crystal oscillator, resonator or oscillator, LSICLK and HSECLK/32 with external frequency of 32.768kHz can be selected as the clock source.

With calendar function, it can display sub-seconds, seconds, minutes, hours (12 or 24 hours format), weeks, dates, months and years. It supports alarm clock function, and can output the alarm clock signal for external use, and wake up from low power consumption mode. It can receive signals to wake up from low power consumption mode. In terms of accuracy, it supports daylight saving time compensation, month angel compensation and leap year days compensation. In terms of precision, the error caused by crystal oscillator can be repaired by RTC digital calibration function, and the accuracy of calendar can be improved by using a more accurate second source clock (50 or 60Hz).

4.14 CRC

A CRC (cyclic redundancy check) calculation unit is built in, which can generate CRC codes and operate 8-bit, 16-bit and 32-bit data.

5 Electrical characteristics

5.1 Test conditions of electrical characteristics

5.1.1 Maximum and minimum values

Unless otherwise specified, all products are tested on the production line at T_A=25℃. Its maximum and minimum values can support the worst environmental temperature, power supply voltage and clock frequency.

In the notes at the bottom of each table, it is stated that the data are obtained through comprehensive evaluation, design simulation or process characteristics and are not tested on the production line; on the basis of comprehensive evaluation, after passing the sample test, take the average value and add and subtract three times the standard deviation (average ±3∑) to get the maximum and minimum values.

5.1.2 Typical values

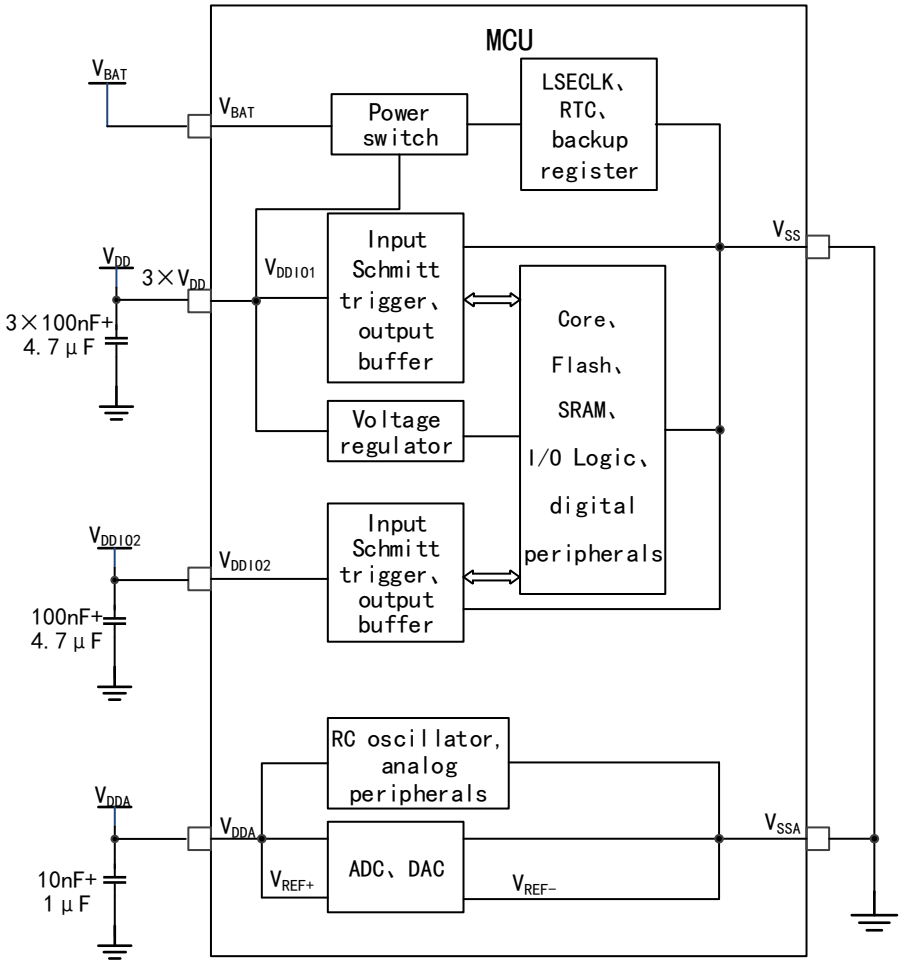
Unless otherwise specified, typical data are measured based on T_A=25℃, V_{DD}=V_{DDA}=3.3V. These data are only used for design guidance.

5.1.3 Typical curve

Unless otherwise specified, typical curves will only be used for design guidance and will not be tested.

5.1.4 Power supply scheme

Figure 4 Power Supply Scheme



5.1.5 Load capacitance

Figure 5 Load conditions when measuring pin parameters

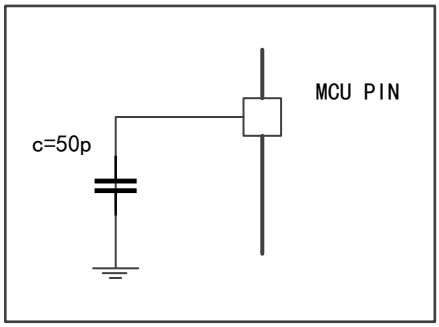


Figure 6 Pin Input Voltage Measurement Scheme

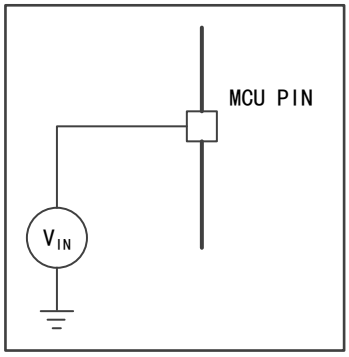
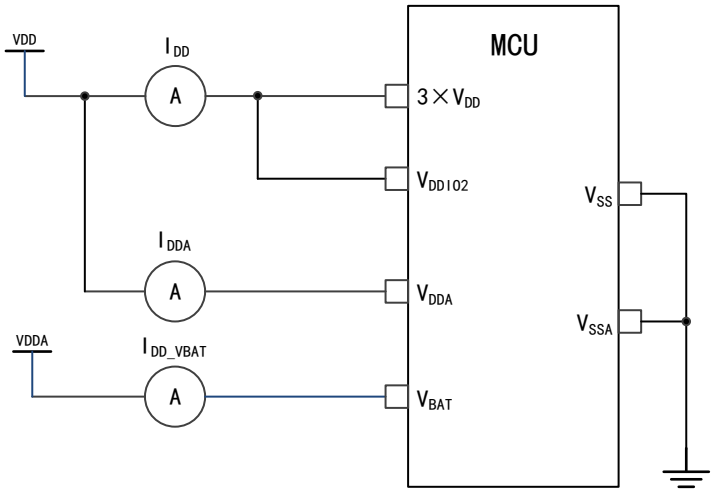


Figure 7 Power Consumption Measurement Scheme



5.2 Test under general operating conditions

Table 19 General Operating Conditions

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
f_{HCLK}	Internal AHB clock frequency	-	-	48	MHz
f_{PCLK}	Internal APB clock frequency	-	-	48	
V_{DD}	Main power supply voltage	-	2	3.6	V
V_{DDIO2}	IO supply voltage	Only V_{DD} exists to supply power	1.65	3.6	V
V_{DDA}	Analog power supply voltage (When neither ADC nor DAC is used)	Must be the same as V_{DD}	V_{DD}	3.6	V
	Analog power supply voltage (When ADC and DAC are used)		2.4	3.6	
V_{BAT}	Power supply voltage of backup domain	-	1.65	3.6	V
T_A	Ambient temperature (temperature number 7)	Maximum power dissipation	-40	105	℃

5.3 Absolute maximum ratings

If the load on the device exceeds the absolute maximum rating, it may cause permanent damage to the device. Here, only the maximum load that can be borne is given, and there is no guarantee that the device functions normally under this condition.

5.3.1 Maximum temperature characteristics

Table 20 Temperature Characteristics

Symbol	Description	Numerical Value	Unit
T_{STG}	Storage temperature range	-55 ~ +150	℃
T_J	Maximum junction temperature	150	℃

5.3.2 Maximum rated voltage characteristics

All power supply (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the power supply within the external limited range.

Table 21 Maximum Rated Voltage Characteristics

Symbol	Description	Minimum value	Maximum value	Unit
V_{DD} - V_{SS}	External main power supply voltage	-0.3	4.0	V
V_{DDA}-V_{SSA}	External analog power supply voltage	-0.3	4.0	
V_{BAT}-V_{SS}	Power supply voltage of external backup domain	-0.3	4.0	
V_{DD}-V_{DDA}	Voltage difference allowed by V_{DD}>V_{DDA}	-	0.3	
V_{IN}	Input voltage on FT pins	V_{SS}-0.3	5.5	
	Input voltage on other pins	V_{SS}-0.3	V_{DD} + 0.3	
| ΔV_{DDx} |	Voltage difference between different power supply pins	-	50	mV
| V_{SSx}-V_{SS} |	Voltage difference between different grounding pins	-	50	

5.3.3 Maximum Rated Current Characteristics

Table 22 Maximum Rated Current Characteristics

Symbol	Description	Maximum value	Unit
ΣI_{VDD}	Total current into sum of all V_{DD} power lines (source)(1)	120	mA
ΣI_{VSS}	Total current out of sum of all V_{SS} ground lines (sink)(1)	-120	
$I_{DD\ (PIN)}$	Maximum current into each V_{DD} power pin (source)(1)	100	
$I_{SS\ (PIN)}$	Maximum current out of each V_{SS} ground pin (sink)(1)	-100	
$I_{IO\ (PIN)}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	-25	
$\Sigma I_{IO\ (PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	80	
	Total output current sourced by sum of all I/Os and control pins(2)	-80	
	Total output current sourced by sum of all I/Os supplied by V_{DDIO2}	-40	

Symbol	Description	Maximum value	Unit
$I_{INJ(PIN)}$ (3)	Injected current on B, 5T and 5Tf pins	-5/+0 (4)	
	Injected current on STD and RST pin	±5	
	Injected current on STDA pins(5)	±5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(6)	±25	

（1） All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

（2） This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.

（3） A positive injection is induced by $V_{IN} > V_{DDIOx}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded.

（4） Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.

（5） On these I/Os, a positive injection is induced by $V_{IN} > V_{DDA}$. Negative injection disturbs the analog performance of the device.

（6） When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

5.3.4 ESD characteristics

Table 23 ESD Characteristics

Symbol	Parameter	Conditions	Maximum value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A=18~24 ℃, conforming to AEC-Q100-002	±2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging device model)	T_A=18~24 ℃, conforming to AEC-Q100-011	±750	

Note: The samples are measured by a third-party testing organization and are not tested in production.

5.3.5 Static latch-up

Table 24 Static Latch-up

Symbol	Parameter	Conditions	Type
LU	Class of static latch-up	T_A = +105℃, conforming to AEC-Q100-004	Class II-A

Note: The samples are measured by a third-party testing organization and are not tested in production.

5.4 On-chip memory

5.4.1 Flash characteristics

Table 25 Flash Memory Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
tprog	16-bit programming time	TA = -40~105℃ VDD=2.4~3.6V	-	48	-	μs
tERASE	Page (2KBytes) erase time	TA = -40~105℃ VDD=2.4~3.6V	-	3	-	ms
tME	Whole erase time	TA = 25℃ VDD=3.3V	-	12	-	ms
Vprog	Programming voltage	TA = -40~105℃	2	-	3.6	V

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.5 Clock

5.4.1 Characteristics of external clock source

High-speed external clock generated by crystal resonator

For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer.

Table 26 HSECLK4~32MHz Oscillator Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R_F	Feedback resistance	-	-	300	-	kΩ
$I_{DD(HSECLK)}$	HSECLK current consumption	V_{DD}=3.3V, C_L=10pF@8MHz	-	0.29	-	mA
$t_{SU(HSECLK)}$	Startup time	V_{DD} is stable	-	2	-	ms

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Low-speed external clock generated by crystal resonator

For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer.

Table 27 LSECLK Oscillator Characteristics (f_{LSECLK}=32.768KHz)

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
f_{OSF_IN}	Oscillator frequency	-	-	32.768	-	KHz
$t_{SU(LSECLK)(1)}$	Startup time	V_{DDIOx} is stable	-	2	-	s
$I_{DD(LSECLK)}$	LSECLK current consumption	-	-	0.9	-	μA

Note: It is obtained from a comprehensive evaluation and is not tested in production.

（1） $t_{SU(LSECLK)}$ is the startup time, which is measured from the time when LSECLK is enabled by software to the time when stable oscillation at 32.768KHz is obtained. This value is measured using a standard crystal resonator, which may vary greatly due to different crystal manufacturers.

5.5.2 Characteristics of internal clock source

High speed internal (HSICLK) RC oscillator

Table 28 HSICLK Oscillator Characteristics

Symbol	Parameter	Conditions		Minimum value	Typical values	Maximum value	Unit
f_{HSICLK}	Frequency	-		-	8	-	MHz
Acc_{HSICLK}	Accuracy of HSICLK oscillator	Factory calibration	V_{DD}=3.3V，T_A=25℃(1)	-1	-	1	%
			V_{DD}=2-3.6V，T_A=-40~105℃	-3	-	3	%
$t_{SU(HSICLK)}$	Startup time of HSICLK oscillator	V_{DD}=3.3V，T_A=-40~105℃		1	-	5	μs
$I_{DDA(HSICLK)}$	Power consumption of HSICLK oscillator	-		-	80	100	μA

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Table 29 HSICLK14 Oscillator Characteristics

Symbol	Parameter	Conditions		Minimum value	Typical values	Maximum value	Unit
$f_{HSICLK14}$	Frequency	-		-	14	-	MHz
$Acc_{HSICLK14}$	Accuracy of HSICLK14 oscillator	Factory calibration	V_{DD}=3.3V，T_A=25℃(1)	-1	-	1	%
			V_{DD}=2-3.6V，T_A=-40~105℃	-3	-	3	%
$t_{SU(HSICLK14)}$	Startup time of HSICLK14 oscillator	V_{DD}=3.3V T_A=-40~105℃		1	-	2	μs
$I_{DDA(HSICLK14)}$	Power consumption of HSICLK14 oscillator	-		-	100	150	μA

Note: (1) Except for calibration in production, other data are obtained from a comprehensive evaluation and is not tested in production.

Table 30 HSICLK48 Oscillator Characteristics

Symbol	Parameter	Conditions		Minimum value	Typical values	Maximum value	Unit
$f_{HSICLK48}$	Frequency	-		-	48	-	MHz
$A_{CC(HSICLK48)}$	Accuracy of HSICLK48 oscillator	Factory calibration	V_{DD}=3.3V，T_A=25℃(1)	-3	-	3	%
			V_{DD}=2-3.6V，T_A=-40~105℃	-5	-	5	%
$t_{SU(HSICLK48)}$	Startup time of HSICLK48 oscillator	V_{DD}=3.3V，T_A=-40~105℃		-	-	6.2	μs
$I_{DDA(HSICLK48)}$	Power consumption of HSICLK48 oscillator	-		-	312	330	μA

Note: (1) Except for calibration in production, other data are obtained from a comprehensive evaluation and is not tested in production.

Low speed internal (LSICLK) RC oscillator

Table 31 LSICLK Oscillator Characteristics

Symbol	Parameter	Minimum value	Typical values	Maximum value	Unit
f_{LSICLK}	Frequency (V_{DD} =2-3.6V, T_A =-40~105℃)	40.12	40	46.10	KHz
$t_{SU(LSICLK)}$	LSICLK oscillator startup time, (V_{DD}=3.3V, T_A=-40~105℃)	-	-	79.2	μs
$I_{DD(LSICLK)}$	Power consumption of LSICLK oscillator	-	0.5	-	μA

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.5.3 PLL Characteristics

Table 32 PLL Characteristics

Symbol	Parameter	Numerical Value			Unit
		Minimum value	Typical values	Maximum value	
f_{PLL_IN}	PLL input clock	1	8.0	24	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL frequency doubling output clock, (V_{DD}=3.3V, T_A=-40~105℃)	16	-	48	MHz
t_{LOCK}	PLL phase locking time	-	-	200	μs

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.6 Reset and power management

5.6.1 Test of Embedded Reset and Power Control Block Characteristics

Table 33 Embedded Reset and Power Control Block Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
$V_{POR/PDR}$	Power-on/power-down reset threshold	Falling edge	1.89	1.92	1.95	V
		Rising edge	1.92	1.95	1.98	V
$V_{PDRhyst}$	PDR hysteresis	-	20.00	30.00	40.00	mV
$T_{RSTTEMPO}$	Reset duration	-	1.10	1.29	1.52	ms

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Table 34 Programmable Power Supply Voltage Detector Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
V_{PVD}	Programmable power supply voltage detector voltage level selection	PLS[2:0]=000 (rising edge)	2.18	2.20	2.22	V
		PLS[2:0]=000 (falling edge)	2.08	2.09	2.11	V
		PLS[2:0]=001 (rising edge)	2.29	2.30	2.32	V
		PLS[2:0]=001 (falling edge)	2.18	2.19	2.21	V
		PLS[2:0]=010 (rising edge)	2.39	2.40	2.42	V
		PLS[2:0]=010 (falling edge)	2.28	2.29	2.31	V
		PLS[2:0]=011 (rising edge)	2.48	2.49	2.52	V
		PLS[2:0]=011 (falling edge)	2.38	2.39	2.41	V
		PLS[2:0]=100 (rising edge)	2.58	2.60	2.62	V
		PLS[2:0]=100 (falling edge)	2.47	2.48	2.51	V
		PLS[2:0]=101 (rising edge)	2.68	2.69	2.72	V
		PLS[2:0]=101 (falling edge)	2.57	2.59	2.61	V
		PLS[2:0]=110 (rising edge)	2.78	2.79	2.82	V
		PLS[2:0]=110 (falling edge)	2.67	2.68	2.71	V
		PLS[2:0]=111 (rising edge)	2.87	2.88	2.91	V
		PLS[2:0]=111 (falling edge)	2.77	2.78	2.81	V
$V_{PVDhyst}$	PVD hysteresis	-	-	107.08	-	mV

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.7 Power consumption

5.7.1 Power consumption test environment

（1） The values are measured by executing Coremark, with the Keil.V5 compilation environment and the L3 compilation optimization level.

（2） All I/O pins are configured as analog inputs and are connected to a static level of V_{DD} or V_{SS} (non-loaded)

（3） Unless otherwise specified, all peripherals are turned off

（4） The relationship between Flash waiting cycle setting and f_{HCLK} :

0~24MHz: 0 waiting cycle

24~48MHz: 1 waiting cycle

（5） The instruction prefetch function is enabled (Note: it must be set before clock setting and bus frequency division)

（6） When the peripherals are enabled: f_{PCLK} =f_{HCLK}

5.7.2 Power consumption in run mode

Table 35 Power Consumption in Run Mode when the Program is Executed in Flash

Parameter	Conditions	fHCLK	Typical value (1)		Maximum value (1)	
			TA=25℃，VDD=3.3V		TA=105℃，VDD=3.6V	
			IDDA(μA)	IDD(mA）	IDDA(μA)	IDD(mA)
Run mode Power consumption	HSECLK bypass (2) , enabling all peripherals	48MHz	103.09	14.51	116.07	15.11
		32MHz	71.88	10.05	83.44	10.50
		24MHz	58.02	7.93	69.07	8.44
		8MHz	2.17	3.17	7.35	3.64
		1MHz	2.17	1.94	7.17	2.78
	HSECLK bypass (2) , turning off all peripherals	48MHz	103.07	8.99	116.02	9.30
		32MHz	71.85	6.23	83.42	6.58
		24MHz	58.04	5.07	69.02	5.56
		8MHz	2.17	2.25	7.28	2.65
		1MHz	2.17	1.82	7.23	2.68
	HSICLK48, enabling all peripherals	48MHz	312.19	14.33	320.91	15.06
	HSICLK48, turning off all peripherals	48MHz	312.23	8.82	320.96	9.21
	HSICLK (2) , enabling all peripherals	48MHz	165.36	14.52	182.74	14.78
		32MHz	134.37	9.97	150.34	10.28
		24MHz	120.54	7.87	135.75	8.13
		8MHz	64.98	3.12	76.50	3.36
	HSICLK (2) , turning off all peripherals	48MHz	165.40	8.89	182.68	9.01
		32MHz	134.36	6.18	150.14	6.44
		24MHz	120.55	5.00	135.79	5.25
		8MHz	64.99	2.16	76.34	2.44

Note: (1) It is obtained from a comprehensive evaluation and is not tested in production.

(2) The external clock is 8MHz, and when f_{HCLK}>8MHz, turn on PLL, otherwise, turn off PLL.

Table 36 Power Consumption in Run Mode when the Program is Executed in RAM

Parameter	Conditions	fHCLK	Typical value (1)		Maximum value (1)	
			TA=25℃，VDD=3.3V		TA=105℃，VDD=3.6V	
			IDDA(μA)	IDD(mA）	IDDA(μA)	IDD(mA)
Run mode Power consumption	HSECLK bypass (2) , enabling all peripherals	48MHz	103.16	12.36	12.51	12.82
		32MHz	71.93	8.52	8.77	8.74
		24MHz	58.01	6.62	6.75	6.91
		8MHz	2.17	2.70	2.89	2.93
		1MHz	2.17	0.98	1.14	1.18
	HSECLK bypass (2) , turning off all peripherals	48MHz	102.49	6.75	7.07	6.97
		32MHz	71.34	4.79	5.08	4.98
		24MHz	57.36	3.72	3.99	4.01
		8MHz	2.33	1.77	1.99	1.96
		1MHz	2.33	086	1.07	1.07
	HSICLK48, enabling all peripherals	48MHz	312.48	12.20	320.95	12.67
	HSICLK48, turning off all peripherals	48MHz	312.50	6.65	320.91	7.01
	HSICLK (2) , enabling all peripherals	48MHz	165.37	12.37	12.82	12.86
		32MHz	134.37	8.57	8.93	8.90
		24MHz	120.52	6.66	6.96	6.84
		8MHz	64.98	2.77	3.00	3.04
	HSICLK (2) , turning off all peripherals	48MHz	164.62	6.74	7.05	7.03
		32MHz	134.35	4.81	5.05	4.99
		24MHz	120.50	3.76	4.03	4.05
		8MHz	64.35	1.84	2.02	2.01

Note: (1) It is obtained from a comprehensive evaluation and is not tested in production.

(2) The external clock is 8MHz, and when f_{HCLK}>8MHz, turn on PLL, otherwise, turn off PLL.

5.7.3 Power consumption in sleep mode

Table37 Power Consumption in Sleep Mode when the Program is Executed in RAM or Flash

Parameter	Conditions	f_{HCLK}	Typical value (1)		Maximum value (1)	
			T_A=25℃，V_{DD}=3.3V		T_A=105℃，V_{DD}=3.6V	
			I_{DDA}(μA)	I_{DD}(mA）	I_{DDA}(μA)	I_{DD}(mA)
Sleep mode Power consumption	HSECLK bypass (2) , enabling all peripherals	48MHz	103.14	9.31	116.13	9.7
		32MHz	71.93	6.52	83.37	6.96
		24MHz	58.00	5.09	69.03	5.59
		8MHz	2.17	2.25	7.23	2.65
		1MHz	2.17	1.82	7.22	1.12
	HSECLK bypass (2) , turning off all peripherals	48MHz	103.13	2.39	115.96	2.79
		32MHz	71.89	1.90	83.17	2.33
		24MHz	57.99	1.65	68.91	2.09
		8MHz	2.17	1.10	7.13	1.53
		1MHz	2.16	0.72	7.12	0.97
	HSICLK48, enabling all peripherals	48MHz	312.24	13.76	320.79	9.49

Parameter	Conditions	f_{HCLK}	Typical value (1)		Maximum value (1)	
			T_A=25℃，V_{DD}=3.3V		T_A=105℃，V_{DD}=3.6V	
			I_{DDA}(μA)	I_{DD}(mA)	I_{DDA}(μA)	I_{DD}(mA)
	HSICLK48, turning off all peripherals	48MHz	312.24	2.26	320.68	2.56
	HSICLK (2) , enabling all peripherals	48MHz	165.34	9.25	182.73	9.59
		32MHz	134.36	6.47	150.16	6.77
		24MHz	120.50	5.03	135.52	5.33
		8MHz	64.98	2.21	75.37	2.48
	HSICLK (2) , turning off all peripherals	48MHz	165.34	2.29	182.58	2.56
		32MHz	134.39	1.80	150.09	2.08
		24MHz	120.51	1.55	135.39	1.82
		8MHz	64.99	1.02	75.68	1.29

Note:

(1) It is obtained from a comprehensive evaluation and is not tested in production.

(2) The external clock is 8MHz, and when f_{HCLK}>8MHz, turn on PLL, otherwise, turn off PLL

5.7.4 Power consumption in stop mode and standby mode

Table 38 Power Consumption in Stop Mode and Standby Mode

Parameter	Conditions		Typical value (1), (T_A=25℃)						Maximum value (1), (V_{DD}=3.6V)				Unit
			V_{DD}=2.0V		V_{DD}=3.3V		V_{DD}=3.6V		T_A=85℃		T_A=105℃		
			I_{DDA}	I_{DD}	I_{DDA}	I_{DD}	I_{DDA}	I_{DD}	I_{DDA}	I_{DD}	I_{DDA}	I_{DD}	
Power consumption in stop mode	V_{DDA} Monitor ON	Regulator in run mode, all oscillators OFF	2.55	22.78	3.03	23.43	3.25	23.96	4.84	79.63	7.57	165.32	μA
		Regulator in low-power mode, all oscillators OFF	2.50	8.53	3.02	9.24	3.25	9.73	4.80	61.51	7.54	142.50	
Power consumption in standby mode		LSICLK and IWDT ON	2.70	1.72	3.40	2.62	3.70	3.18	5.21	7.18	7.65	14.37	
		LSICLK and IWDT OFF	2.37	1.43	2.90	2.25	3.13	2.69	4.66	6.66	7.11	13.88	
Power consumption in stop mode	V_{DDA} Monitor OFF	Regulator in run mode, all oscillators OFF	1.35	22.73	1.53	23.62	1.64	24.05	3.16	79.76	5.95	165.3	
		Regulator in low-power mode, all oscillators OFF	1.35	8.50	1.52	9.35	1.63	9.77	3.14	61.66	5.88	143.7	
Power consumption in standby mode		LSICLK and IWDT ON	1.55	1.71	1.90	2.75	2.06	3.23	3.54	7.23	6.01	14.46	
		LSICLK and IWDT OFF	1.22	1.42	1.40	23.00	1.51	2.74	2.99	6.74	5.46	13.89	

Note: (1) It is obtained from a comprehensive evaluation and is not tested in production.

5.7.5 Backup Domain Power Consumption

Table 39 Backup Domain Power Consumption

Symbol	Conditions	Typical value (1), T_A=25℃			Maximum value (1), V_{BAT}=3.6V			Unit
		V_{BAT}=1.8V	V_{BAT}=2.4V	V_{BAT}=3.3V	T_A=25℃	T_A=85℃	T_A=105℃	
I_{DD_VBAT}	The low-speed oscillator and RTC are in ON state	0.79	0.97	1.21	2.78	2.6	4.2	μA

Note: (1) It is obtained from a comprehensive evaluation and is not tested in production.

5.7.6 Peripheral power consumption

The HSECLK Bypass 1M is adopted as clock source, f_{PCLK}=f_{HCLK}

=1M.

Peripheral power consumption = current that enables the peripheral clock-current that disables the peripheral clock.

Table 40 Peripheral Power Consumption

Parameter	Peripheral	Typical value (1) T_A =25℃, V_{DD} =3.3V	Unit
Peripheral power consumption	BusMatrix	1.12	μA/MHz
	CRC	0.70	
	DMA	2.25	
	FLASH	23.75	
	GPIOA	2.25	
	GPIOB	2.12	
	GPIOC	0.87	
	GPIOD	0.79	
	GPIOE	1.08	
	GPIOF	0.71	
	SRAM	0.25	
	TSC	2.04	
	ALL_AHB	41.04	
	APB_Bridge	1.00	
	ADC	3.00	
	CAN	6.62	
	DAC	2.46	
	DBGMCU	0.25	
	I2C1	7.54	
	I2C2	1.87	
	PMU	0.91	
	SPI1	4.91	
	SPI2	4.5	
	SYSCFG	1.08	

Parameter	Peripheral	Typical value (1) T_A =25℃, V_{DD} =3.3V	Unit
	TMR1	6.95	
	TMR2	7.17	
	TMR3	5.20	
	TMR6	1.41	
	TMR7	1.33	
	TMR14	2.70	
	TMR15	4.20	
	TMR16	3.20	
	TMR17	3.58	
	USART1	9.08	
	USART2	9.10	
	USART3	9.04	
	USART4	3.2	
	USART5	3.08	
	USART6	2.83	
	USART7	3.00	
	USART8	2.95	
	USBD	48.58	
	WWDT	0.83	
	ALL_APB	114.62	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.8 Wake-up time in low power mode

The measurement of wake-up time in low power mode is from the start of wake-up event to the time when the user program reads the first instruction, in which V_{DD}=V_{DDA}.

Table 41 Wake Up Time in Low-power Mode

Symbol	Parameter	Conditions	Typical value (T_A=25℃)			Maximum value	Unit
			2V	3.3V	3.6V		
$t_{WUSLEEP}$	Wake-up from sleep mode	-	0.15	0.15	0.15	0.17	μs
t_{WUSTOP}	Wake up from stop mode	The voltage regulator is in run mode	3..45	3.09	3.02	3.89	
		The voltage regulator is in low power mode	8.15	5.43	5.14	9.72	
$t_{WUSTDBY}$	Wake up from standby mode	-	46.65	37.15	35.93	53.80	

Note: (1) It is obtained from a comprehensive evaluation and is not tested in production.

5.9 Pin characteristics

5.9.1 I/O pin characteristics

Table 42 DC Characteristics (T_A=-40℃-105℃,V_{DD}=2~3.6V)

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
V_{IL}	Low level input voltage	STD and STDA I/O	-	-	$0.3V_{DDIOx}$+0.07	V
		5T and 5Tf I/O	-	-	$0.475V_{DDIOx}$ -0.2	
		I/O pins except Boot0 pin	-	-	$0.3V_{DDIOx}$	
V_{IH}	High level input voltage	STD and STDA I/O	$0.445V_{DDIOx}$ +0.398	-	-	V
		5T and 5Tf I/O	0.5_{VDDIOx} +0.2	-	-	
		I/O pins except Boot0 pin	$0.7V_{DDIOx}$	-	-	
Vhys	Schmitt trigger hysteresis	STD and STDA I/O	-	300	-	mV
		5T and 5Tf I/O	-	300	-	
Ilkg	Input leakage current	STD, 5T and 5Tf I/OTTa in digital mode, VSS≤VIN≤VDDIOx	-	-	+0.1	μA
		STDA in digital mode, V_{DDIOx}≤V_{IN}≤V_{DDA}	-	-	1	
		5T and 5Tf I/O V_{DDIOx}≤V_{IN}≤5V	-	-	10	
RPU	Weak pull-up equivalent resistance	V_{IN}=V_{SS}	22	42	46	kΩ
RPD	Weak pull-down equivalent resistance	V_{IN}=V_{DDIOx}	22	42	46	kΩ

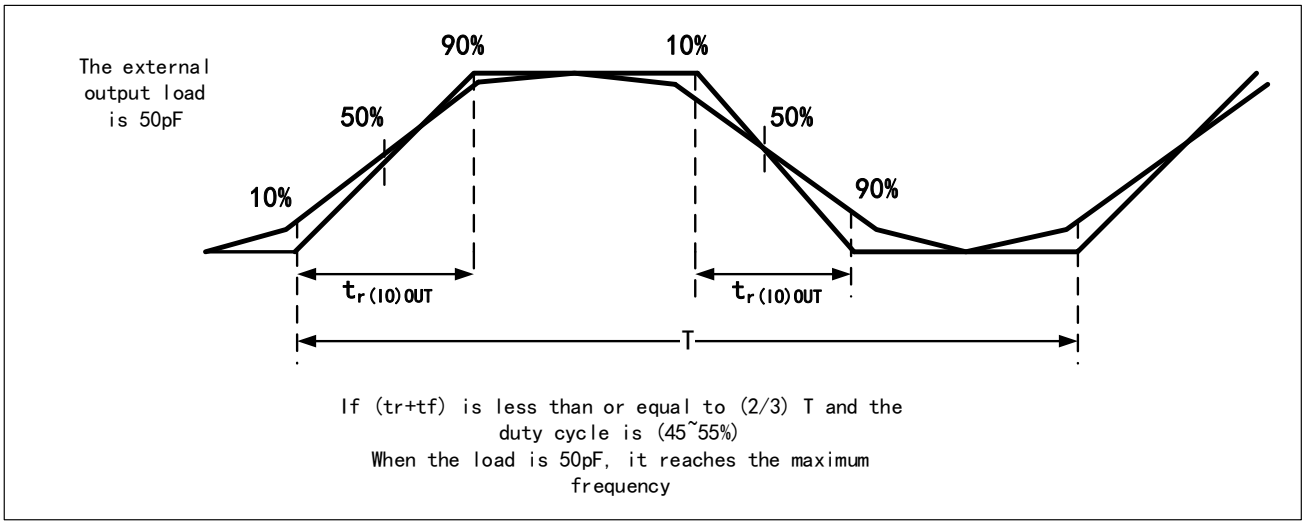
Note: It is obtained from a comprehensive evaluation and is not tested in production.

Table 43 AC Characteristics (TA =25℃)

OSSELy[1:0]	Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
X0(2MHz)	$f_{max(IO)out}$	Maximum frequency	C_L=50pF, V_{DDIOX}=2~3.6V	-	2	MHz
	$t_{f(IO)out}$	Output fall time from high to low level		-	18.16	ns

OSSELy[1:0]	Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
	$t_{r(IO)out}$	Output rise time from low to high level		-	16.66	
01(10MHz)	$f_{max(IO)out}$	Maximum frequency	C_L=50pF, V_{DDIOX}=2~3.6V	-	10	MHz
	tf(IO)out	Output fall time from high to low level		-	11.50	ns
	$t_{r(IO)out}$	Output rise time from low to high level		-	11.14	
10(50MHz)	$f_{max(IO)out}$	Maximum frequency	C_L=30pF, V_{DD}=2.7~3.6V	-	50	MHz
	$t_{f(IO)out}$	Output fall time from high to low level		-	3.58	ns
	$t_{r(IO)out}$	Output rise time from low to high level		-	8.06	
FM+ configuration	$f_{max(IO)out}$	Maximum frequency	C_L=50pF, V_{DDIOx}≥2V	-	2	MHz
	$t_{f(IO)out}$	Output fall time		-	11	ns
	$t_{r(IO)out}$	Output rise time		-	33	
FM+ configuration	$f_{max(IO)out}$	Maximum frequency	C_L=50pF, V_{DDIOx}<2V	-	0.5	MHz
	$t_{f(IO)out}$	Output fall time		-	14	ns
	$t_{r(IO)out}$	Output rise time		-	43	

Figure 8 I/O AC Characteristics Definition



Note: It is obtained from a comprehensive evaluation and is not tested in production.

Table 44 Output Drive Current Characteristics (T_A =25℃)

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
V_{OL}	I/O pin outputs low voltage	|IIO|=8mA, V_{DDIOx}≥2.7V	-	0.4	V
V_{OH}	I/O pin outputs high voltage		V_{DDIOx}-0.4	-	
V_{OL}	I/O pin outputs low voltage	|IIO|=20mA, V_{DDIOx}≥2.7V	-	1.3	
V_{OH}	I/O pin outputs high voltage		V_{DDIOx}-1.3	-	

5.9.2 NRST pin characteristics

The NRST pin input drive adopts CMOS process, which is connected with a permanent pull-up resistor R_{PU}.

Table 45 NRST Pin Characteristics (test condition V_{CC} =3.3V, T_A =-40~105℃)

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
$V_{IL(NRST)}$	NRST low level input voltage	-	1.44	1.75	1.8	V
$V_{IH(NRST)}$	NRST high level input voltage	-	0	1.37	1.38	V
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	-0.38	-	V
R_{PU}	Weak pull-up equivalent resistance	V_{IN} = V_{SS}	25	40	55	kΩ

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.10 Communication peripherals

5.10.1 I2C peripheral characteristics

To achieve maximum frequency of I2C in standard mode, f_{PCLK1} must be greater than 2MHz.
To achieve maximum frequency of I2C in fast mode, f_{PCLK1} must be greater than 4MHz.

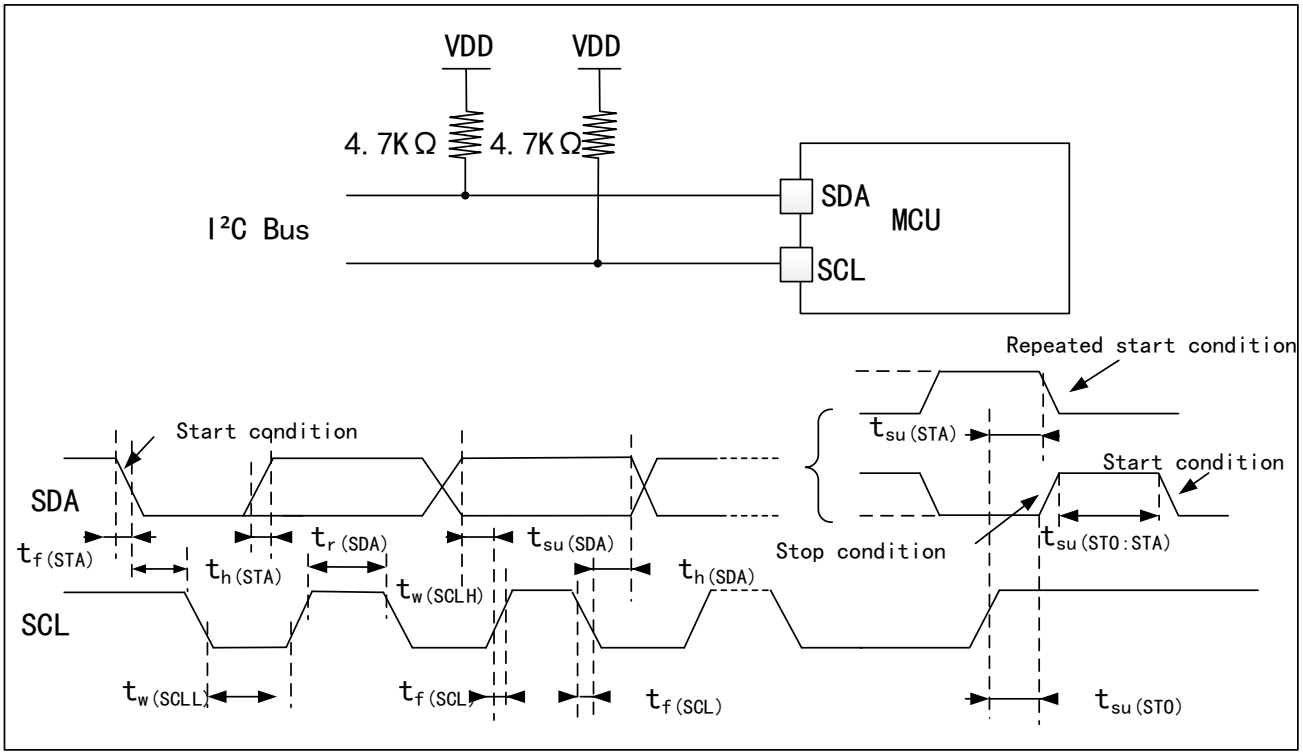
Table 46 I2C Interface Characteristics (T_A=25℃, V_{DD}=3.3V)

Symbol	Parameter	Standard I2C		Fast I2C		Ultra fast I2C		Unit
		Minimum value	Maximum value	Minimum value	Maximum value	Minimum value	Maximum value	
tw(SCLL)	SCL clock low time	4.82	-	1.67	-	0.54	-	μs
tw(SCLH)	SCL clock high time	5.09	-	0.80	-	0.45	-	
tsu(SDA)	SDA setup time	4570	-	1432	-	311.11	-	ns
th(SDA)	SDA data hold time	-	3450	0	156.17	0	150.86	

Symbol	Parameter	Standard I2C		Fast I2C		Ultra fast I2C		Unit
		Minimum value	Maximum value	Minimum value	Maximum value	Minimum value	Maximum value	
tr(SDA)/ tr(SCL)	SDA and SCL rise time	-	310.05	-	301.37	-	314.08	
tf(SDA)/ tf(SCL)	SDA and SCL fall time	-	3.05	-	3.61	-	5.19	
th(STA)	Start condition hold time	5.00	-	0.69	-	0.35	-	μs
tsu(STA)	Repeated start condition setup time	5.19	-	0.91	-	0.56	-	
tsu(STO)	Setup time of stop condition	4.91	-	1.78	-	0.66	-	
tw(STO:STA)	Time from stop condition to start condition (bus idle)	6.46	-	6.31	-	5.80	-	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Figure 9 Bus AC Waveform and Measurement Circuit



Note: The measuring points are set at CMOS levels: 0.3VDD and 0.7VDD .

5.10.2 SPI peripheral characteristics

Table 47 SPI Characteristics (T_A=25℃, V_{DD}=3.3V)

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	10	
$t_{r(SCK)}$ $t_{f(SCK)}$	SI clock rise and fall time	Load capacitance: C = 30pF	-	9.7	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	106.89	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	80.67	-	ns
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Main mode, f_{PCLK} = 36MHz, Prescaler factor=4	54	57	ns
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	17	-	ns
		Slave mode	20.93	-	
$t_{h(MI)}$ $t_{h(SI)}$	Data input hold time	Master mode	32.86	-	ns
		Slave mode	25.11	-	
$t_{a(SO)}$	Data output access time	Slave mode, f_{PCLK} = 20MHz	6.48	8.08	ns
$t_{dis(SO)}$	Data output prohibition time	Slave mode	14.28	-	ns
$t_{v(SO)}$	Effective time of data output	Slave mode (after enable edge)	-	11.89	ns
$t_{v(MO)}$	Effective time of data output	Master mode (after enable edge)	-	5.4	ns
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge)	9.5	-	ns
$t_{h(MO)}$		Master mode (after enable edge)	1.05	-	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Figure 10 SPI Timing Diagram - Slave Mode and CPHA=0

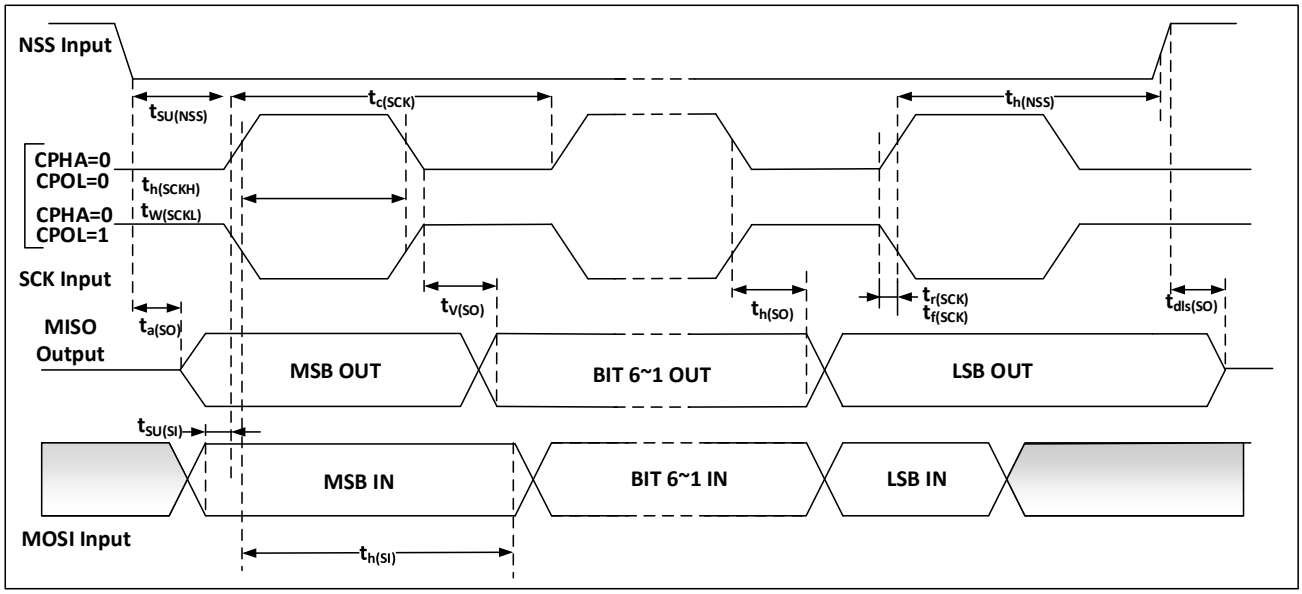
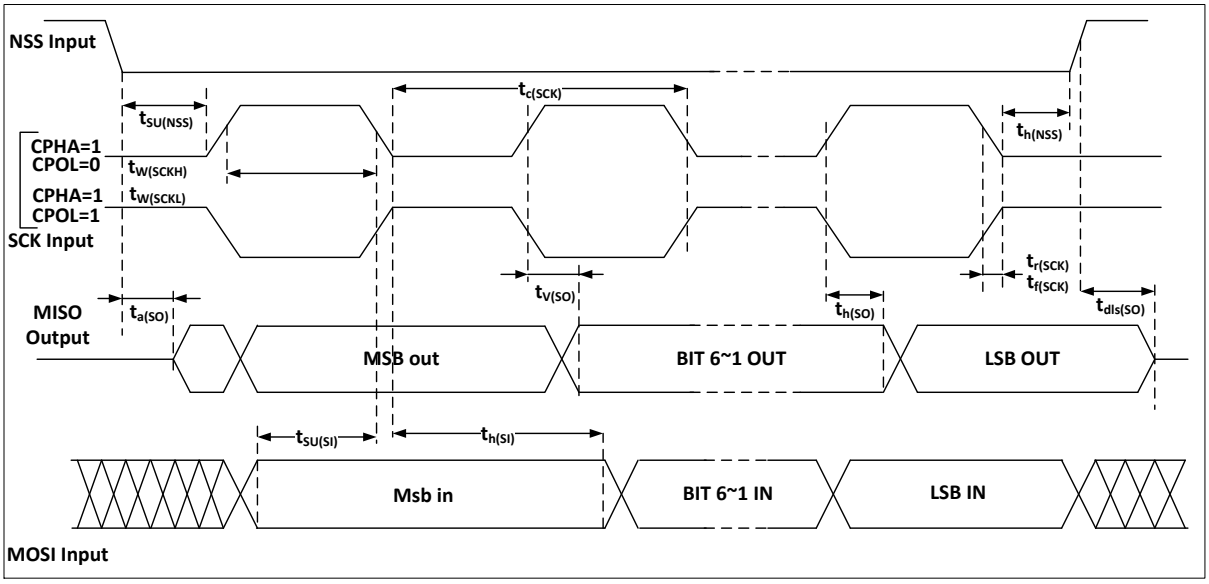
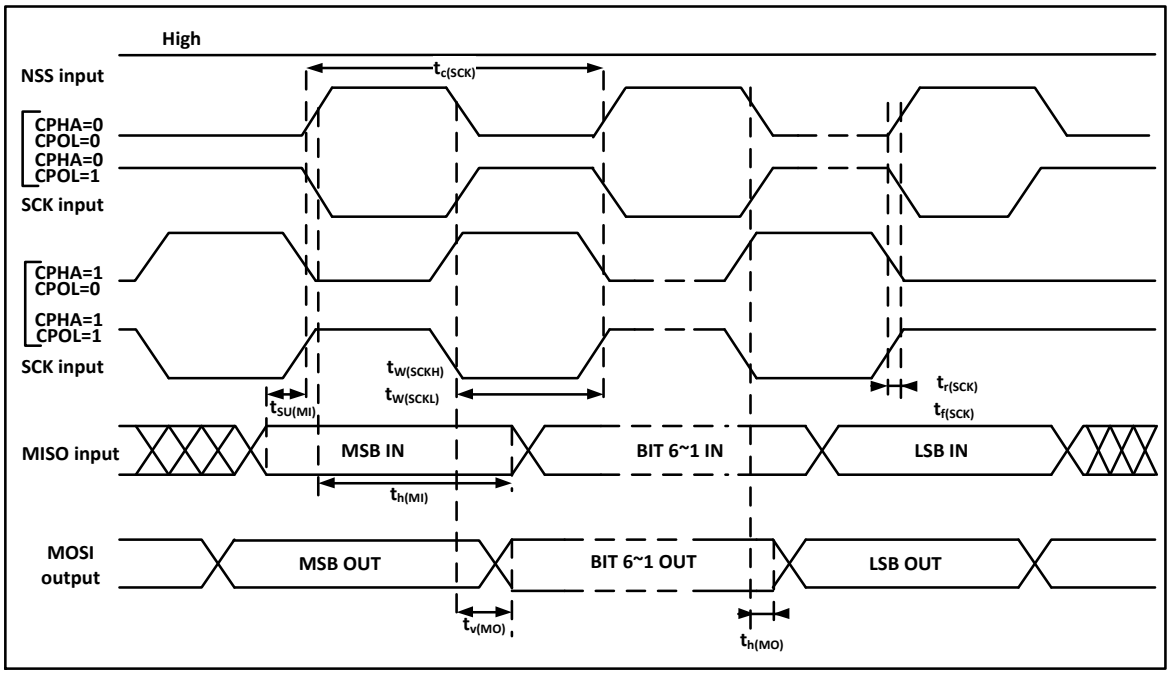


Figure 11 SPI Timing Diagram - Slave Mode and CPHA=1



Note: The measuring points are set at CMOS levels: 0.3VDD and 0.7V_{DD} .

Figure 12 SPI Timing Diagram - Master Mode



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.11 Analog peripherals

5.11.1 ADC

Test parameter description:

- Sampling rate: the number of conversion of analog quantity to digital quantity by ADC per second
  Sample rate=ADC clock/(number of sampling periods + number of conversion periods)

5.11.1.1 12-bit ADC characteristics

Table 48 12-bit ADC Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
V_{DDA}	Power supply voltage	-	2.4	-	3.6	V
I_{DDA}	ADC pwoer consumption	V_{DDA}=3.3V，f_{ADC}=14MHz，Sampling time=1.5 fADCs	-	1	-	mA
f_{ADC}	ADC frequency	-	0.6	-	14	MHz
C_{ADC}	Internal sampling and holding capacitance	-	-	8	-	pF
R_{ADC}	Sampling resistor	-	-	-	1000	Ω
t_S	Sampline Time	f_{ADC}=14MHz	0.107	-	17.1	μs
T_{CONV}	Sampling and conversion time	f_{ADC}=14MHz, 12-bit conversion	1	-	18	μs

Table 49 12-bit ADC Accuracy

Symbol	Parameter	Conditions	Typical values	Maximum value	Unit
|ET|	Composite error	f_{PCLK}=48MHz, f_{ADC}=12MHz, V_{DDA}=2.4V-3.6V T_A=-40℃~105℃	-	3.8	LSB
|EO|	Offset error		-	2.7	
|EG|	Gain error		-	1.9	
|ED|	Differential linear error		-	1	
|EL|	Integral linear error		-	3.4	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.11.1.2 Test of Built-in Reference Voltage Characteristics

Table 50 Embedded Reference Voltage Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
V_{REFINT}	Built-in Reference Voltage	-40℃ < T_A < +105℃ V_{DD}= 2-3.6V	1.19	1.23	1.27	V
t_{START}	ADC_IN17 buffer startup time	-	-	-	10	μs
$T_{S\_vrefint}$	Sampling time of ADC when reading out internal reference voltage	-	4	-	-	μs
ΔV_{REFINT}	Built-in reference voltage extends to temperature range	V_{DDA}=3.3V	-	-	25	mV

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.11.2 DAC

Test parameter description:

- DNL differential non-linear error: the deviation between two consecutive codes is—— 1 LSB
- INL integral non-linear error: the difference between the measured value at code i and the value at code i on the connection between code 0 and the last code 4095

Table 51 DAC Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
V_{DDA}	Analog power supply voltage	-	2.4	-	3.6	V
R_{LOAD}	Resistive load	Load is connected to V_{SSA} with buffer on	5	-	-	kΩ
RO	Output impedance	The resistive load between DAC_OUT and VSS is 1.5MΩ with buffer off	-	-	15	kΩ
C_{LOAD}	Capacitive load	Maximum capacitive load at DAC_OUT pin with buffer on	-	-	50	pF

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
DAC_OUT min	Low DAC_OUT voltage with buffer	Maximum output offset of DAC, (0x0E1) corresponding to 12-bit input code to V_{REF+}= (0xF1B) at 3.6V and V_{REF+}= (0x154) at 2.4V and (0xEAC)	0.2	-	-	V
DAC_OUT max	High output voltage with buffer		-	-	V_{DDA}-0.2	V
I_{DDA}	Power consumption of DAC in quiescent mode	Non-load, the input terminal adopts intermediate code (0x800)	-	-	295	uA
		Non-load, the input terminal adopts difference code (0xF1C)	-	-	340	uA
DNL	Differential non-linear error	Configured with 12-bit DAC	-	-	±2	LSB
INL	Integral non-linear error	Configured with 12-bit DAC	-	-	±5	LSB
Offset	Offset error	V_{REF+}=3.6V, configuring 12-bit DAC	-	-	±8	LSB
Gain error	Gain error	Configured with 12-bit DAC	-	-	±0.5	%

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.11.3 Comparator

Table 52 Comparator Characteristics

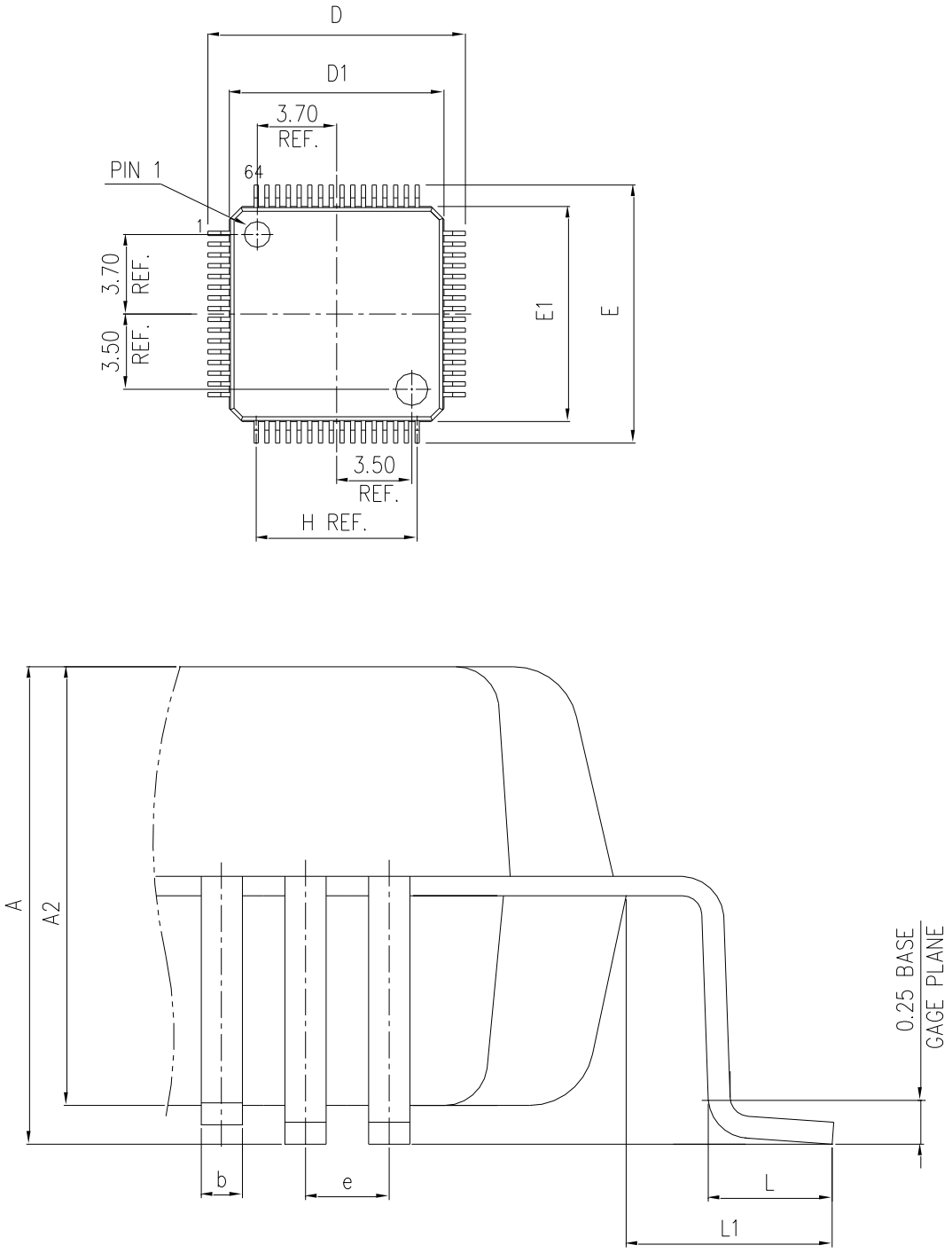
Symbol	Parameter	Conditions		Minimum value	Typical values	Maximum value	Unit
V_{DDA}	Analog power supply voltage	-		V_{DD}	-	3.6	V
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	-
t_D	Full range step, overload propagation delay of 100mV	Very low power mode		-	428	627	ns
		Low-power mode		-	144	165	
		Medium power mode		-	93	100	
		Full speed mode	V_{DDA}≥2.7V	-	32	39	ns
			V_{DDA}＜2.7V	-	45	50	
V_{OFFSET}	Offset error	-		-	-2	+6	mV
V_{HYS}	Comparator hysteresis voltage	Without hysteresis (HYSCFGx[1:0]=00)		-	2	-	mV
		Low hysteresis level (HYSCFGx[1:0]=01)		5	6	7	
		Medium hysteresis level (HYSCFGx[1:0]=10)		9	12	14	
		High hysteresis level (HYSCFGx[1:0]=11)		17	22	26	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

6 Package information

6.1 LQFP64 Package Diagram

Figure 13 LQFP64 Package Diagram



（1） The figure is not drawn to scale.

（2） All pins should be soldered to the PCB

Table 53 LQFP64 Package Data

DIMENSION LIST（FOOTPRINT: 2.00）			
S/N	**SYM**	**DIMENSIONS**	**REMARKS**
1	A	MAX. 1.600	OVERALL HEIGHT
2	A2	1.400±0.050	PKG THICKNESS
3	D	12.000±0.200	LEAD TIP TO TIP
4	D1	10.000±0.100	PKG LENGTH
5	E	12.000±0.200	LEAD TIP TO TIP
6	E1	10.000±0.100	PKG WDTH
7	L	0.600±0.150	FOOT LENGTH
8	L1	1.000 REF	LEAD LENGTH
9	e	0.500 BASE	LEAD PITCH
10	H（REF）	（7.500）	CUM LEAD PITCH
11	b	0.22±0.050	LEAD WIDTH

（1） Dimensions are expressed in mm

Figure 14 LQFP64-64 pins, 10×10mm recommended welding Layout

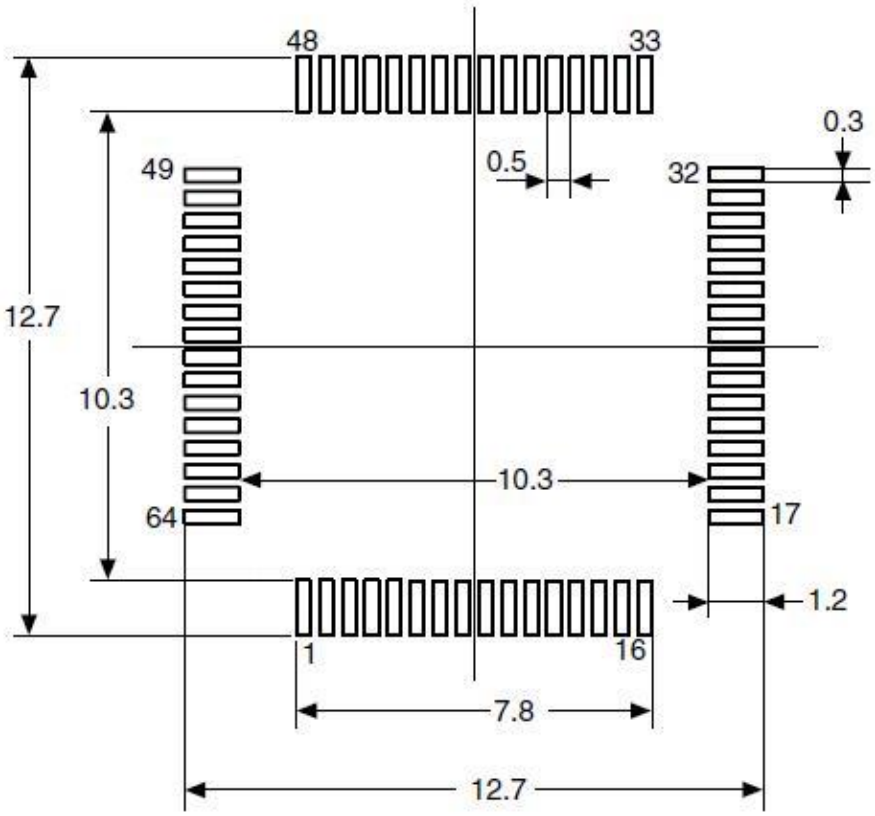
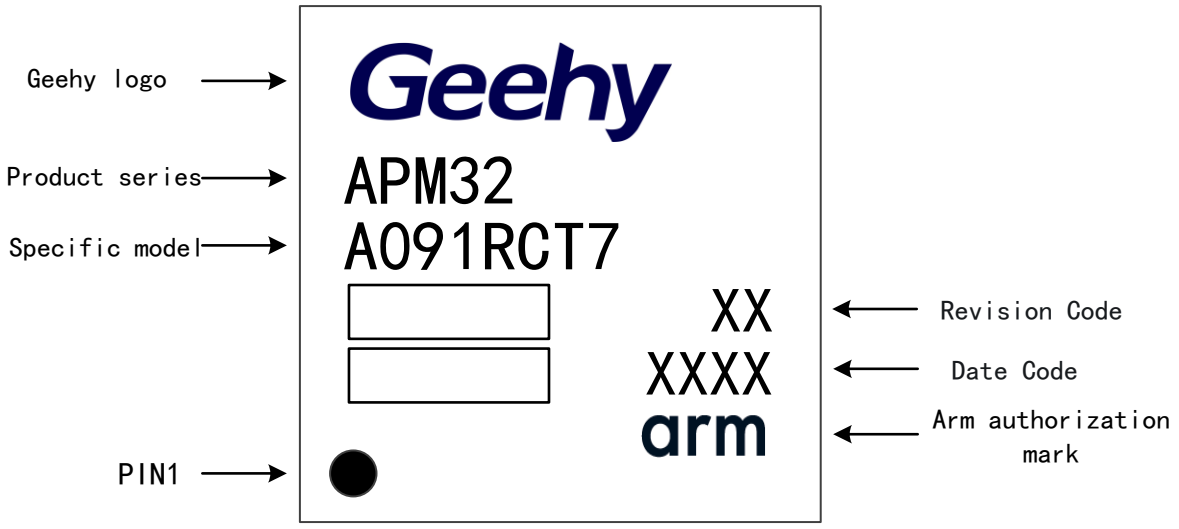


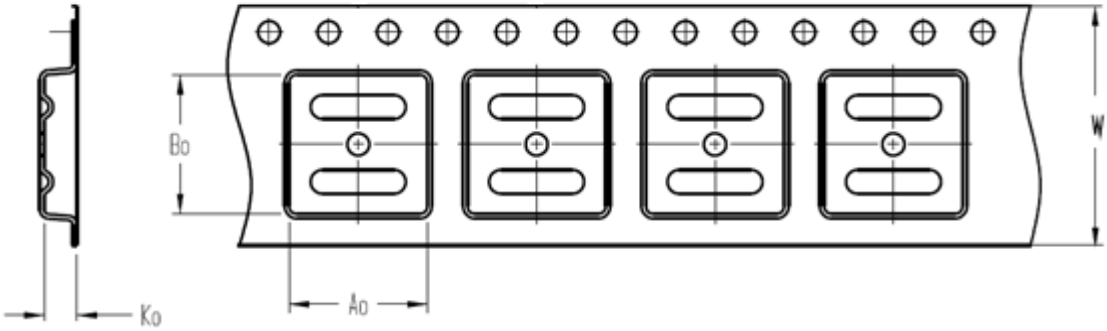
Figure 15 LQFP64-64 pins, 10×10mm package identification



7 Packaging Information

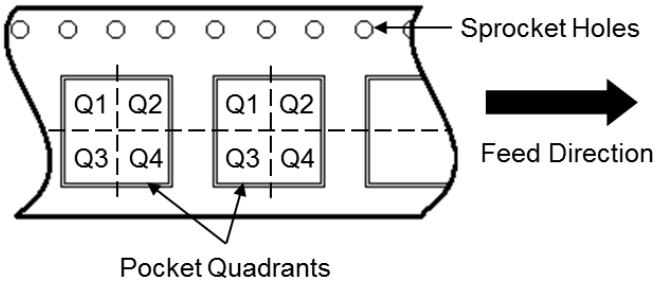
7.1 Reel Packaging

Figure 16 Specification Drawing of Reel Packaging

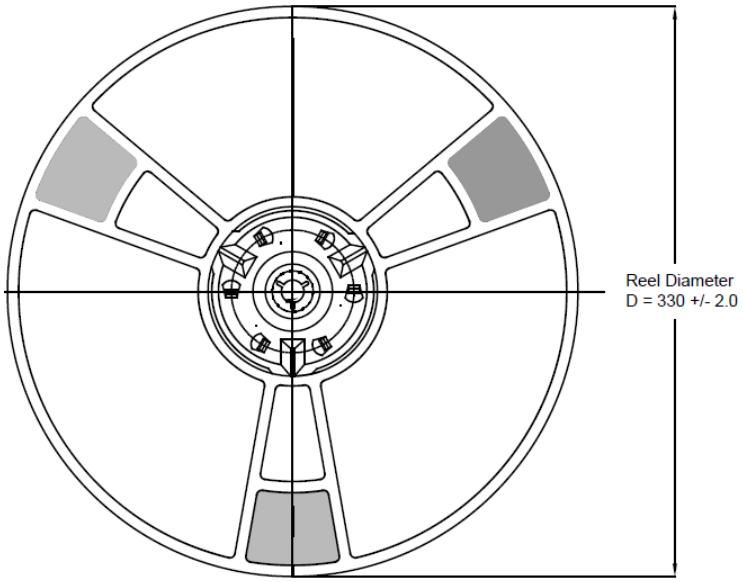


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape

Quadrant Assignments for PIN1 Orientation in Tape



Reel Dimensions



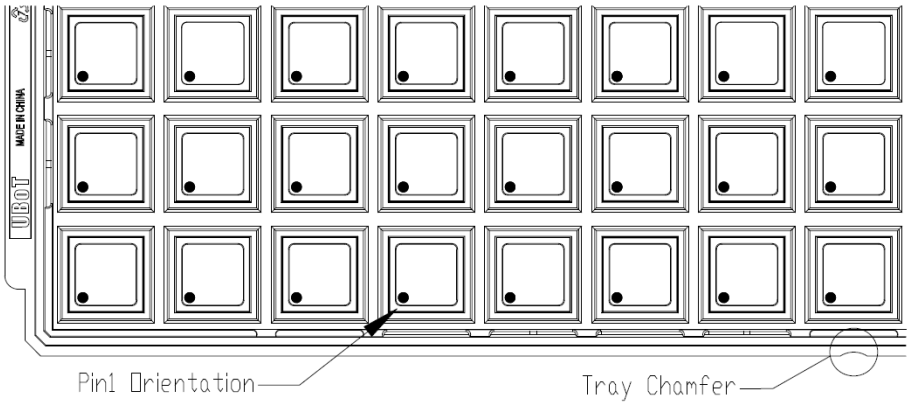
All photos are for reference only, and the appearance is subject to the product.

Table 54 Reel Packaging Parameter Specification Table

Device	Package Type	Pins	SPQ	Reel Diameter（mm）	A0（mm）	B0（mm）	K0（mm）	W（mm）	Pin1 Quadrant
APM32A091RCT7	LQFP	64	1000	330	12.35	12.35	2.2	24	Q1

7.2 Tray packaging

Figure 17 Tray Packaging Diagram



Tray Dimensions

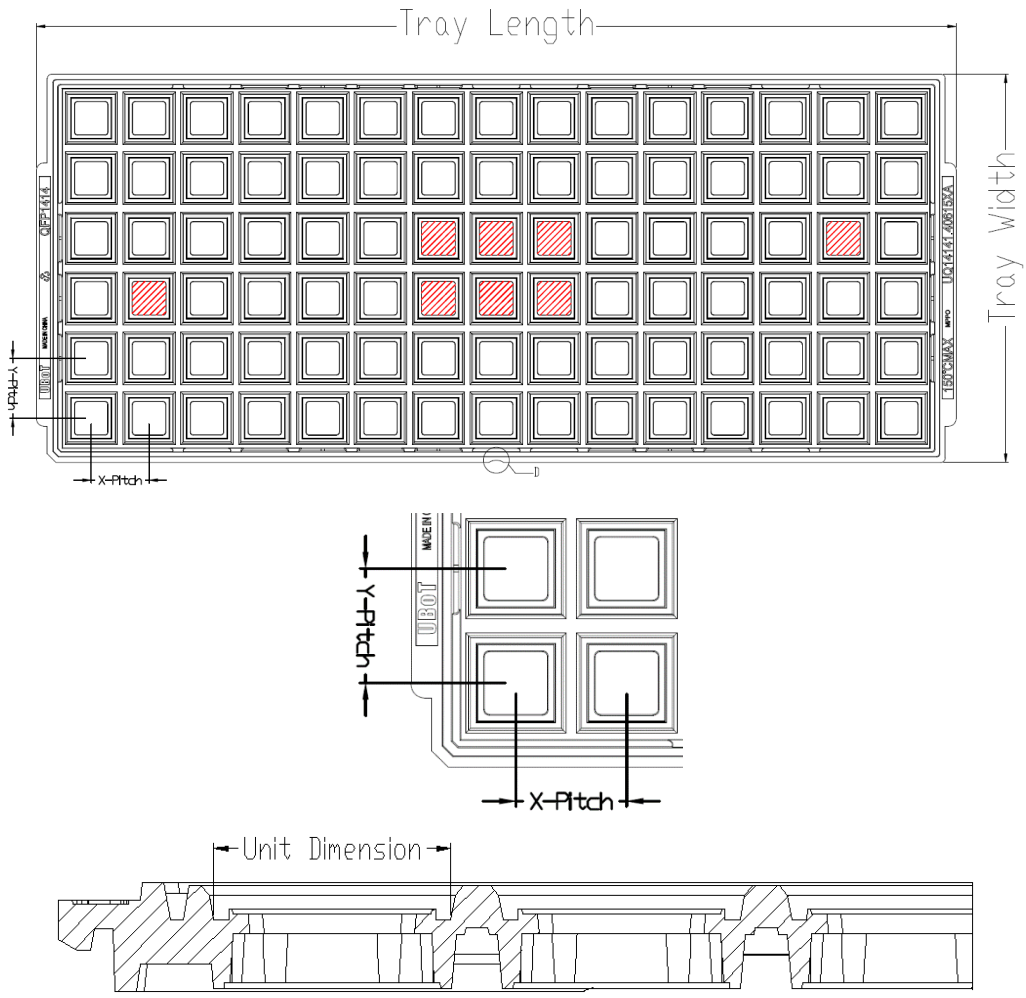


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Table 55 Tray Packaging Parameter Specification Table

Device	Package Type	Pins	SPQ	X-Dimension（mm）	Y-Dimension（mm）	X-Pitch（mm）	Y-Pitch（mm）	Tray Length（mm）	Tray Width（mm）
APM32A091RCT7	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9

8 Ordering Information

Figure 18 Product Information Naming Rules

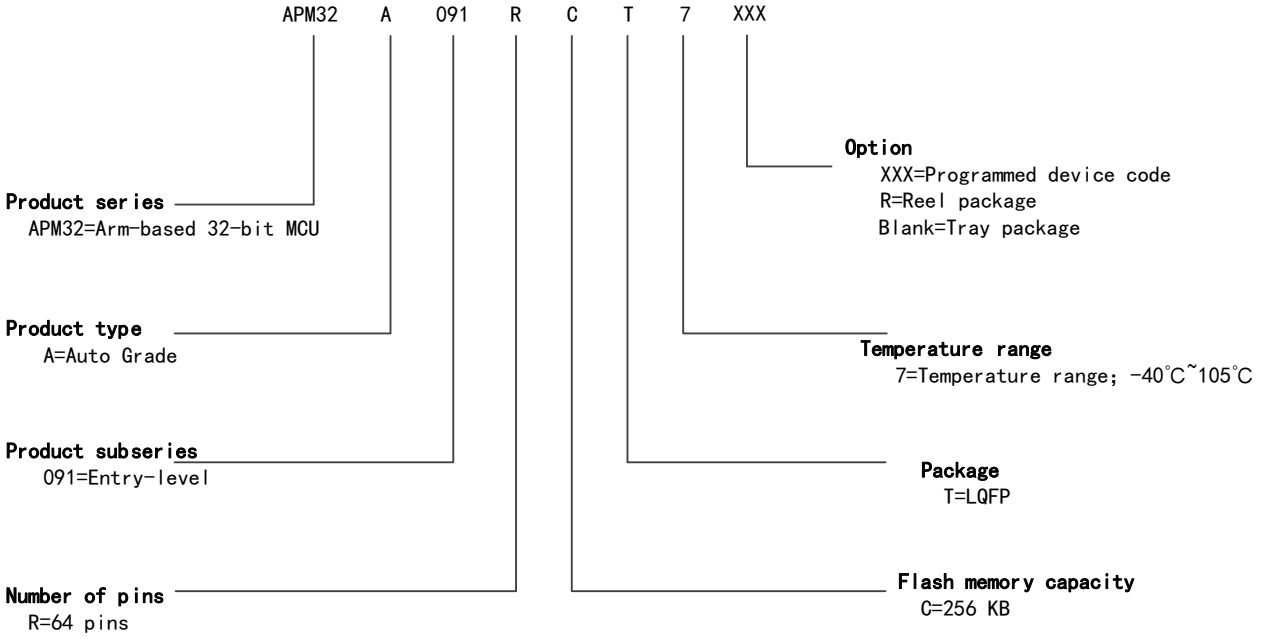

Table 56 Ordering Information Table

Order Code	Flash (KB)	SRAM (KB)	Package	SPQ	Temperature Range
APM32A091RCT7-R	256	32	LQFP64	1000	-40℃~105℃
APM32A091RCT7	256	32	LQFP64	1600	-40℃~105℃

Note :SPQ= Minimum number of packages

9 Commonly Used Function Module Denomination

Table 57 Commonly Used Function Module Denomination

Chinese description	Short name
Reset management unit	RMU
Clock management unit	CMU
Reset and clock management	RCM
Clock recovery system	CRS
External interrupt	EINT
Genera-purpose IO	GPIO
Alternate function IO	AFIO
Wake up controller	WUPT
Buzzer	BUZZER
Independent watchdog timer	IWDT
Window watchdog timer	WWDT
Timer	TMR
CRC controller	CRC
Power Management Unit	PMU
DMA controller	DMA
Analog-to-digital converter	ADC
Digital-to-analog converter	DAC
Real-time clock	RTC
External memory controller	EMMC
Controller local area network	CAN
I2C interface	I2C
Serial peripheral interface	SPI
Universal asynchronous transmitter receiver	UART
Universal synchronous and asynchronous transmitter receiver	USART
Flash interface control unit	FMC

10 Revision History

Table 58 Document Revision History

Date	Version	Change History
2022.12	1.0	New

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