Low R_{DSON} Power Load Switch with Current Monitoring

Features

- **N-CH MOSFET $R_{DS(ON)}$: 12mΩ(typ.)**
- **Ultra-low quiescent current : Less than 50uA**
- **Input Voltage Range (VIN) : 0.8V ~ V_{DD}**
- **Bias Voltage Range (VDD) : 3V ~ 5.5V**
- **Built in Internal Charge Pump Function for Internal gate driver**
- **Built in ADJ Current Limit function**
- **Built in Bulk Select function (without body diode effect)**
- **Built in VOUT Discharge function when Switch disable**
- **Built in Adjustable Soft Start function by SS pin**
- **Built in Input Over Voltage Protection**
- **Built in Over-Temperature Protection**
- **Built in VDD Under Voltage Lock Out**
- **Built in Enable / Shutdown Control by EN pin with initial floating Low**
- **Built in POK Indication Output**
- **Built in IMON function with 5% accuracy for current detection**
- **Tiny small VTQFN2x3-17 package**

General Description

The APL3557 is a power-distribution switch with some protection functions that can deliver current up to 5A. The device incorporates a 12mΩ N-channel MOSFET power switch that is controlled by an enable logic pin and has a SS pin dedicated to soft start ramp-up rate control that can be used in application where the inrush current is concerned.

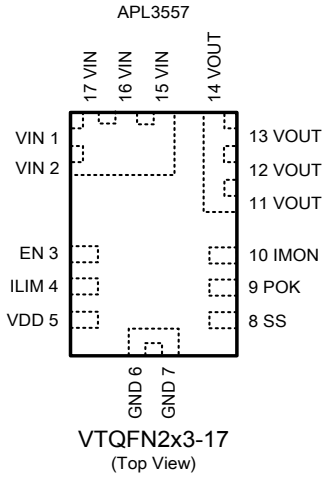
The device integrates some protection features, including current limit protection, over temperature protection, and input over voltage protection. The current limit protection can protect down-stream devices from catastrophic failure by limiting the output current at current-limit threshold during over-load or short-circuit events. The over temperature protection function shuts down the N-channel MOSFET power switch when the junction temperature rises beyond 140°C.

Other features include an accurate current monitor function. The device is available in lead free VTQFN2x3-17 package.

Applications

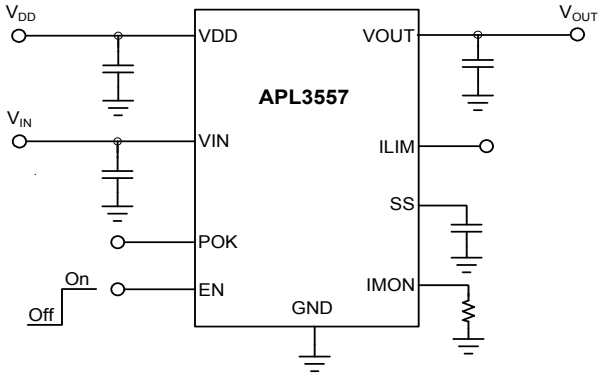
- **Notebook**
- **AIO PC**

Pin Configuration

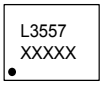


VTQFN2x3-17
(Top View)

Simplified Application Circuit



Ordering and Marking Information

APL3557 □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QF: VTQFN2x3-17 Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Lead Free Code G : Halogen and Lead Free Device
APL3557 QF : 	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN}, V_{DD}	Supply Voltage (V_{IN}, V_{DD}) to GND	-0.3 ~ 6	V
V_{OUT}	Output Voltage V_{OUT} to GND	-0.3 ~ 6	V
$V_{I/O}$	Input & Output or I/O (EN, POK, ILIM, IMON)	-0.3 ~ 6	V
P_D	Power Dissipation	Internally Limited	W
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)	260	°C
V_{ESD}	Minimum ESD Rating (Human Body Mode) (MM Mode)	±2 0.2	kV

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under"recommended operating conditions"is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics (Note2)

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air	60	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{DD}	VDD Supply Voltage ($V_{DD} \geq V_{IN}$)	3.0 ~ 5.5	V
V_{IN}	VIN Supply Voltage	0.8 ~ V_{DD}	V
I_{OUT}	Output Current (continue)	0 ~ 5	A
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the typical application circuit

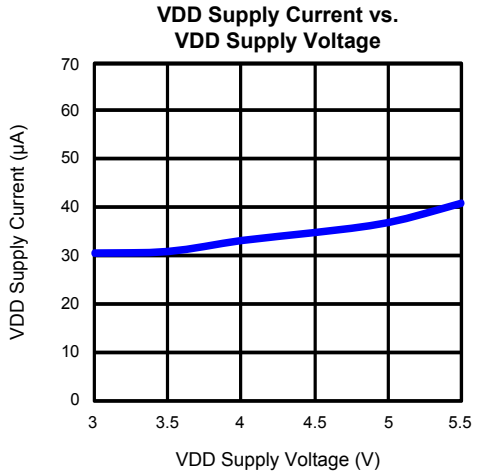
Electrical Characteristics

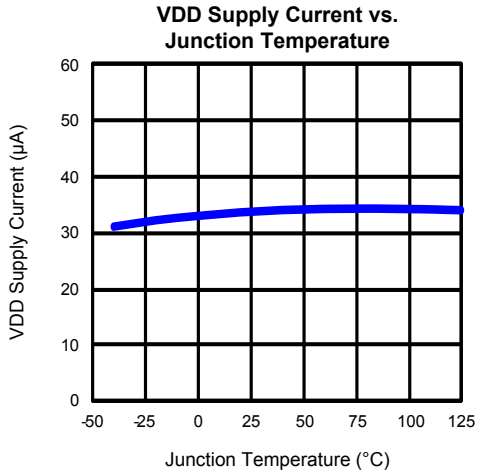
Unless otherwise specified, these specifications apply over V_{IN}=5V, V_{DD}=5V, V_{EN} =5V, T_A=25°C.

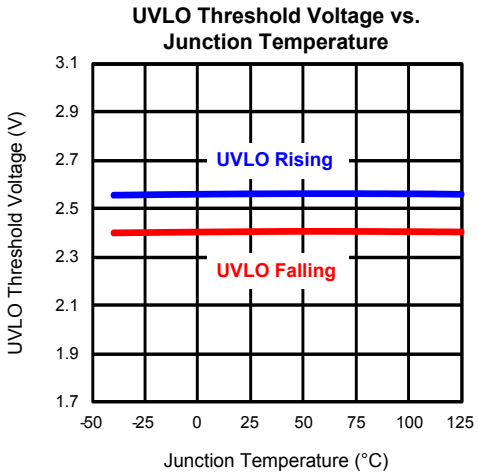
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
SUPPLY CURRENT						
I_{VDD}	VDD Supply Current	No load	-	30	50	μA
I_{VDD_SD}	VDD Supply Current at Shutdown	No Load, V_{VDD}=5V, V_{EN}=0V	-	-	1	μA
I_{VIN}	VIN Supply Current	No load	-	10	-	μA
I_{VIN_OFF}	VIN Supply Current at Shutdown	No Load, V_{VDD}=V_{VIN}=5V, V_{EN}=0V	-	-	1	μA
I_{OUT_RCP}	VOUT Reverse Leakage Current	V_{OUT}=5.5V, V_{IN}=0V, EN go Low	-	-	1	μA
UNDER-VOLTAGE LOCK OUT (UVLO)						
	Rising VDD UVLO Threshold	V_{DD} Rising	2.3	2.5	2.7	V
	VDD UVLO Hysteresis		-	0.2	-	V
EN INPUT PIN						
V_{IH}	Input Logic High		1.7	-	-	V
V_{IL}	Input Logic Low		-	-	0.8	V
	Pull Down Resistor	V_{DD}=5V	-	1	-	MΩ
$t_{D(ON)}$	Turn on Delay Time	From ENABLE to VOUT Rising, C_{SS}=0pF	-	35	-	μs
$t_{D(OFF)}$	Turn off Delay Time	From DISABLE to VOUT Falling	-	2	-	μs
POWER SWITCH						
$R_{DS(ON)}$	Power Switch On Resistance	V_{DD}=5V &3.3V, at 25 degree	-	12	-	mΩ
R_{DIS}	VOUT Discharge Resistance	V_{EN}=0V, VOUT force 1V	-	10	-	Ω
OVERT-TEMPERATURE PROTECTION						
T_{OTP}	Over-Temperature Threshold		-	140	-	°C
CURRENT LIMIT PROTECTION (Note 4)						
I_{LIM}	Current Limit Threshold	V_{ILIM} < 0.5V	4.2	-	5	A
		V_{ILIM} > 2V (Floating)	6	-	8	A
	Fold-back Current Limit Threshold	V_{ILIM} < 0.5V	-	2.6	-	A
		V_{ILIM} > 2V (Floating)	-	4	-	A
	Response Time of Short current		-	-	1	us
Input Voltage Protection						
V_{OVP}	Input OVP trip voltage		-	5.8	-	V
T_{deb}	Response Time for Voltage Detection		-	200	-	μs
POWER GOOD INDICATOR						
	POK High Threshold	POK Go High	-	85	-	%
	POK Low Threshold	POK Go Low	-	40	-	%
	POK Pull Low voltage	POK sink 5mA	-	0.25	-	V
CURRENT MONITOR PARAMETER						
I_{MON}	I_{OUT} Current to I_{MON} Current Gain	I_{OUT} / I_{MON}	-	5400	-	A/A
	I_{MON} Voltage Accuracy	I_{OUT} = 0.5A	-20	-	20	%
		I_{OUT} = 3A	-7.5	-	7.5	%
		I_{OUT} = 6A	-5	-	5	%

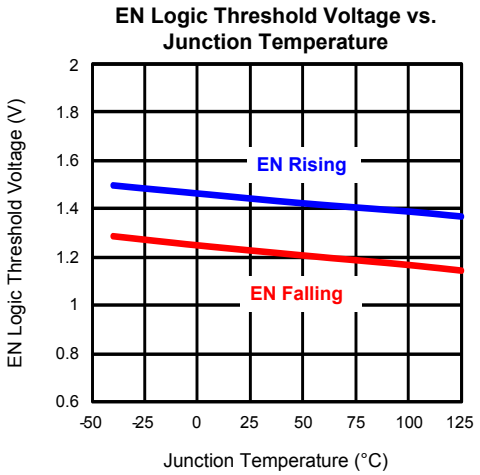
Note 4: During start-up, the current limit is always set high.

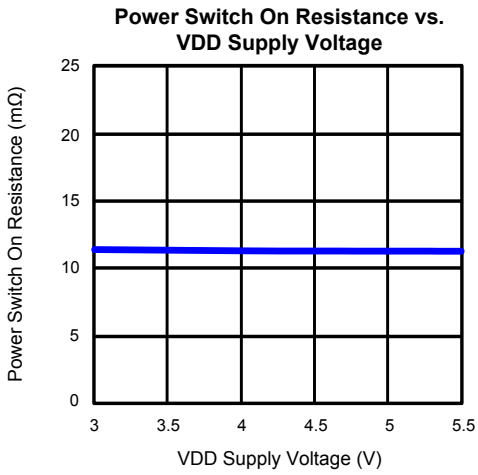
Typical Operating Characteristics

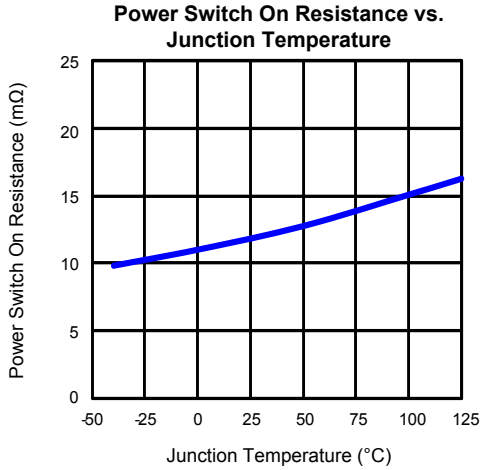




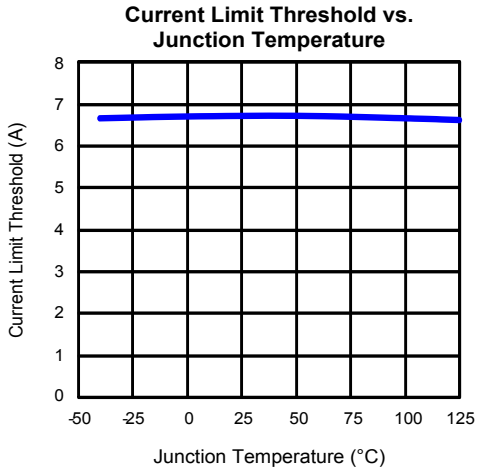








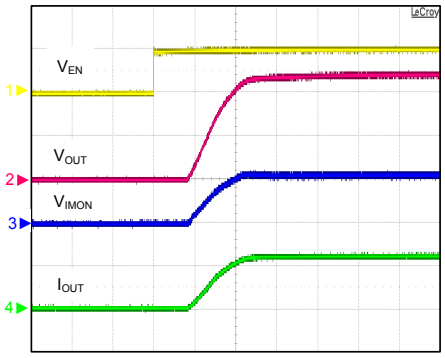
Typical Operating Characteristics (Cont.)



Operating Waveforms

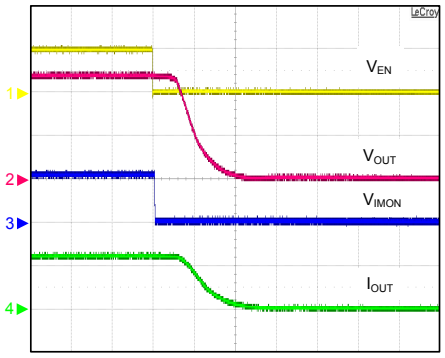
Refer to the typical application circuit. The test condition is V_{IN}=V_{DD}=V_{EN}=5V, T_A= 25°C, R_{IMON}=510Ω unless otherwise specified.

Enable



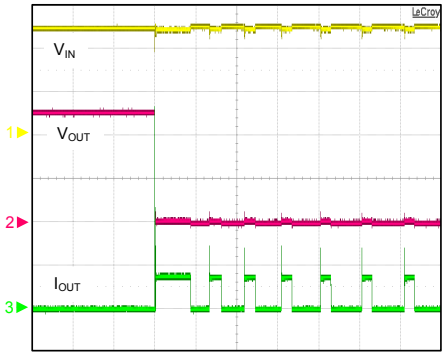
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: V_{IMON}, 500mV/Div, DC
CH4: I_{OUT}, 5A/Div, DC
TIME: 50μs/Div

Shutdown



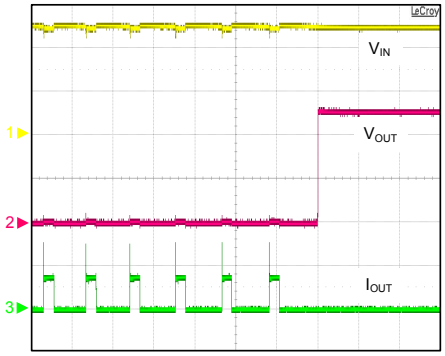
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: V_{IMON}, 500mV/Div, DC
CH4: I_{OUT}, 5A/Div, DC
TIME: 5μs/Div

Short Circuit Response



CH1: V_{IN}, 2V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: I_{OUT}, 5A/Div, DC
TIME: 10ms/Div

Short Circuit Release

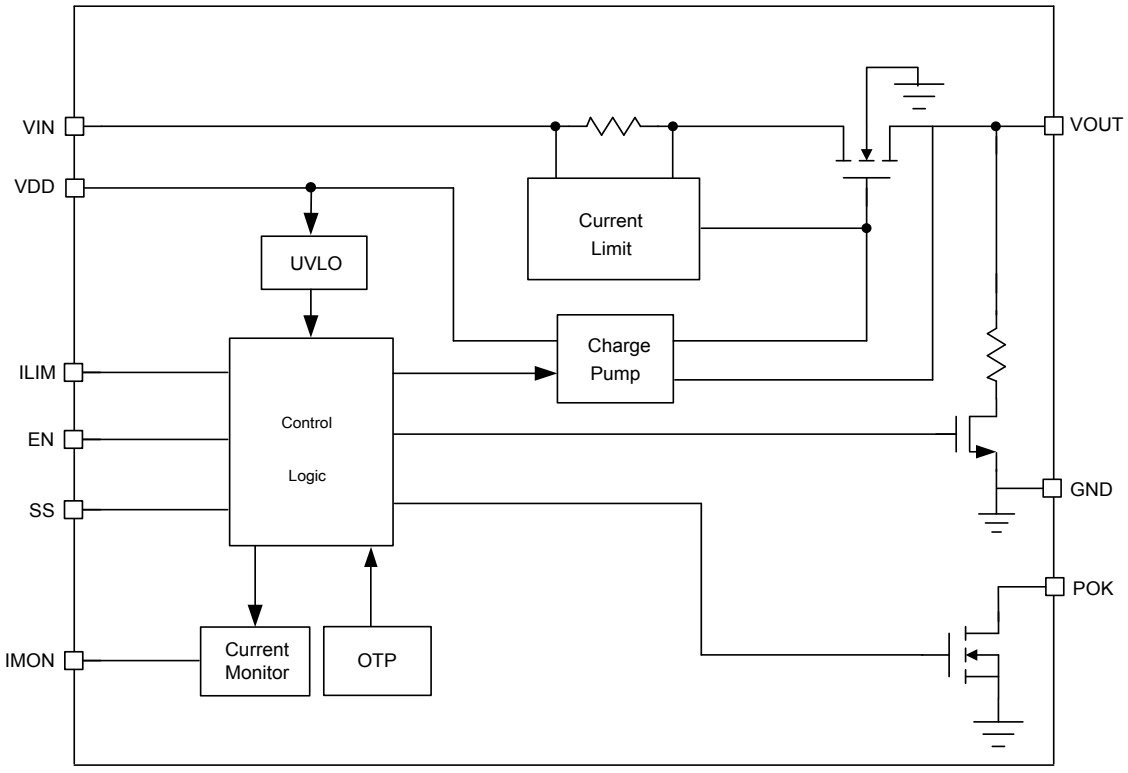


CH1: V_{IN}, 2V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: I_{OUT}, 5A/Div, DC
TIME: 10ms/Div

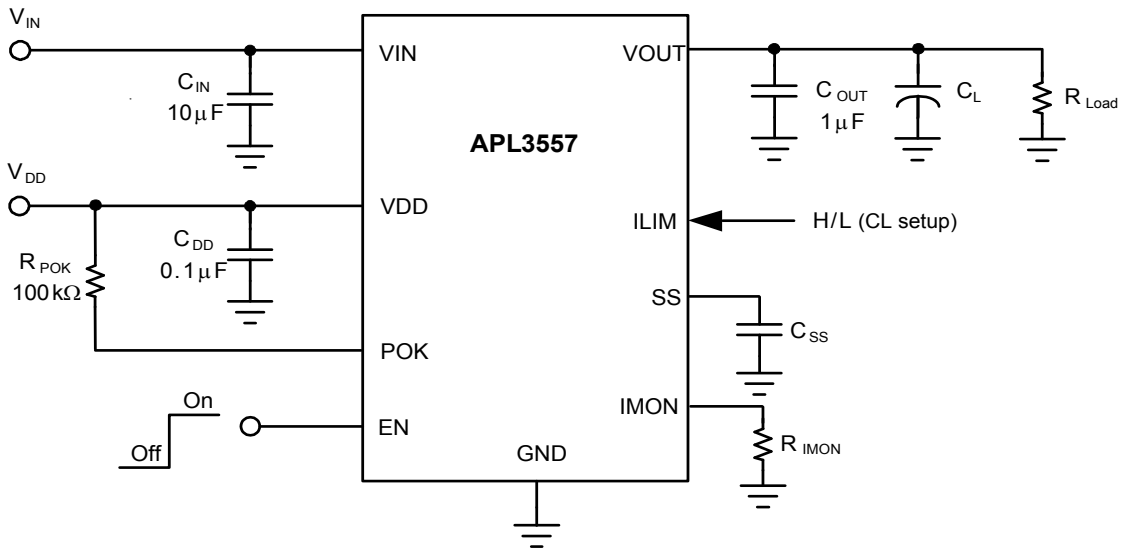
Pin Description

PIN		Description
NO.	NAME	
1,2,15,16,17	VIN	Power supply input pin.
3	EN	EN control pin. (Active Low with internal 1MΩ Pull Down resistor)
4	ILIM	Current Limit Setup. Pull High / Pull Low to adjust 2 step current limit level.
5	VDD	VDD input pin for internal control circuit.
6,7	GND	Ground.
8	SS	Soft Start Control of Switch.
9	POK	Power Good Indicator.
10	IMON	Output current sense monitor indicator.
11,12,13,14	VOUT	Switch Output.

Block Diagram



Typical Application Circuit



C_{SS}(nF)	Soft-Start Time (μs) 10% to 90%, V_{DD}=5V, C_{IN}=10μF, C_{OUT}=1μF						
	VIN=5V	VIN=3.3V	VIN=1.8V	VIN=1.5V	VIN=1.2V	VIN=1.05V	VIN=0.8V
0	41.5	29.7	19.3	16.9	14.2	12.9	10.4
1	104.6	72.3	41.5	34.8	28.3	24.8	19.3
4.7	520	353	204.8	173.2	141.8	126.2	100.2
10	1047	719.3	408.9	345.7	283.4	251.8	197.9

Function Description

Under-voltage Lockout (UVLO)

A under-voltage lockout (UVLO) circuit monitors the VDD pin voltage to prevent wrong logic controls. The UVLO function initiates a soft-start process after the VDD supply voltages exceed rising UVLO voltage threshold during powering on.

Current-Limit Protection

The APL3557 power switch provides the current-limit protection function. During current-limit, the devices limit output current at current-limit threshold. For reliable operation, the device should not be operated in current limit for extended period time.

Soft-Start

The APL3557 provides an adjustable soft-start circuitry to control rise rate of the output voltage and limit the current surge during start-up. The soft-start time is set with a capacitor from the SS pin to the ground.

Enable/Disable

Pull the EN below 0.8V to disable the device and pull EN above 1.7V to enable the device. When the IC is disabled the supply current is reduced to less than 1μA.

Power OK Indicator

The power okay function monitors the output voltage and drives the POK low to indicate a fault. When the VOUT output voltage reaches to 85% of VIN input voltage, the POK is pulled high after the delay. When the VOUT output voltage falls to 40% of VIN input voltage, the POK will be pulled low. Since the POK is an open-drain device, connecting a resistor to a pull high voltage is necessary.

Over-Temperature Protection

When the junction temperature exceeds 140°C, the internal thermal sense circuit turns off the power FET and allows the device to cool down. When the device's junction temperature cools by 20°C, the internal thermal sense circuit will enable the device, resulting in a pulsed output during continuous thermal protection. Thermal protection is designed to protect the IC in the event of over temperature conditions. For normal operation, the junction temperature cannot exceed T_J=125°C.

Input Over-voltage Protection

The over-voltage function monitors the input voltage by VIN pin. Once the input voltage exceeds the threshold, the comparator outputs a logic signal to turn off the N-channel MOSFET to prevent the high input voltage from damaging the electronics in the system. When the input over-voltage condition is removed, the N-channel MOSFET is turned on again by running through the softstart.

Application Information

Input Capacitor

A 1μF or higher ceramic bypass capacitor from VIN to GND, located near the APL3557, is strongly recommended to suppress the ringing during over-load or short-circuit fault event. Without the bypass capacitor, the over-load or output short may cause sufficient ringing on the input (from supply lead inductance) to damage internal control circuitry. Input capacitor is especially important to prevent VIN from ringing too high in some applications where the inductance between power source to VIN is large due to poor PCB layout or purposely adding an inductive component in front of VIN pin.

When the VIN's supply voltage is higher, it is required to add some adequate amount of capacitance of input capacitor into VIN pin for overshoot suppression because a slight ringing of VIN is most likely to exceed VIN's absolute maximum rating, or else the device could be burnout during over load conditions.

Output Capacitor

A low-ESR 1μF MLCC, aluminum electrolytic or tantalum between VOUT and GND is strongly recommended to reduce the voltage droop during hot-attachment of downstream peripheral. Higher-value output capacitor is better when the output load is heavy. Additionally, bypassing the output with a 0.1μF ceramic capacitor improves the immunity of the device to short-circuit transients.

IMON Resistor

R_{IMON} is a series resistor between IMON and GND. Calculation example is provided below.

IMON Calculation :
$I_{MON} = I_{OUT} / 5400$

IOUT(A)	IMON(mA)	RMON(Ω)	VMON(V)
0.5	0.092592593	1000	0.092592593
3	0.555555556	1000	0.555555556
6	1.111111111	1000	1.111111111
7	1.296296296	1000	1.296296296

Power Sequence

The following figure 1 shows the recommended power sequence. The output pin cannot be load before VOUT reach approximately 0.5V.

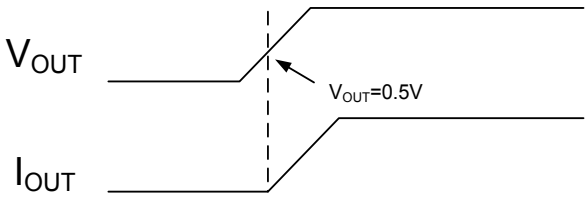


Figure 1

Layout Consideration

The PCB layout should be carefully performed to maximize thermal dissipation and to minimize voltage drop, droop and EMI. The following guidelines must be considered:

1. Please place the input capacitors near the VIN pin as close as possible.

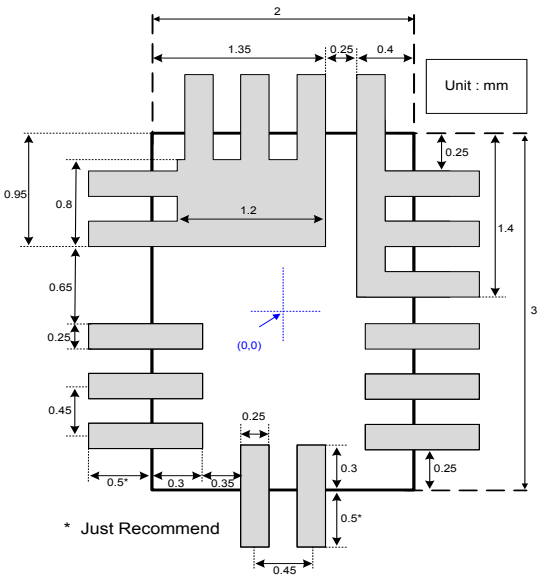
2. Output decoupling capacitors for load must be placed near the load as close as possible for decoupling high frequency ripples.

3. Locate APL3557 and output capacitors near the load to reduce parasitic resistance and inductance for excellent load transient performance.

4. The negative pins of the input and output capacitors and the GND pin must be connected to the ground plane of the load.

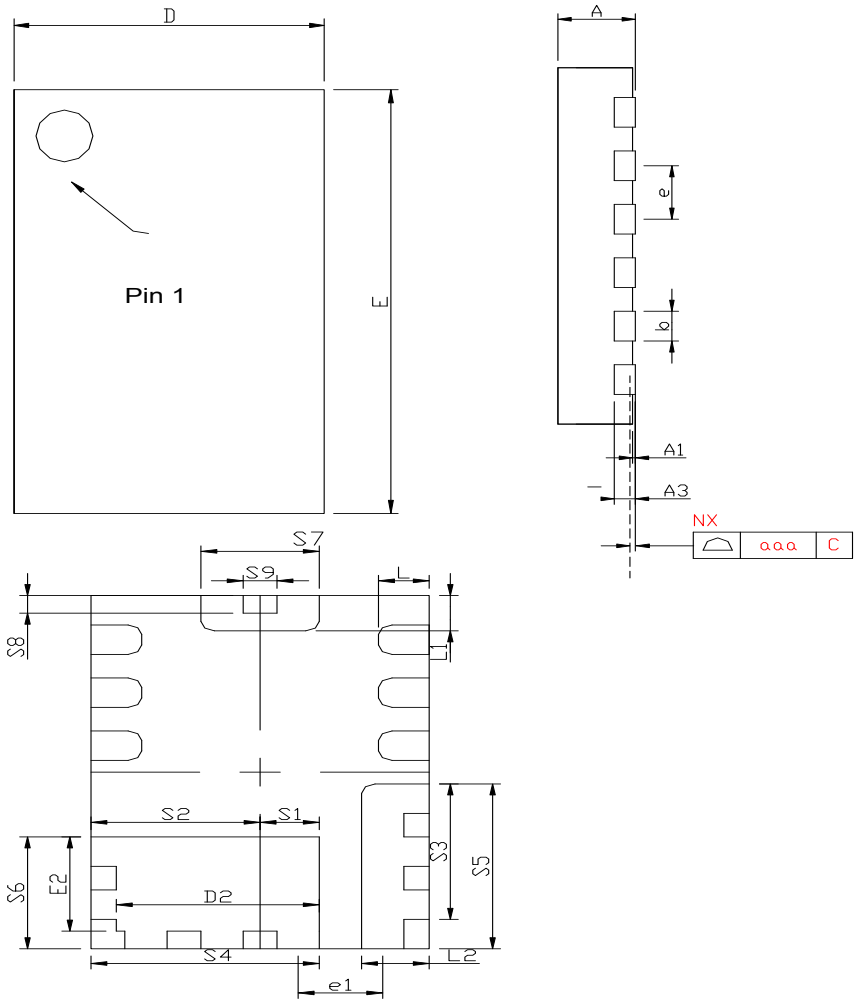
5. Keep VIN and VOUT traces as wide and short as possible.

Recommended Minimum Footprint



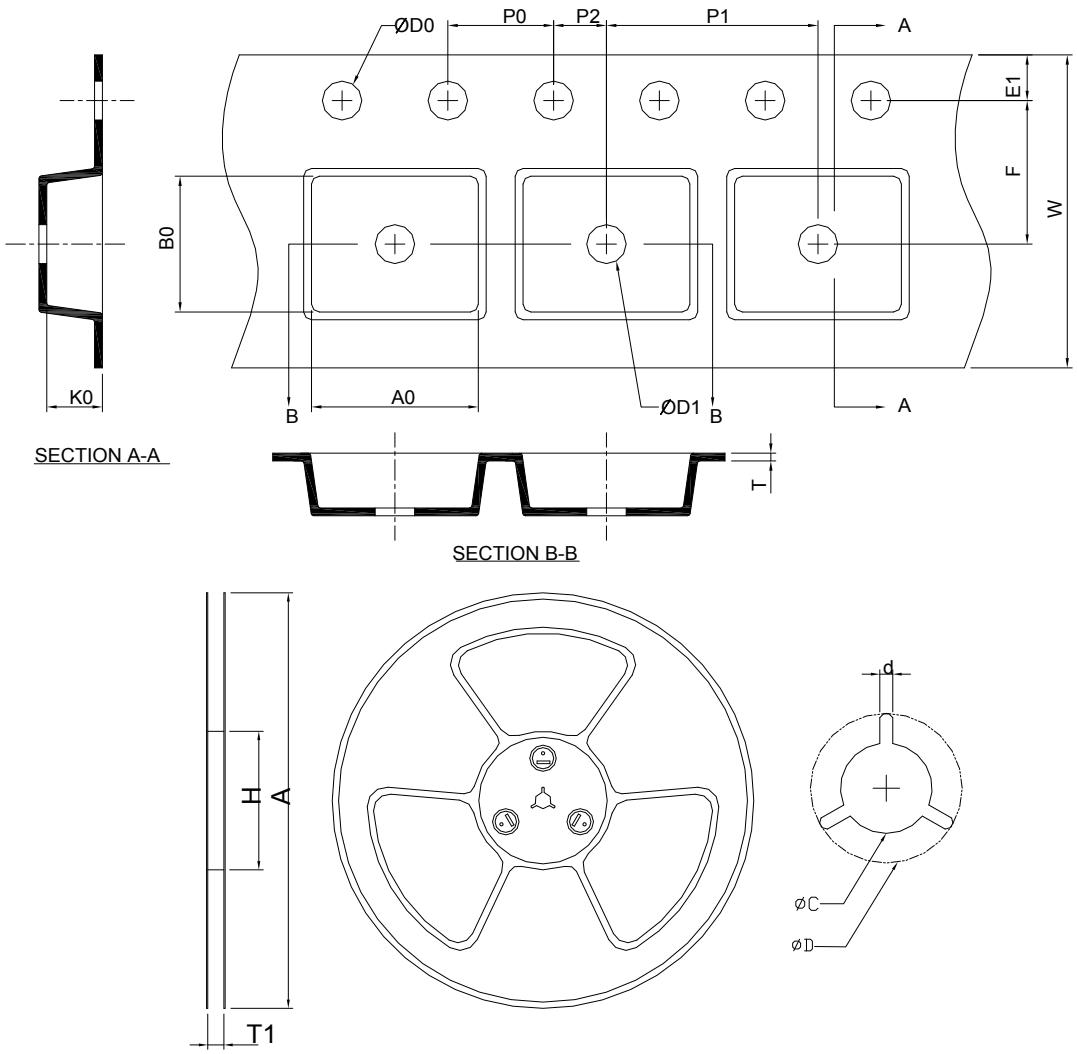
Package Information

VTQFN2x3-17



SYMBOL	VTQ FN2*3-17			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.50	0.60	0.020	0.024
A1	0.00	0.05	0.000	0.002
A3	0.15 REF		0.006 REF	
b	0.20	0.30	0.008	0.012
D	1.90	2.10	0.075	0.083
E	2.90	3.10	0.114	0.122
e	0.45 BSC		0.018 BSC	
e1	0.50 BSC		0.020 BSC	
D2	1.15	1.25	0.045	0.049
E2	0.75	0.85	0.030	0.033
L	0.25	0.35	0.010	0.014
L1	0.25	0.35	0.010	0.014
L2	0.35	0.45	0.014	0.018
S1	0.30	0.40	0.012	0.016
S2	0.95	1.05	0.037	0.041
S3	1.10	1.20	0.043	0.047
S4	1.30	1.40	0.051	0.055
S5	1.35	1.45	0.053	0.057
S6	0.90	1.00	0.035	0.039
S7	0.65	0.75	0.026	0.030
S8	0.10	0.20	0.004	0.008
S9	0.15	0.25	0.006	0.010
aaa	0.08		0.003	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
VTQFN(2x3)	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0+0.30 -0.10	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	0.5 MIN.	0.25±0.05	2.20±0.05	3.25±0.05	0.80+0.10 -0.05

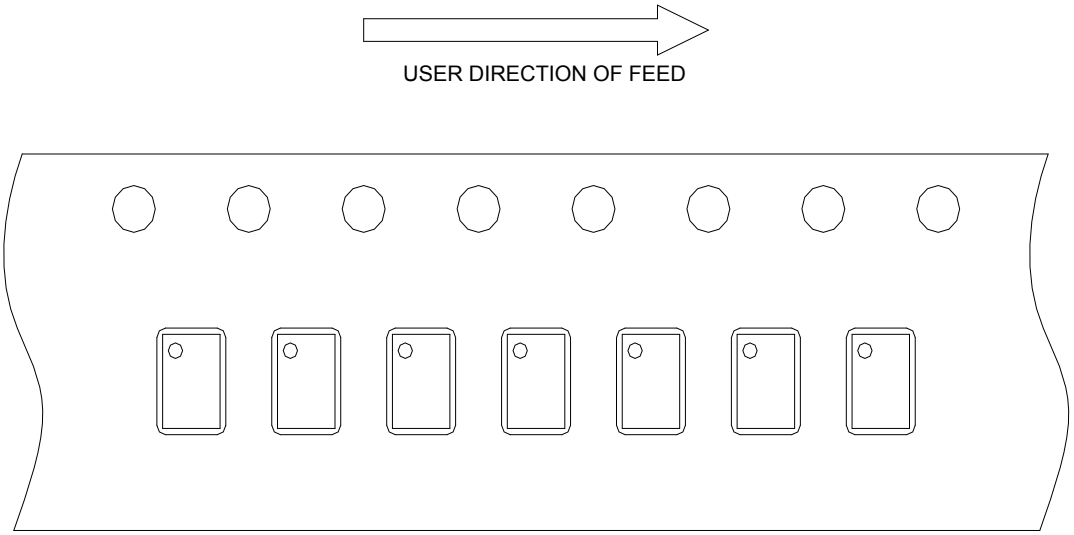
(mm)

Devices Per Unit

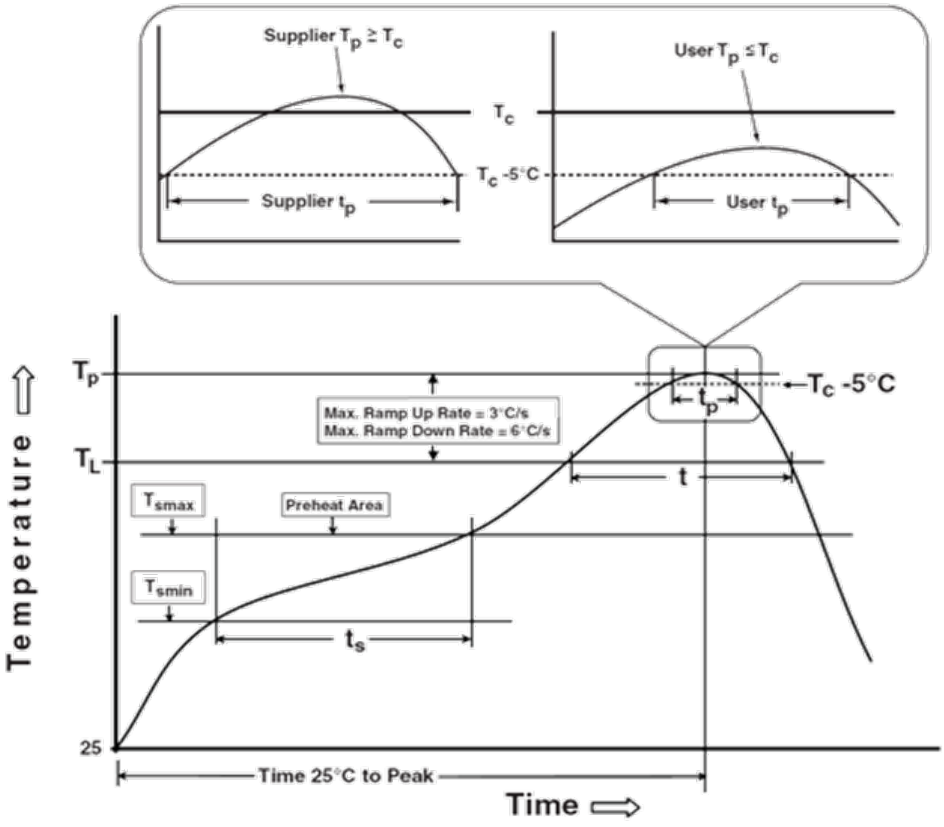
Package type	Packing	Quantity
VTQFN(2x3)	Tape & Reel	2500

Taping Direction Information

VTQFN2x3-17



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≧ 2KV
MM	JESD-22, A115	VMM ≧ 200V
Latch-Up	JESD 78	10ms, 1_{tr} ≧ 100mA

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