APL3556

Adjustable Current Limit Power Distribution Switches

Features

- **50mΩ Power Switch On Resistance**
- **Wide Supply Voltage Range: 2.9V to 5.5V**
- **Adjustable Current Limit Protection**
- **Fast Over current Response: 2μs (typ.)**
- **Over-Temperature Protection**
- **Fault Indication Output**
- **Reverse Input-Output Voltage Protection: 25mV (typ.)**
- **Enable Input**
- **Built-in Soft-Start**
- **UL Approved-File No. E328191**
- **UL-CB Scheme IEC/EN62368-1 Certified**
- **TUV IEC/EN62368-1 Certified**

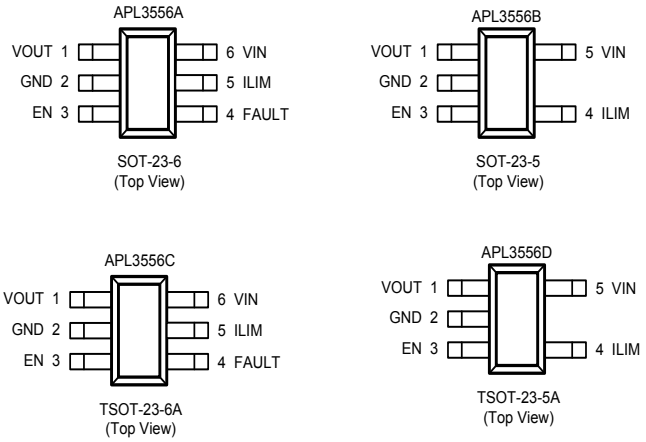
General Description

The APL3556 series of power switches integrate a 50mΩ N-channel MOSFET power switch, an enable input pin, a fault flag and some protection functions into a single package. The protection features include adjustable/fix current limit, reverse current protection, and over temperature protection. APL3556 offer an adjustable currentlimit threshold between 62mA and 6A (typ.) via an external resistor. The reverse current protection disable the power switch when the output voltage is driven higher than the input to protect devices on the input side of the switch. The FAULT output asserts low during over current and reverse current conditions. The over-temperature protection limits the junction temperature below 150°C in case of short circuit or over load conditions.

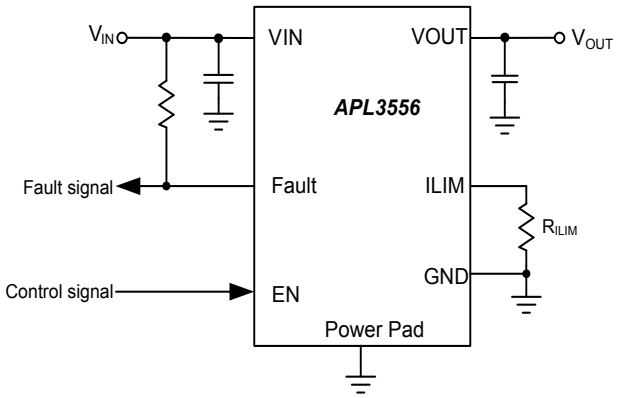
Applications

- **Notebook and Desktop Computers**
- **USB Ports**
- **High-Side Power Protection Switchs**
- **MHL Ports**

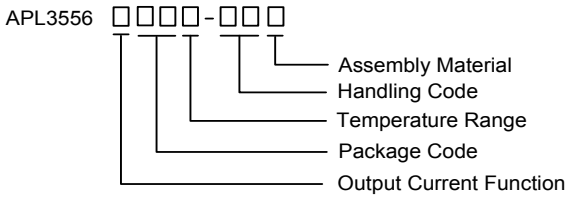
Pin Configuration



Simplified Application Circuit



Ordering and Marking Information



Package Code
CT: TSOT-23-6A BT: TSOT-23-5A
C: SOT-23-6 B: SOT-23-5
Operating Ambient Temperature Range
I : -40 to 85°C
Handling Code
TR : Tape & Reel
Output Current Function
A/B : 2A C/D : 3A
Assembly Material
G: Halogen and Lead Free Device

APL3556D BT:	56DX	X - Date Code
APL3556C CT:	56CX ●	X - Date Code
APL3556B B:	56BX	X - Date Code
APL3556A C:	56AX ●	X - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
	Voltage range on VIN, VOUT, EN, ILIM, FAULT to GND	-0.3 ~ 7	V
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics (Note2)

Symbol	Parameter		Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air	TSOT-23-5A	260	°C/W
		TSOT-23-6A	250	
		SOT-23-5	260	
		SOT-23-6	250	
θ_{JC}	Junction-to-Case Resistance in Free Air	TSOT-23-5A	130	°C/W
		TSOT-23-6A	120	
		SOT-23-5	130	
		SOT-23-6	120	

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{IN}	VIN Input Voltage	2.9 ~ 5.5	V
I_{OUT}	VOUT Output Current (For APL3556(C/D))	0 ~ 3	A
	VOUT Output Current(For APL3556(A/B))	0 ~ 2	
	IOUT peak current(<10mS)	5	
R_{ILIM}	Current-limit threshold resistor range	0 ~ 27	kΩ
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=5V, V_{EN}=5V and T_A= -40 to 85°C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions		APL3556 Min.	APL3556 Typ.	APL3556 Max.	Unit
SUPPLY CURRENT							
I_{IN}	VIN Supply Current	NO load, V_{EN}=0V		-	-	1	μA
		NO load, V_{EN}=5V		-	100	150	
	Leakage Current	OUT=GND, V_{EN}=0V		-	-	1	
I_{REV}	Reverse Leakage Current	V_{OUT}=5V, V_{IN}=GND, V_{EN}=0V		-	-	1	
POWER SWITCH							
$R_{DS(ON)}$	Power Switch On Resistance	V_{IN}=5V, I_{OUT}=1A, T_A= 25 °C (For APL3556C/D)		-	50	60	mΩ
		V_{IN}=5V, I_{OUT}=1A, T_A= 25 °C (For APL3556A/B)		-	60	70	mΩ
UNDER-VOLTAGE LOCKOUT(UVLO)							
V_{IN}	VIN UVLO Threshold Voltage	V_{IN} rising, T_A= -40 ~ 85 °C		1.7	-	2.65	V
	VIN UVLO Hysteresis	V_{IN} falling		-	0.2	-	
CURRENT LIMIT							
	Maximum Current-limit set point	R_{ILIM}=OPEN or GND (Note 4)		5.5	6	6.5	A
I_{LIM}	Current Limit Threshold	V_{IN}=2.9V to 5.5V, T_A= -40 ~ 85 °C	R_{ILIM}=4.57k	3.3	3.6	3.9	A
			R_{ILIM}=5.9k	2.4	2.8	3.2	
			R_{ILIM}=10k	1.4	1.7	2	
			R_{ILIM}=13k	1.101	1.295	1.489	
			R_{ILIM}=27k	0.57	0.62	0.67	
T_{IOS}	Response time of over current	V_{IN} = 5V		-	2	-	μs
Output Discharge							
R_{DIS}	Output Discharge Resistor			-	150	-	Ω

Note 4:This specification is not certified

Electrical Characteristics (Cont.)

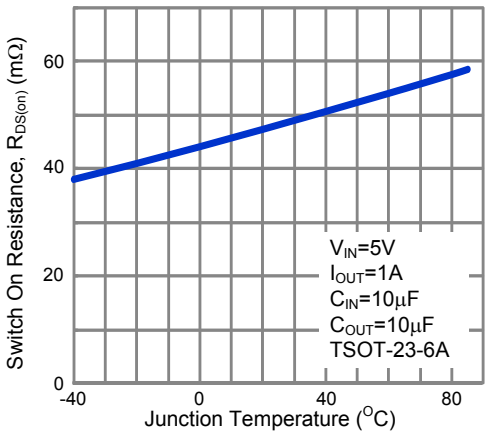
Unless otherwise specified, these specifications apply over V_{IN}=5V, V_{EN}=5V and T_A= -40 to 85°C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APL3556			Unit
			Min.	Typ.	Max.	
FAULT OUTPUT PIN						
V_{FAULT}	FAULT Output Low Voltage	I_{FAULT} =5mA	-	0.2	0.4	V
I_{FAULT}	FAULT Leakage Current	V_{FAULT} =5V	-	-	1	μA
$T_{D(FAULT)}$	FAULT Deglitch Time	FAULT assertion, T_A=-40~85°C	-	12	-	ms
REVERSE VOLTAGE PROTECT						
I_{REV}	Reverse current trip point	Enable reverse current protection	-	200	-	mA
V_{REV}	Reverse voltage comparator trip point	V_{IN} -V_{OUT}, disable reverse current protection	-	25	-	mV
T_{REV}	Time from reverse current condition to MOSFET turn off	V_{IN}=5V	-	5	-	ms
EN INPUT PIN						
V_{IH}	Input Logic High	V_{IN}=2.7V to 5.5V	1.2	-	-	V
V_{IL}	Input Logic Low	V_{IN}=2.7V to 5.5V	-	-	0.4	
I_{EN}	EN Input Current		-	-	1	μA
$T_{D(ON)}$	Turn on Delay Time		-	80	-	μs
$T_{D(OFF)}$	Turn off Delay Time		-	80	-	
T_{SS}	Soft Start Time	No Load, C_{OUT}=1μF, V_{IN}=5V	2	2.5	3	ms
OVERT-TEMPERATURE PROTECTION (OTP)						
T_{OTP}	Over-Temperature Threshold	T_J rising	-	150	-	°C
	Over-Temperature Hysteresis		-	40	-	

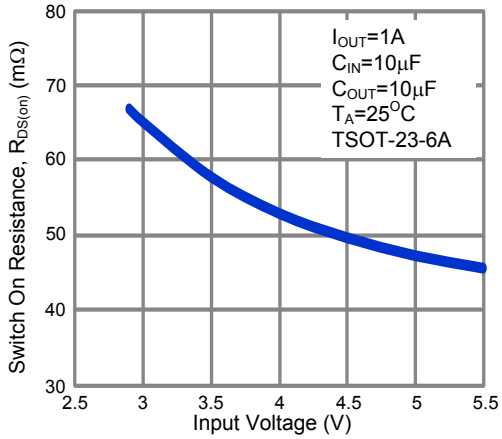
Typical Operating Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=5V, V_{EN}=5V and T_A= -40 to 85°C. Typical values are at T_A=25°C.

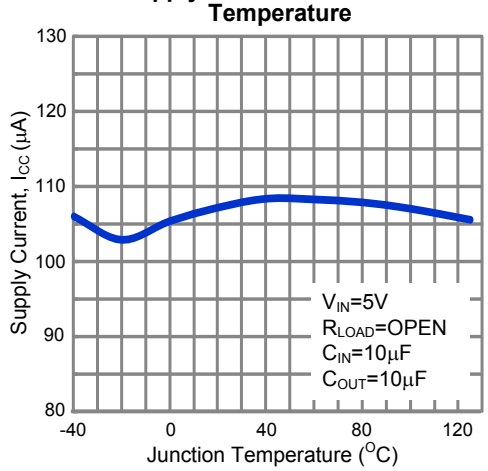
Switch On Resistance vs. Junction Temperature



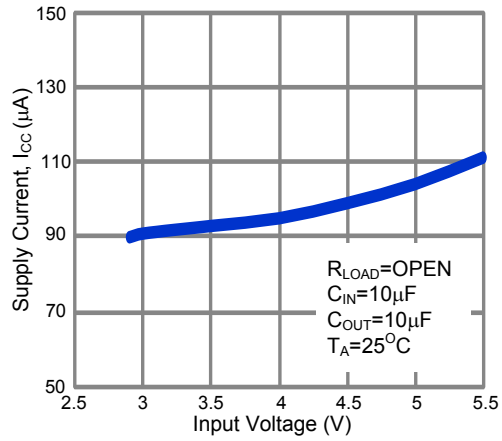
Switch On Resistance vs. Input Voltage



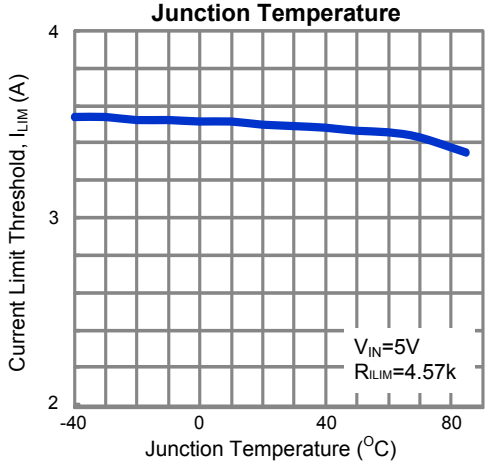
Supply Current vs. Junction Temperature



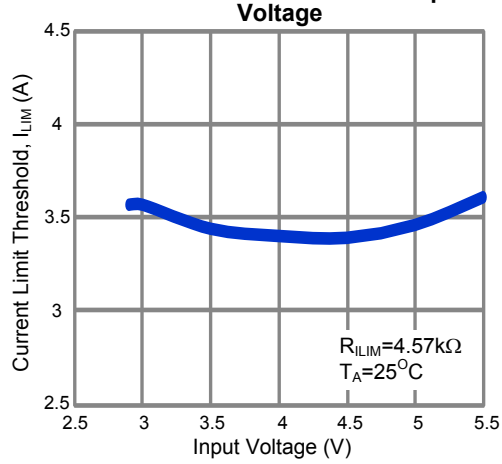
Supply Current vs. Input Voltage



Current Limit Threshold vs. Junction Temperature



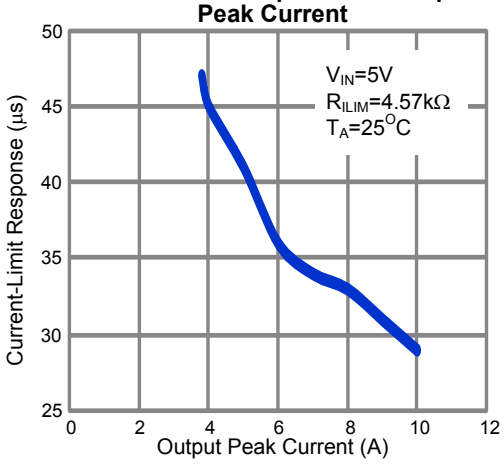
Current Limit Threshold vs. Input Voltage



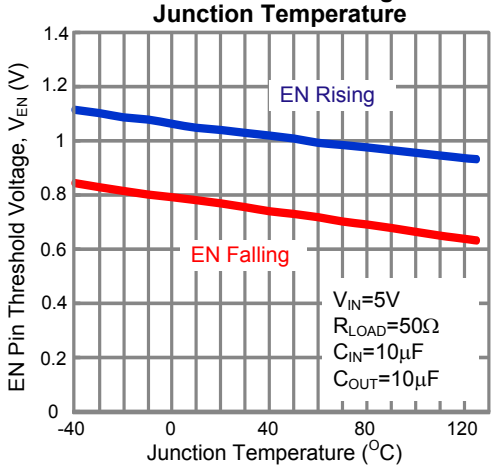
Typical Operating Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{IN}=5V, V_{EN}=5V and T_A= -40 to 85°C. Typical values are at T_A=25°C.

Current-Limit Response vs. Output Peak Current



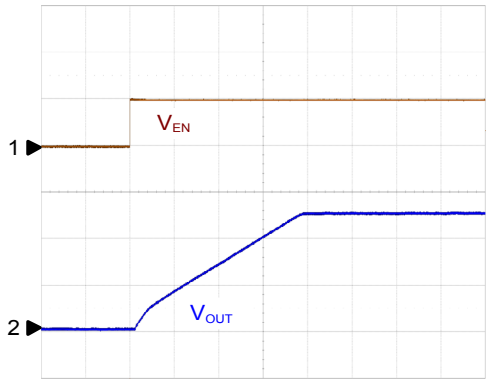
EN Pin Threshold Voltage vs. Junction Temperature



Operating Waveforms

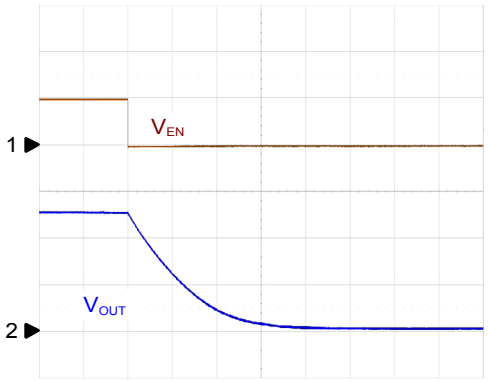
Unless otherwise specified, these specifications apply over V_{IN}=5V, V_{EN}=5V and T_A= -40 to 85°C. Typical values are at T_A=25°C.

Turn On Response



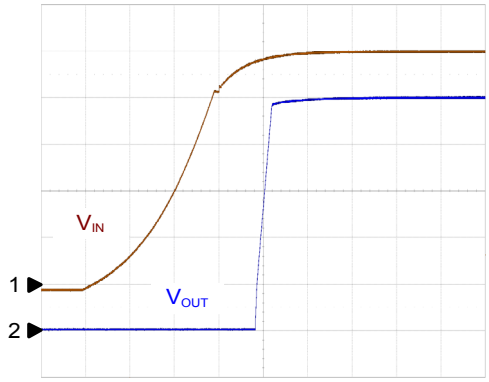
V_{IN}=5V,C_{OUT}=10μF/Electrolytic,
C_{IN}=10μF/Electrolytic,R_{LOAD}=30Ω
CH1:V_{EN},5V/Div, DC
CH2:V_{OUT},2V/Div, DC
TIME:500μs/Div

Turn Off Response



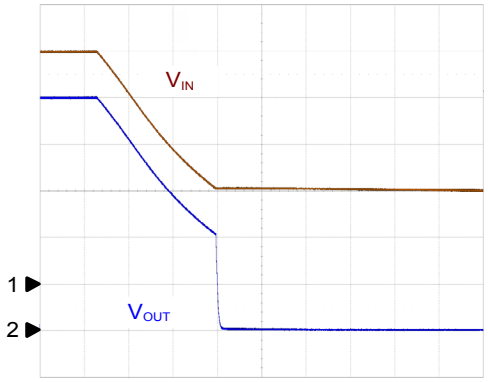
V_{IN}=5V,C_{OUT}=10μF/Electrolytic,
C_{IN}=10μF/Electrolytic,R_{LOAD}=30Ω
CH1:V_{EN},5V/Div, DC
CH2:V_{OUT},2V/Div, DC
TIME:100μs/Div

UVLO at Rising



V_{IN}=5V,C_{OUT}=10μF/Electrolytic,
C_{IN}=10μF/Electrolytic,R_{LOAD}=30Ω
CH1:V_{IN},1V/Div, DC
CH2:V_{OUT},1V/Div, DC
TIME:5ms/Div

UVLO at Falling

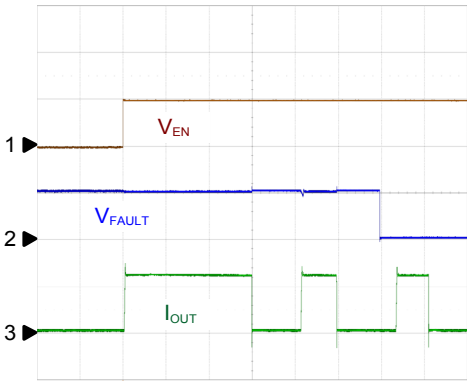


V_{IN}=5V,C_{OUT}=10μF/Electrolytic,
C_{IN}=10μF/Electrolytic,R_{LOAD}=30Ω
CH1:V_{IN},1V/Div, DC
CH2:V_{OUT},1V/Div, DC
TIME:5ms/Div

Operating Waveforms (Cont.)

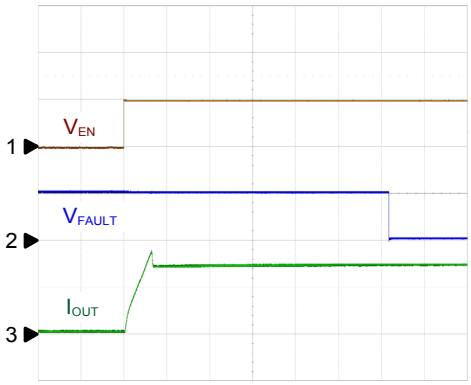
Unless otherwise specified, these specifications apply over V_{IN}=5V, V_{EN}=5V and T_A= -40 to 85°C. Typical values are at T_A=25°C.

FAULT Response During Short Circuit



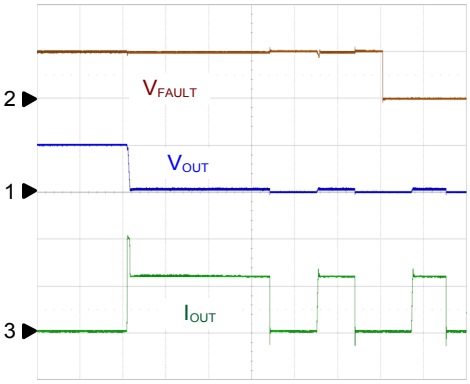
V_{IN}=5V,C_{OUT}=10µF/Electrolytic,
C_{IN}=10µF/Electrolytic,R_{LOAD}=0Ω
CH1:V_{EN},5V/Div, DC
CH2:V_{FAULT},5V/Div, DC
CH3:I_{OUT},2A/Div, DC
TIME:2ms/Div

FAULT Response During Over Load



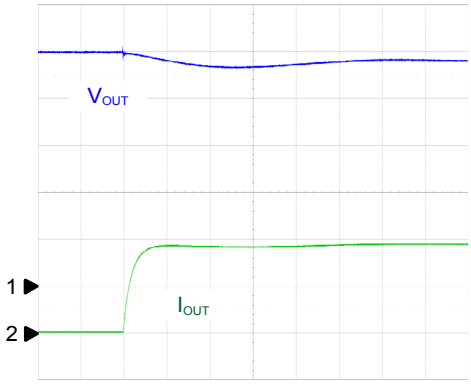
V_{IN}=5V,C_{OUT}=10µF/Electrolytic,
C_{IN}=10µF/Electrolytic,R_{LOAD}=1Ω
CH1:V_{EN},5V/Div, DC
CH2:V_{FAULT},5V/Div, DC
CH3:I_{OUT},2A/Div, DC
TIME:2ms/Div

FAULT Response with Ramped Load



V_{IN}=5V,C_{OUT}=10µF/Electrolytic,
C_{IN}=10µF/Electrolytic
CH1:V_{OUT},5V/Div, DC
CH2:V_{FAULT},5V/Div, DC
CH3:I_{OUT},2A/Div, DC
TIME:2ms/Div

Load-Transient Response

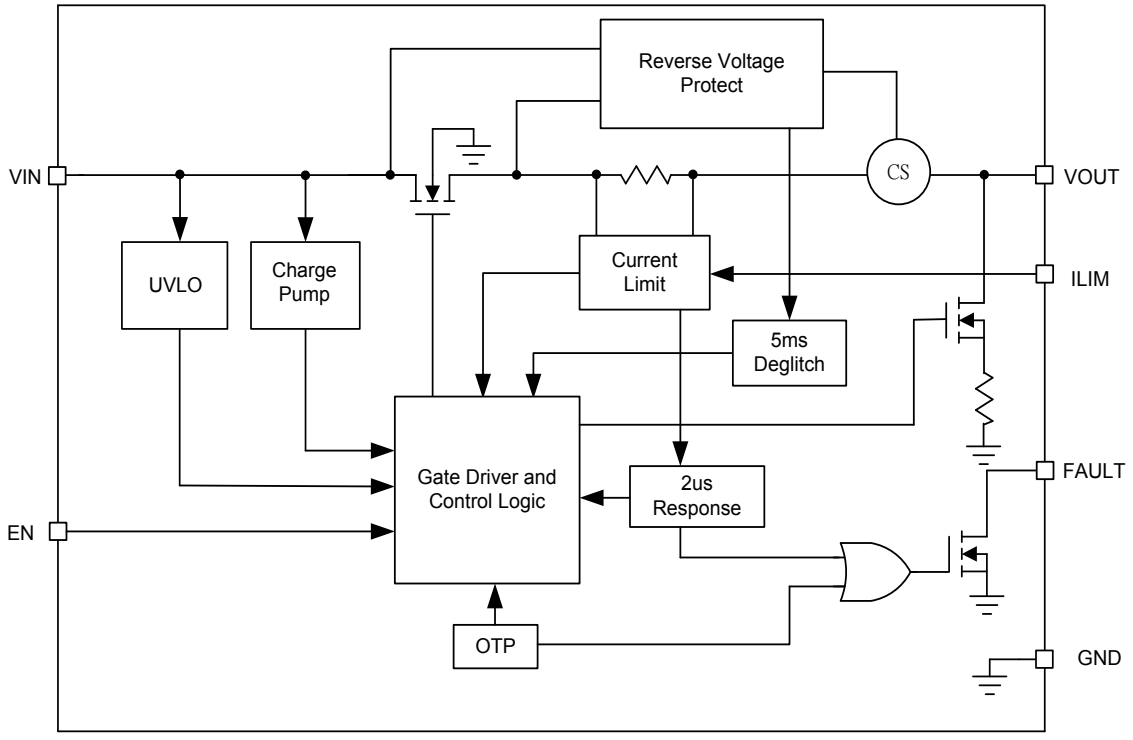


V_{IN}=5V,C_{OUT}=10µF/Electrolytic,
C_{IN}=10µF/Electrolytic,I_{OUT}=0 to 2A
CH1:V_{OUT},1V/Div, DC
CH2:I_{OUT},1A/Div, DC
TIME:2µs/Div

Pin Description

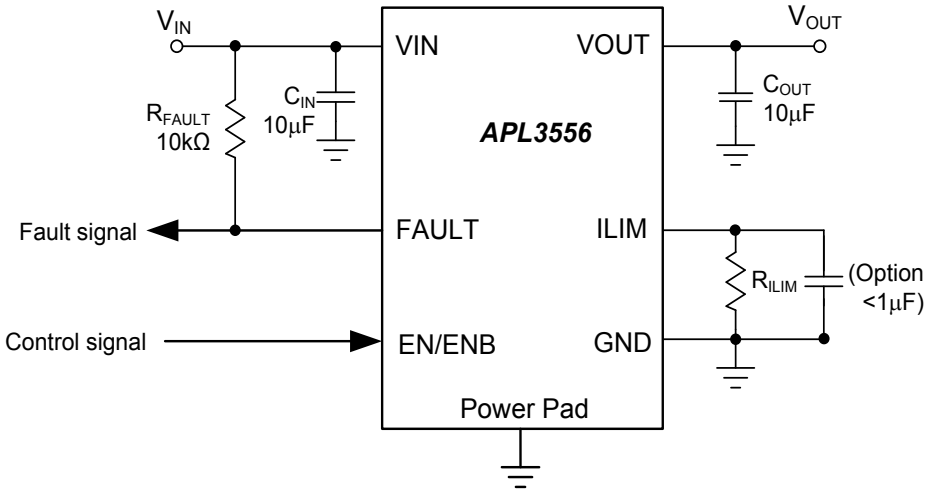
PIN			FUNCTION
NO.		NAME	
TSOT23-6A SOT-23-6 (56A/C)	TSOT23-5A SOT-23-5 (56B/D)		
1	1	VOUT	Output Voltage Pin. The output voltage follows the input voltage. When the device is enable.
5	4	ILIM	External resistor used to set current-limit threshold.
4	-	FAULT	Fault Indication Pin. This pin goes low when a current limit or a reverse voltage condition is detected after a 12ms deglitch time.
3	3	EN	Enable Input. Pulling this pin to high will enable the device and pulling this pin to low will disable device. The EN pin cannot be left floating.
2	2	GND	Ground.
6	5	VIN	Power Supply Input. Connect this pin to external DC supply.

Block Diagram

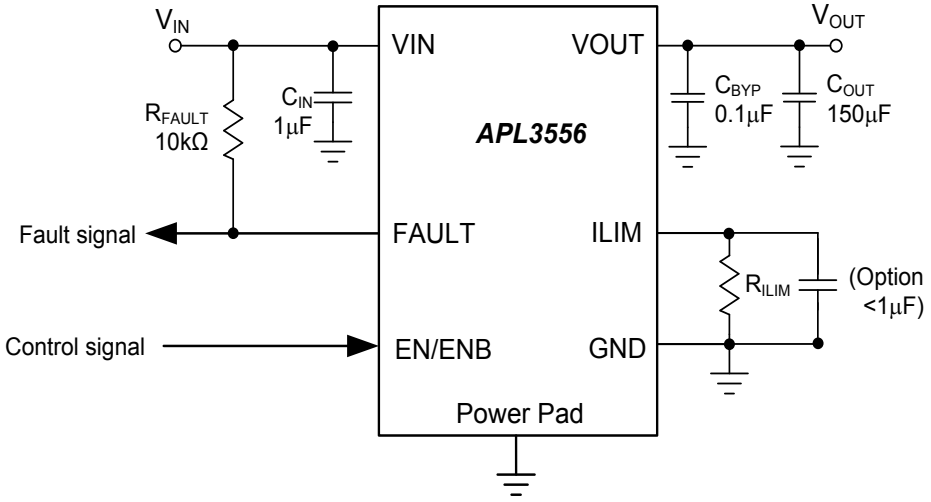


Typical Application Circuit

Circuit 1.



Circuit 2.



Note: The C_{IN} is typically 1μF. However, the parasitic inductance before VIN pin could cause voltage spike to damage internal circuitry. If voltage spike, especially during short circuit or hot plug-in of large capacitance load, on VIN exceeds VIN's absolute maximum rating, adding at least 10μF/MLCC capacitor at VIN is strongly recommended.

Parameter Measurement Information

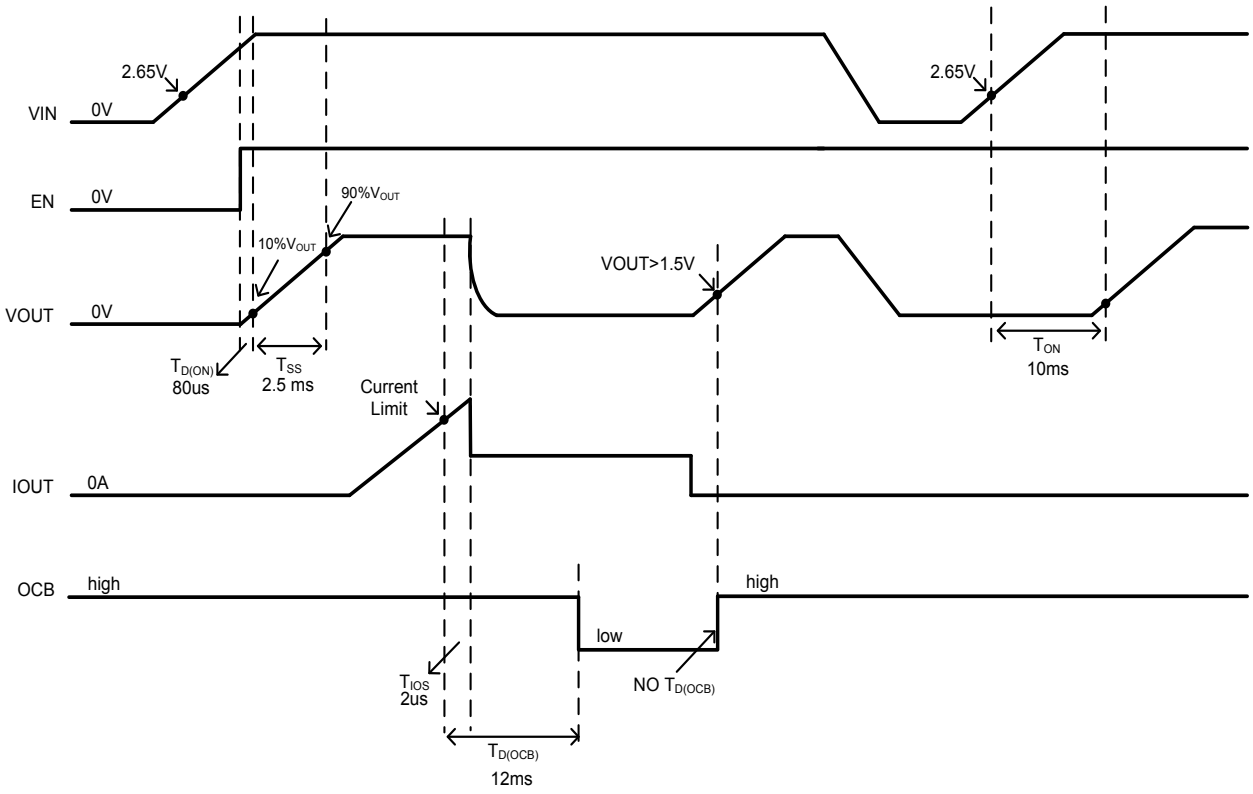


Figure 1. Sequence of Power On & Current Limit & OCB Indicate

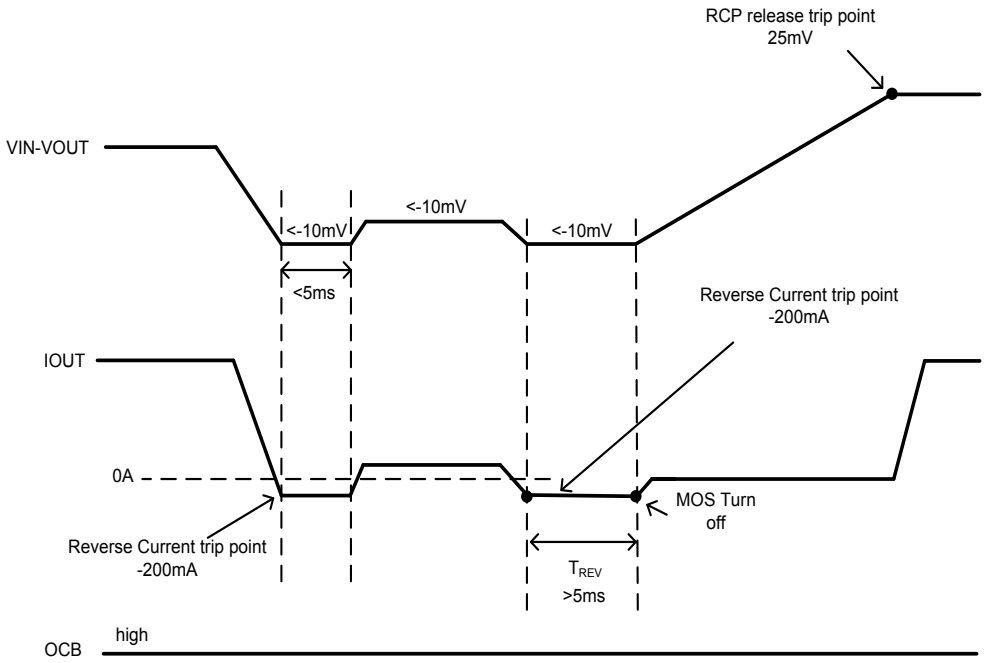


Figure 2. Reverse Current trip point & Recovery

Function Description

VIN Under-Voltage Lockout (UVLO)

The APL3556 series of power switches have a built-in under-voltage lockout circuit to keep the output shutting off until internal circuitry is operating properly. The UVLO circuit has hysteresis and a de-glitch feature so that it will typically ignore undershoot transients on the input. When input voltage exceeds the UVLO threshold, the output voltage starts a soft-start to reduce the inrush current.

Power Switch

The power switch is an N-channel MOSFET with a low $R_{DS(ON)}$. The internal power MOSFET does not have the body diode. When IC is off, the MOSFET prevents a current flowing from the VOUT back to VIN and VIN to VOUT.

Current-Limit Protection

The APL3556 series of power switches provide the current-limit protection function. The adjustable current limit threshold of APL3556 is user programmable via an external resistor. The recommended 1% resistor range for RILIM is 2.7kΩ<RILIM<27kΩ to ensure stability of the internal regulation loop.

Current Limit Threshold Equations (I_{OS}):
$I_{OS(NOM)}$(A)=16700/Rilim
Where 2.7kΩ<R_{ILIM}<27kΩ

FAULT Output

The APL3556 series of power switches provide an opendrain output to indicate that a fault has occurred. When any of current-limit or over-temperature protection occurs for a deglitch time of $t_{D(FAULT)}$, the FAULT goes low. If fault condition release, FAULT will goes high when VOUT > 1.5V (see Figure 1). Since the FAULT pin is an open-drain output, connecting a resistor to a pull high voltage is necessary.

Enable/Disable

Pull the EN below 0.4V will disable the device, and pull EN above 1.2V will enable the device. When the IC is disabled, the supply current is reduced to less than 1uA. The enable input is compatible with both TTL and CMOS logic levels. The EN pin cannot be left floating.

Reverse-Voltage Protection

The reverse voltage protection feature turns off the Nchannel MOSFET when a reverse current of (VOUT - VIN)/$R_{DS(on)}$) over 200mA(typ.) for 5ms (typ) deglitch time(see Figure 2). The APL3556 device allows the N-channel MOSFET immediately turn on once the output voltage goes lower than the input voltage by 25 mV (typ) (see Figure 2). This prevents damage to devices on the input side of the APL3556 by preventing significant current from sinking into the input capacitance.

Over-Temperature Protection

When the junction temperature exceeds 150°C, the internal thermal sense circuit turns off the power FET and allows the device to cool down. When the device's junction temperature cools by 40°C, the internal thermal sense circuit will enable the device, resulting in a pulsed output during continuous thermal protection. Thermal protection is designed to protect the IC in the event of over temperature conditions. For normal operation, the junction temperature cannot exceed T_J=+125°C.

Application Information

Input Capacitor

A 10uF or higher ceramic bypass capacitor from VIN to GND, located near the APL35556, is strongly recommended to suppress the ringing during short circuit fault event. When the load current trips the SCP threshold in an over load condition such as a short circuit, hot plug-in or heavy load transient the IC immediately turns off the internal power switch that will cause VIN ringing due to the inductance between power source and VIN. Without the bypass capacitor, the output short may cause sufficient ringing on the input to damage internal control circuitry. Input capacitor is especially important to prevent VIN from ringing too high in some applications where the inductance between power source to VIN is large (ex, an extra bead is added between power source line to VIN for EMI reduction), additional input capacitance may be needed on the input to reduce voltage overshoot from exceeding the absolute maximum voltage of the device during over load conditions.

Output Capacitor

A low-ESR 150μF aluminum electrolytic between OUT and GND is strongly recommended to reduce the voltage droop during hot-attachment of downstream peripheral. Higher-value output capacitor is better when the output load is heavy. Additionally, bypassing the output with a 0.1μF ceramic capacitor improves the immunity of the device to short-circuit transients.

Layout Consideration

The PCB layout should be carefully performed to maximize thermal dissipation and to minimize voltage drop, droop and EMI. The following guidelines must be considered:

1.Please place the input capacitors near the IN pin as close as possible.

2.Output decoupling capacitors for load must be placed near the load as close as possible for decoupling high frequency ripples.

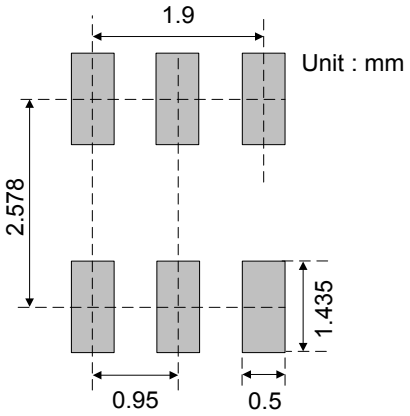
3.Locate APL3556 and output capacitors near the load to reduce parasitic resistance and inductance for excellent load transient performance.

4.The negative pins of the input and output capacitors and the GND pin must be connected to the ground plane of the load.

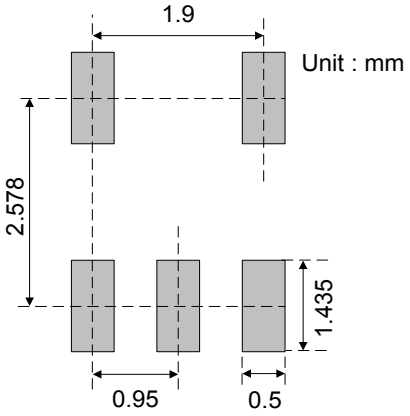
5.Keep IN and OUT traces as wide and short as possible.

6.The traces routing the R_{ILIM} resistor to the APL3556 should be as short as possible to reduce parasitic effects on the current limit accuracy.

Recommended Minimum Footprint



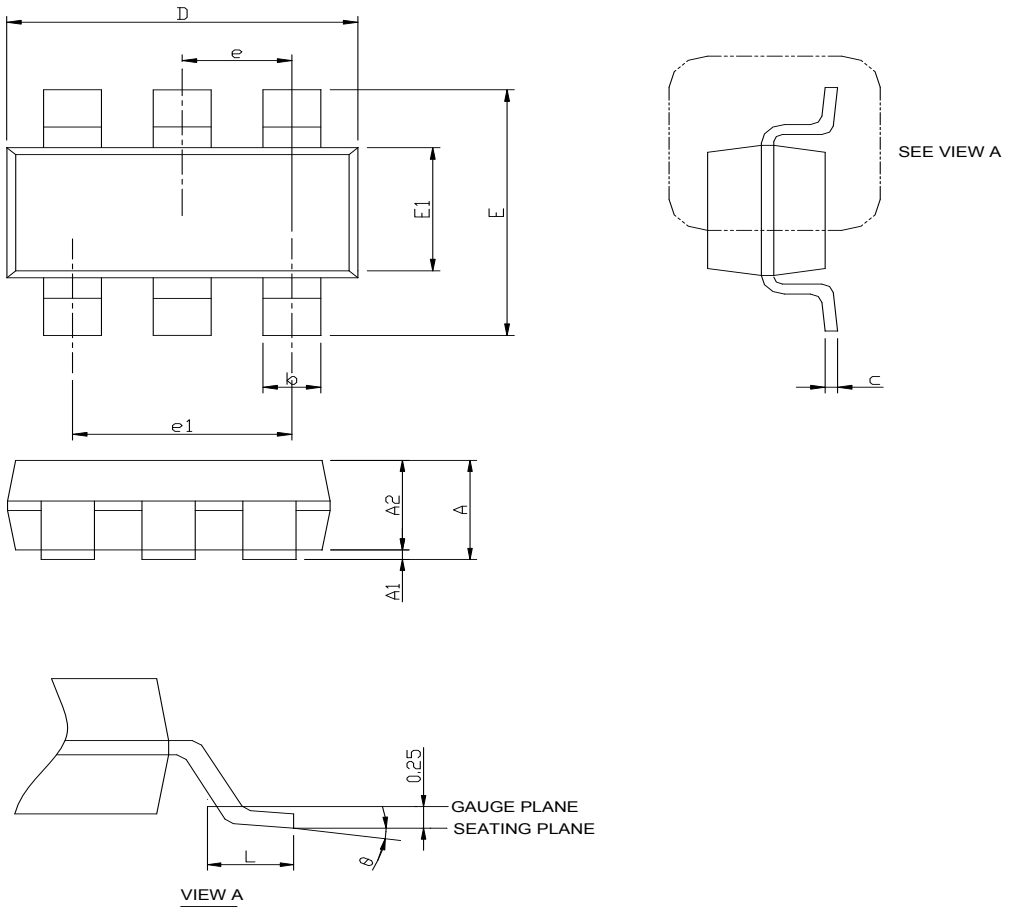
TSOT-23-6A
SOT-23-6



TSOT-23-5A
SOT-23-5

Package Information

TSOT-23-6A

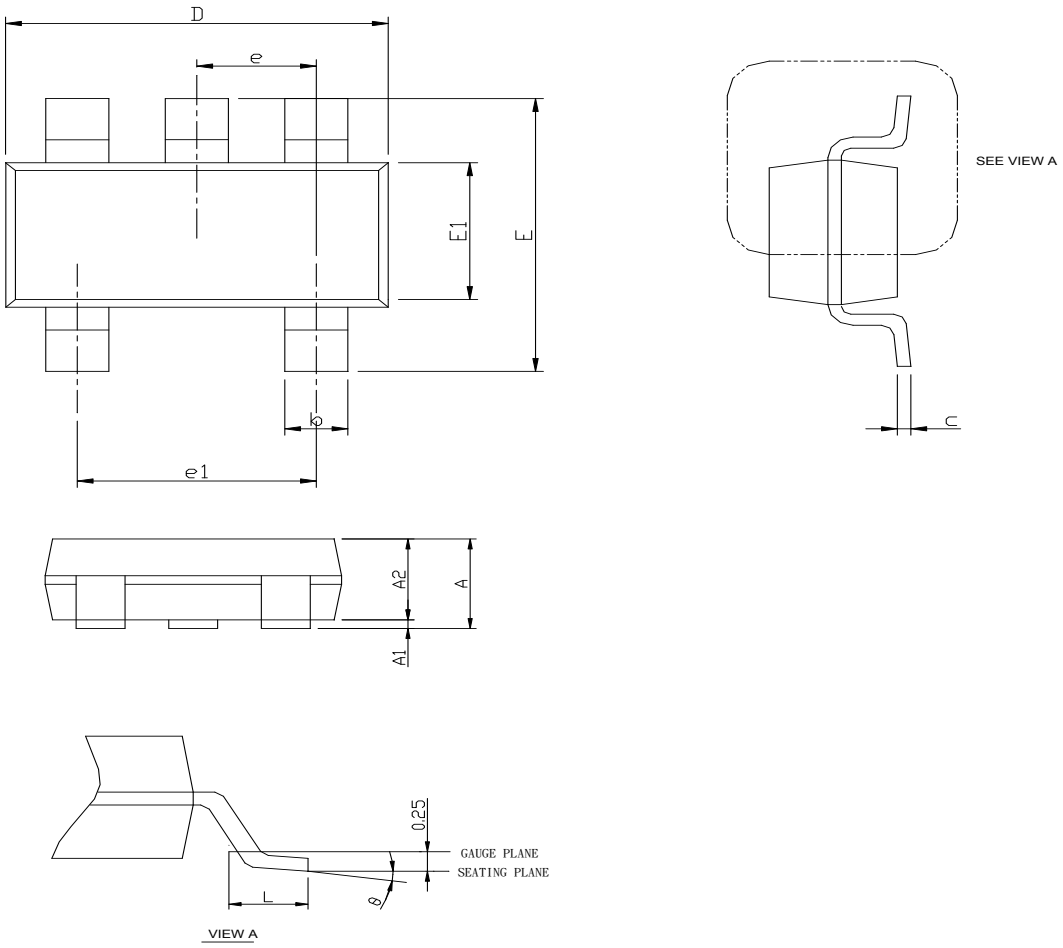


SYMBOL	TSOT-23-6A			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	1.00	0.028	0.039
A1	0.01	0.10	0.000	0.004
A2	0.70	0.90	0.028	0.035
b	0.30	0.50	0.012	0.020
c	0.08	0.20	0.003	0.008
D	2.70	3.10	0.106	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

Note : 1. Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

Package Information

TSOT-23-5A

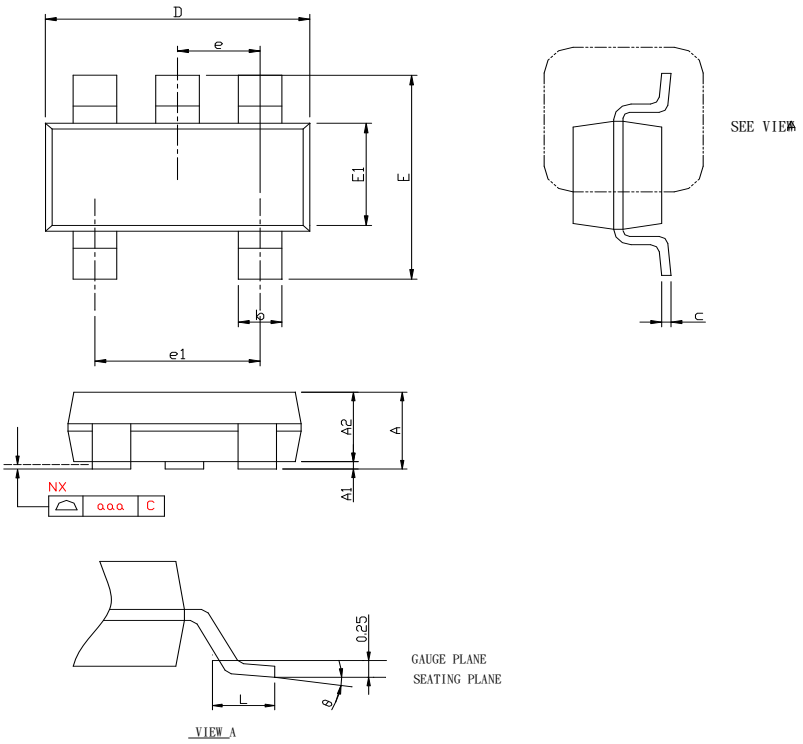


SYMBOL	TSOT-23-5A			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	1.00	0.028	0.039
A1	0.01	0.10	0.000	0.004
A2	0.70	0.90	0.028	0.035
b	0.30	0.50	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.70	3.10	0.106	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

Note : 1. Followed from JEDEC TO-178 AA.
2. Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

Package Information

SOT-23-5

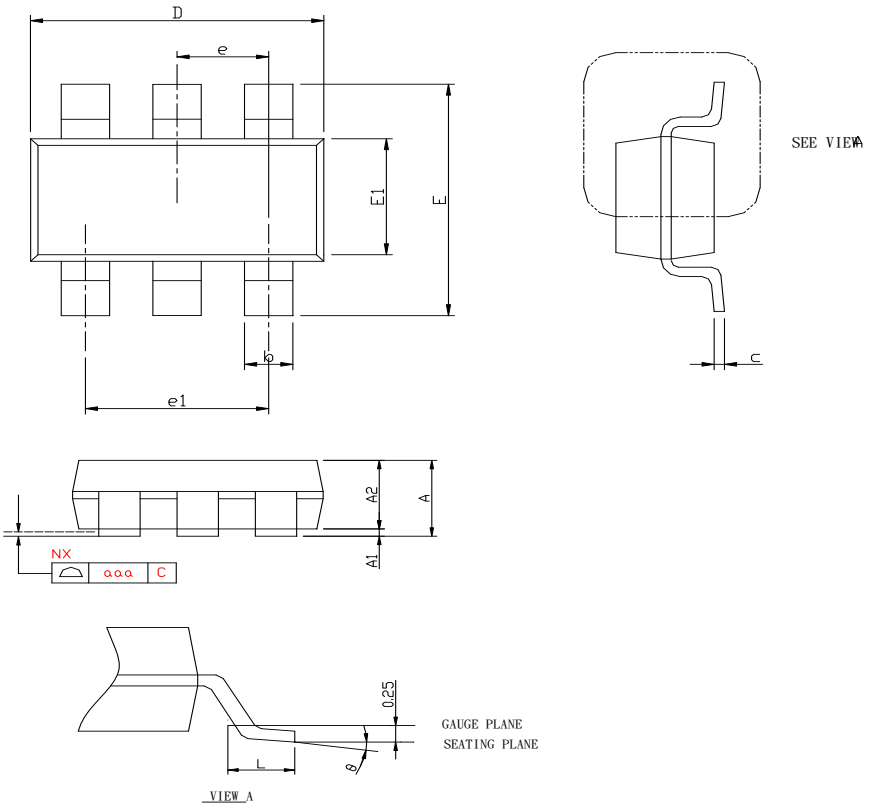


SYMBOL	SOT-23-5					
	MILLIMETERS			INCHES		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A		1.16	1.45		0.046	0.057
A1	0.00	0.05	0.15	0.000	0.002	0.006
A2	0.90	1.10	1.30	0.035	0.043	0.051
b	0.30	0.38	0.50	0.012	0.015	0.020
c	0.08	0.17	0.22	0.003	0.007	0.009
D	2.70	2.93	3.10	0.106	0.115	0.122
E	2.60	2.83	3.00	0.102	0.111	0.118
E1	1.40	1.60	1.80	0.055	0.063	0.071
e	0.95 BSC			0.037BSC		
e1	1.90 BSC			0.075BSC		
K	0.30	0.45	0.60	0.012	0.018	0.024
θ	0°	4°	8°	0°	4°	8°
aaa	0.10			0.004		

Note : 1. Followed from JEDEC TO-178 AA.
2. Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

Package Information

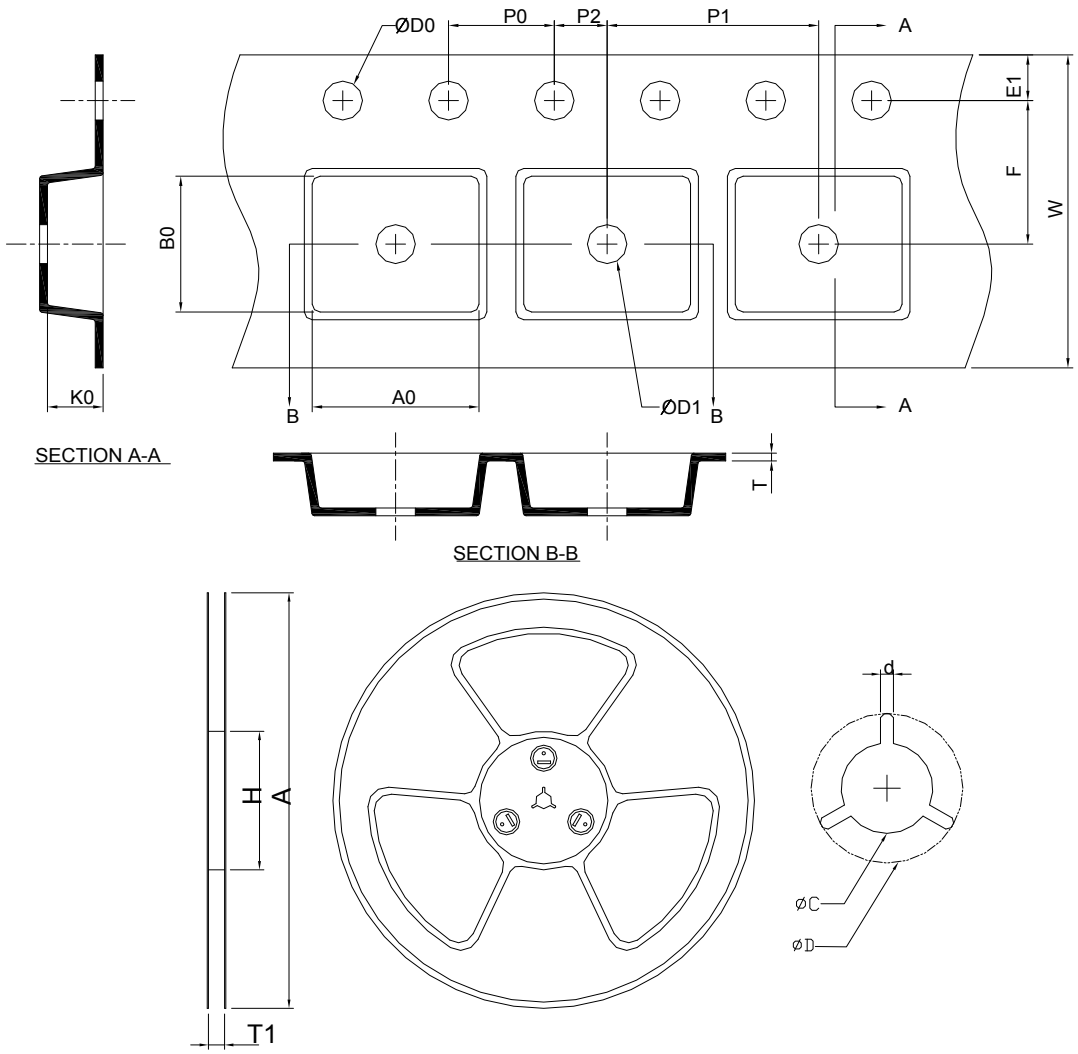
SOT-23-6



SYMBOL	SOT-23-6					
	MILLIMETERS			INCHES		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A		1.16	1.45		0.046	0.057
A1	0.00	0.05	0.15	0.000	0.002	0.006
A2	0.90	1.10	1.30	0.035	0.043	0.051
b	0.30	0.38	0.50	0.012	0.015	0.020
c	0.08	0.17	0.22	0.003	0.007	0.009
D	2.70	2.93	3.10	0.106	0.115	0.122
E	2.60	2.83	3.00	0.102	0.111	0.118
E1	1.40	1.60	1.80	0.055	0.063	0.071
e	0.95 BSC			0.037BSC		
e1	1.90 BSC			0.075BSC		
K	0.30	0.45	0.60	0.012	0.018	0.024
θ	0°	4°	8°	0°	4°	8°

Note : 1. Followed from JEDEC TO-178 AB.
2. Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TSOT 23-6(A)	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.0 MIN.	0.6+0.00 -0.40	3.20±0.20	3.10±0.20	1.20±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
TSOT 23-5A	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.0 MIN.	0.6+0.00 -0.40	3.20±0.20	3.10±0.20	1.20±0.20

Carrier Tape & Reel Dimensions

SOT-23-5	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.0 MIN.	0.6+0.00 -0.40	3.20±0.20	3.10±0.20	1.50±0.20
SOT-23-6	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.0 MIN.	0.6+0.00 -0.40	3.20±0.20	3.10±0.20	1.50±0.20

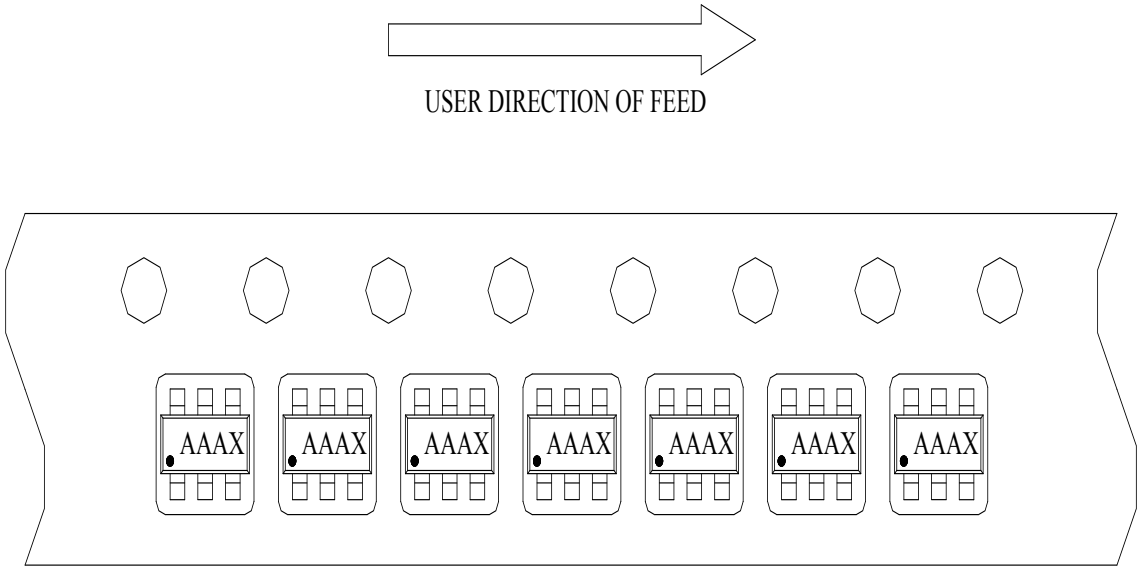
(mm)

Devices Per Unit

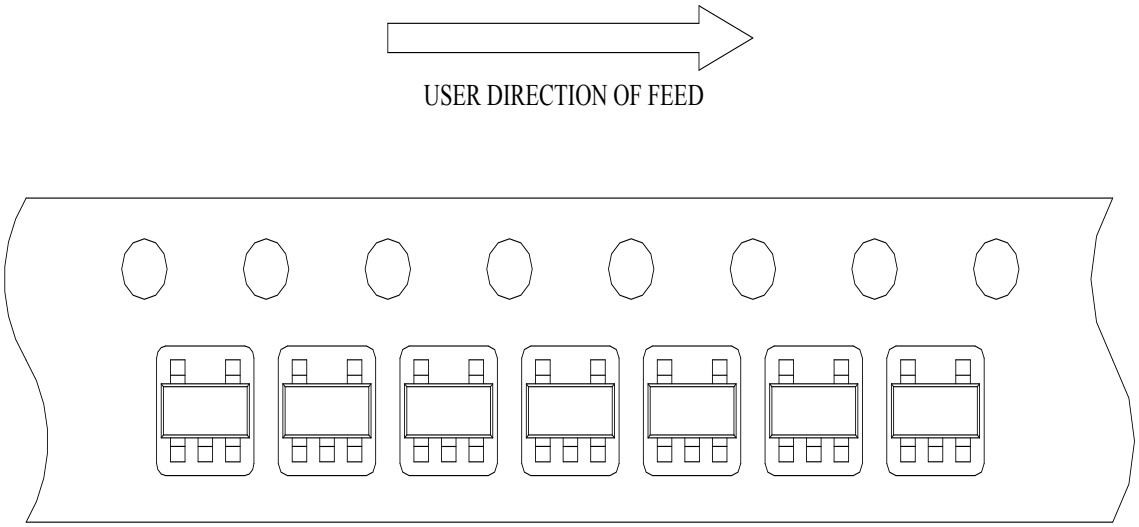
Package type	Packing	Quantity
TSOT-23-6(A)	Tape & Reel	3000
TSOT-23-5A	Tape & Reel	3000
SOT-23-5	Tape & Reel	3000
SOT-23-6	Tape & Reel	3000

Taping Direction Information

TSOT-23-6A

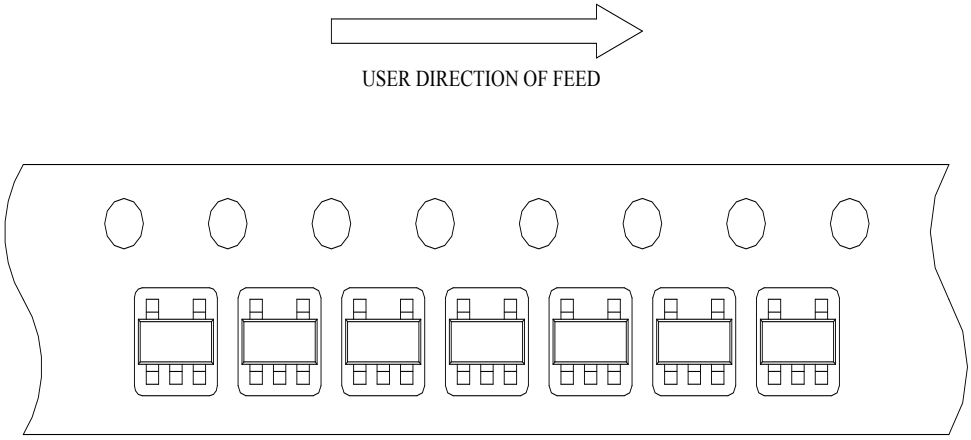


TSOT-23-5A

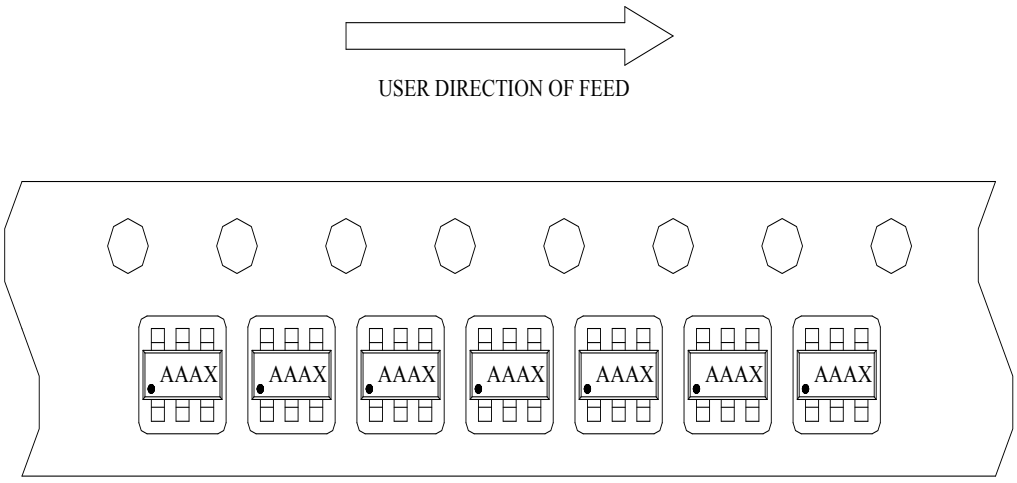


Taping Direction Information

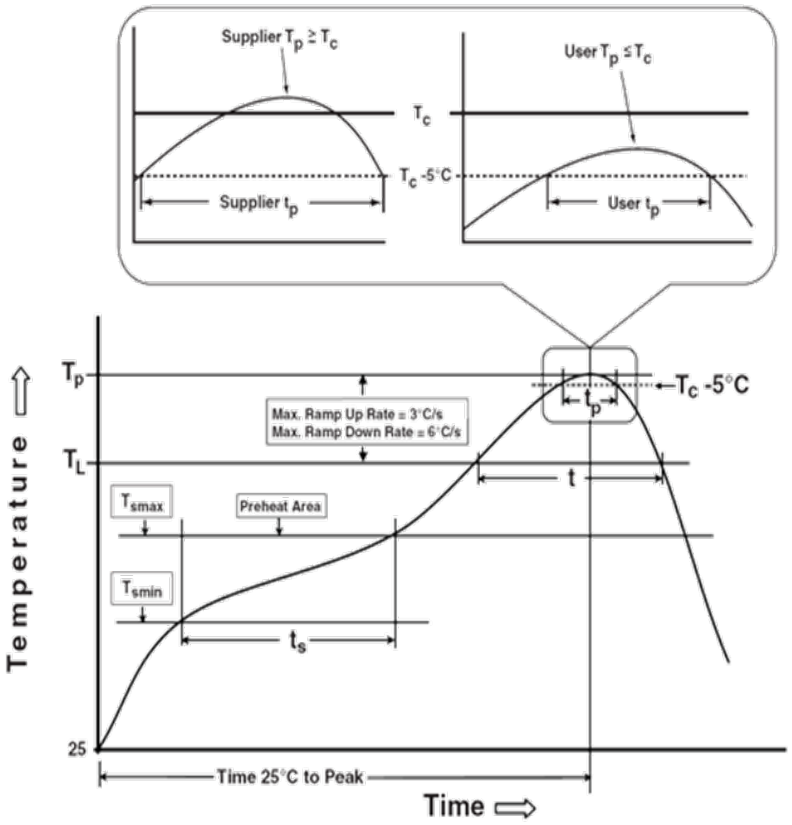
SOT-23-5



SOT-23-6



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≧ 2KV
MM	JESD-22, A115	VMM ≧ 200V
Latch-Up	JESD 78	10ms, 1_{tr} ≧ 100mA

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