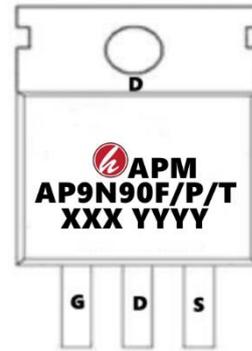
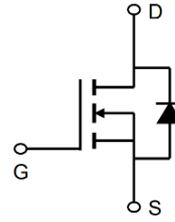


## 900V N-Channel Enhancement Mode MOSFET

### Description

The AP9N90F/T/P is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.



### General Features

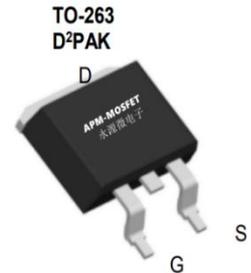
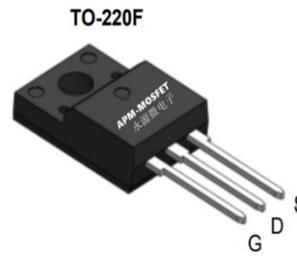
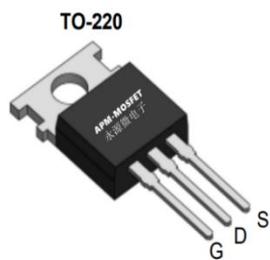
$V_{DS} = 900V$   $I_D = 9A$

$R_{DS(ON)} < 1000m\Omega$  @  $V_{GS}=10V$  (Type: **920mΩ**)

### Application

Uninterruptible Power Supply(UPS)

Power Factor Correction (PFC)



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP9N90F	TO-220F-3L	AP9N90F XXX YYYY	1000
AP9N90P	TO-220-3L	AP9N90P XXX YYYY	1000
AP9N90T	TO-263-3L	AP9N90T XXX YYYY	800

### Absolute Maximum Ratings ( $T_c=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Value	Units
$V_{DSS}$	Drain-Source Voltage	900	V
$V_{GS}$	Gate-Source Voltage	$\pm 30$	V
$I_D @ T_c=25^\circ C$	Drain Current, $V_{GS} @ 10V$	9	A
$I_D @ T_c=100^\circ C$	Drain Current, $V_{GS} @ 10V$	5.8	A
IDM	Drain Current - Pulsed	36	A
EAS	Single Pulsed Avalanche Energy	576	mJ
IAR	Avalanche Current	9	A
EAR	Repetitive Avalanche Energy	53	mJ
dv/dt	Peak Diode Recovery dv/dt	5	V/ns
$P_D$	Power Dissipation	31.2	W
$T_J, T_{stg}$	Operating and Storage Temperature Range	-55 to +150	$^\circ C$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	4.0	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	48.0	$^\circ C/W$

## 900V N-Channel Enhancement Mode MOSFET

### Electrical Characteristics (T<sub>J</sub>=25°C, unless otherwise noted)

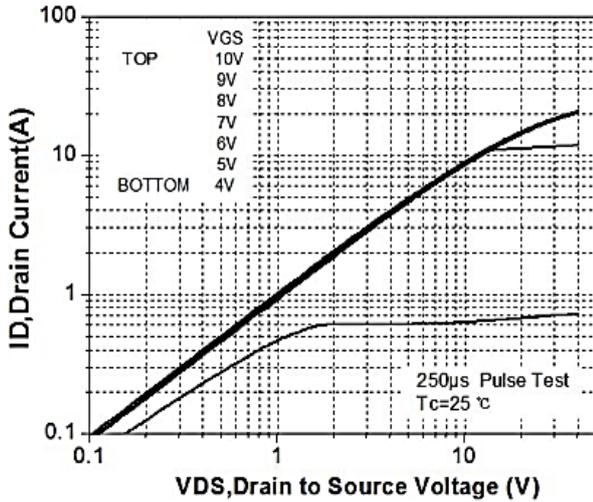
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	900	1000		V
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> =250μA, Referenced to 25°C		0.74		V/°C
IDSS	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 900 V, V <sub>GS</sub> = 0 V			1	μA
IDSS	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 720 V, TC = 125°C			10	μA
IGSSF	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V			100	nA
IGSSR	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V			-100	nA
VGS(TH)	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250 uA	2.0		4.0	V
RDS(On)	Drain-Source On-state Resistance	V <sub>GS</sub> =10 V, I <sub>D</sub> =4.5 A,		975	1200	mΩ
gFS	Forward Transconductance	V <sub>DS</sub> = 40 V, I <sub>D</sub> = 4.5 A		11		S
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =25 V, V <sub>GS</sub> =0V, f=1.0 MHz		2752		pF
C <sub>oss</sub>	Output Capacitance			206		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			36		pF
td(on)	Turn On Delay Time	V <sub>DD</sub> =450 V, I <sub>D</sub> =9A, R <sub>G</sub> =25Ω		33		ns
t <sub>r</sub>	Rising Time			57		ns
td(off)	Turn Off Delay Time			270		ns
t <sub>f</sub>	Fall Time			91		ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =450V, I <sub>D</sub> =9A, V <sub>GS</sub> =10V		80		nC
Q <sub>gs</sub>	Gate-Source Charge			12		nC
Q <sub>gd</sub>	Gate-Drain Charge			38		nC
ISM	Maximum Pulsed Drain-Source Diode Forward Current				36	A
V <sub>SD</sub>	Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 9 A			1.4	V
trr	Reverse Recovery Time	V <sub>GS</sub> =0V, I <sub>S</sub> =9A, dI <sub>F</sub> /dt=100 A/μs		533		ns
Q <sub>rr</sub>	Reverse Recovery Charge	Note4)		6.2		μC

#### Note :

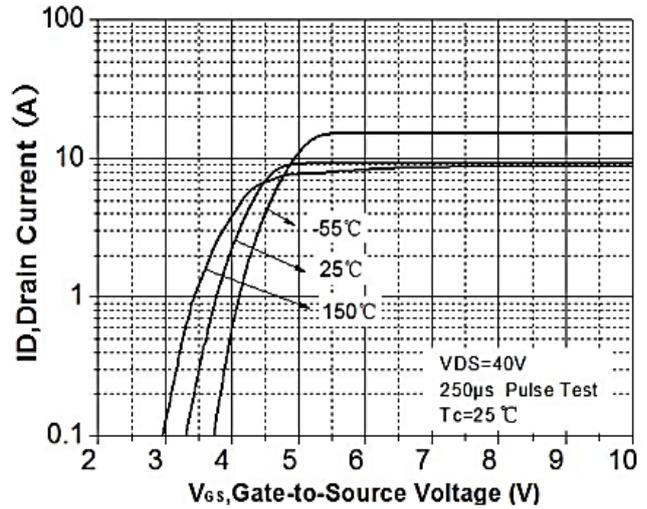
- 1、 The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2、 The EAS data shows Max. rating . L=4.1Mh IAS=18A, VDD=50V, RG=25Ω, Starting T<sub>J</sub> = 25 °C
- 3、 The test condition is Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%
- 4、 The power dissipation is limited by 150°C junction temperature
- 5、 The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

**900V N-Channel Enhancement Mode MOSFET**

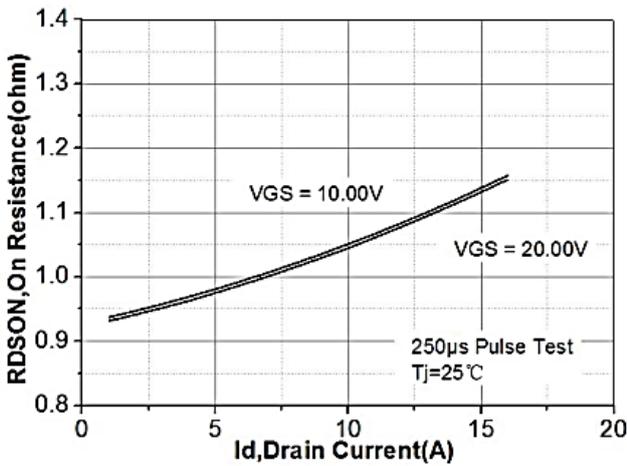
**Typical Characteristics**



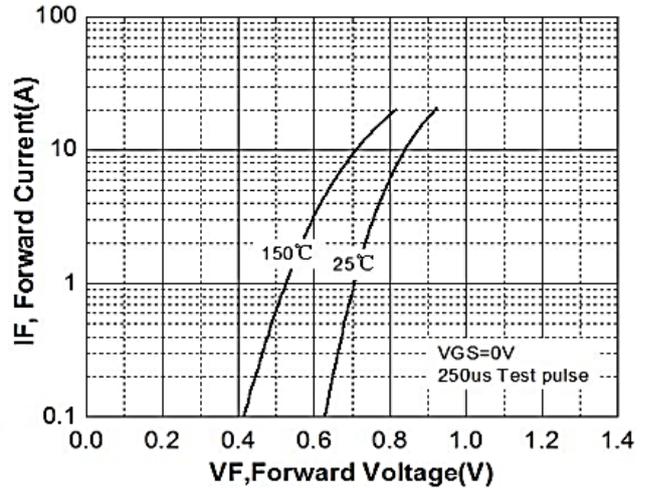
**Figure 1. On-Region Characteristics**



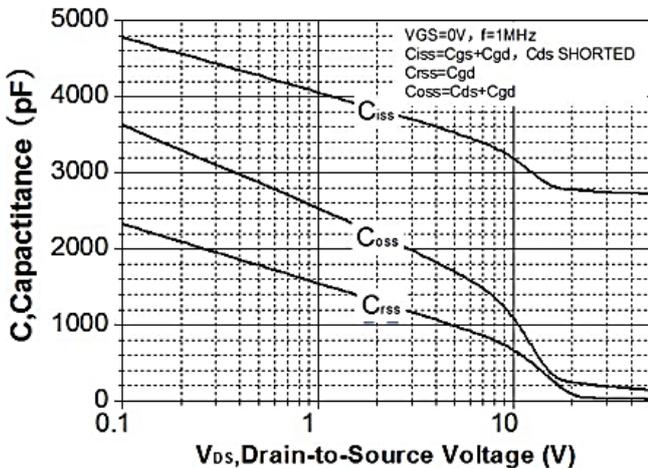
**Figure 2. Transfer Characteristics**



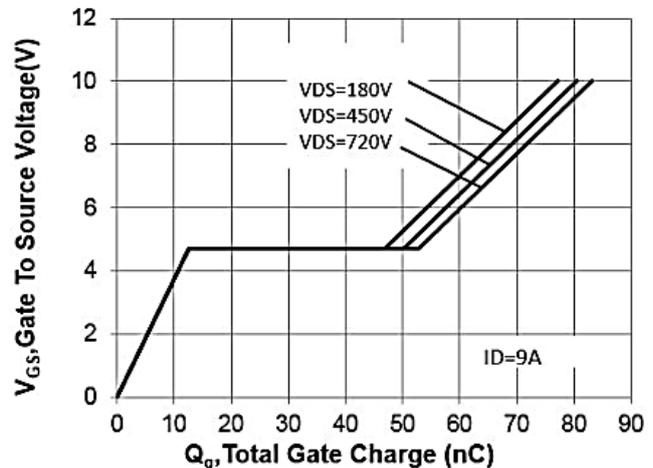
**Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage**



**Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature**

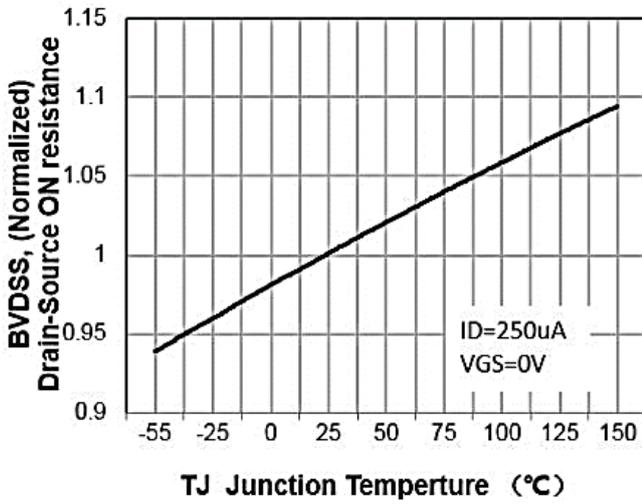


**Figure 5. Capacitance Characteristics**

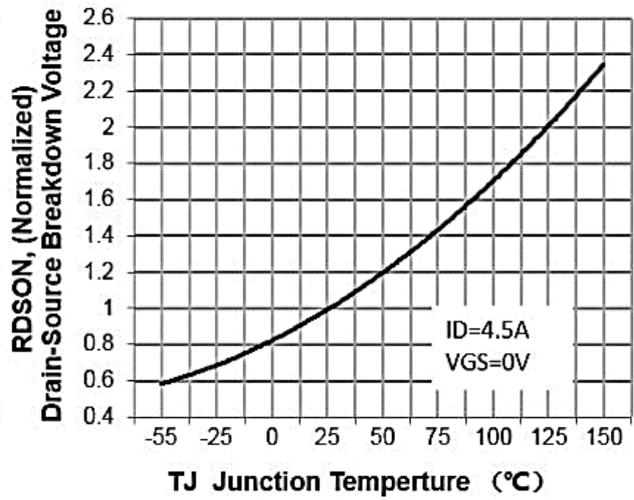


**Figure 6. Gate Charge Characteristics**

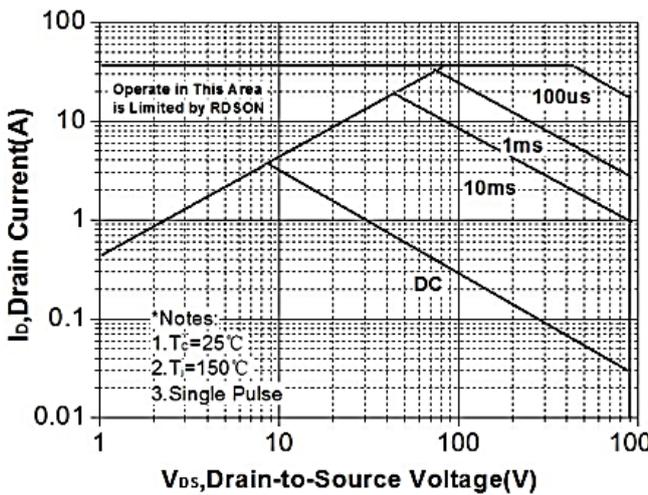
**900V N-Channel Enhancement Mode MOSFET**



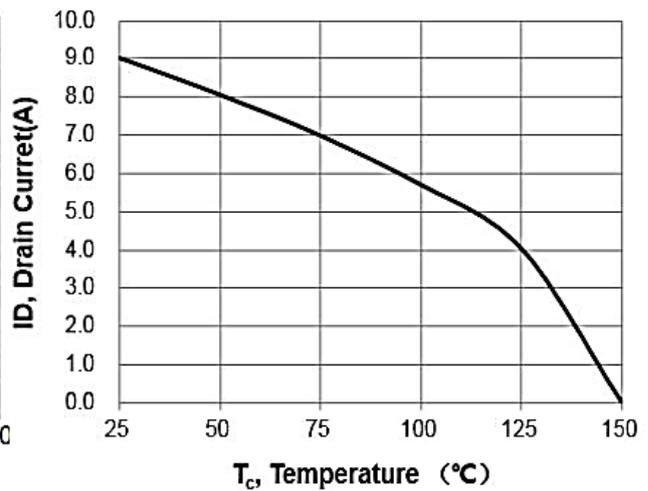
**Figure 7. Breakdown Voltage Variation vs Temperature**



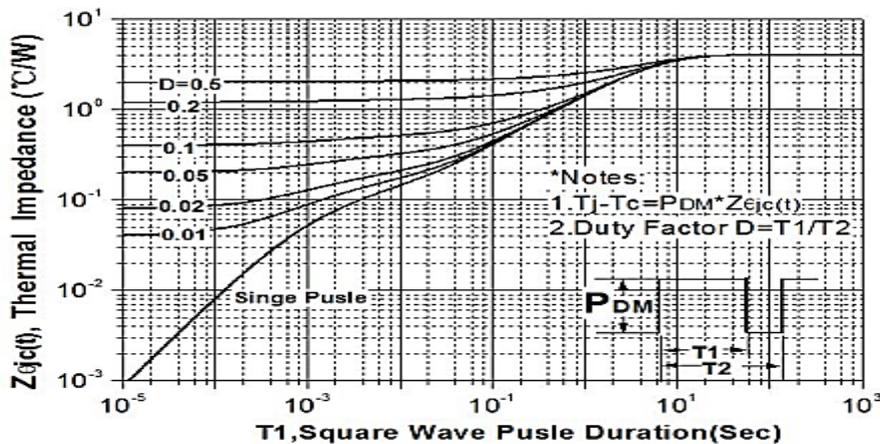
**Figure 8. On-Resistance Variation vs Temperature**



**Figure 9. Maximum Safe Operating Area**



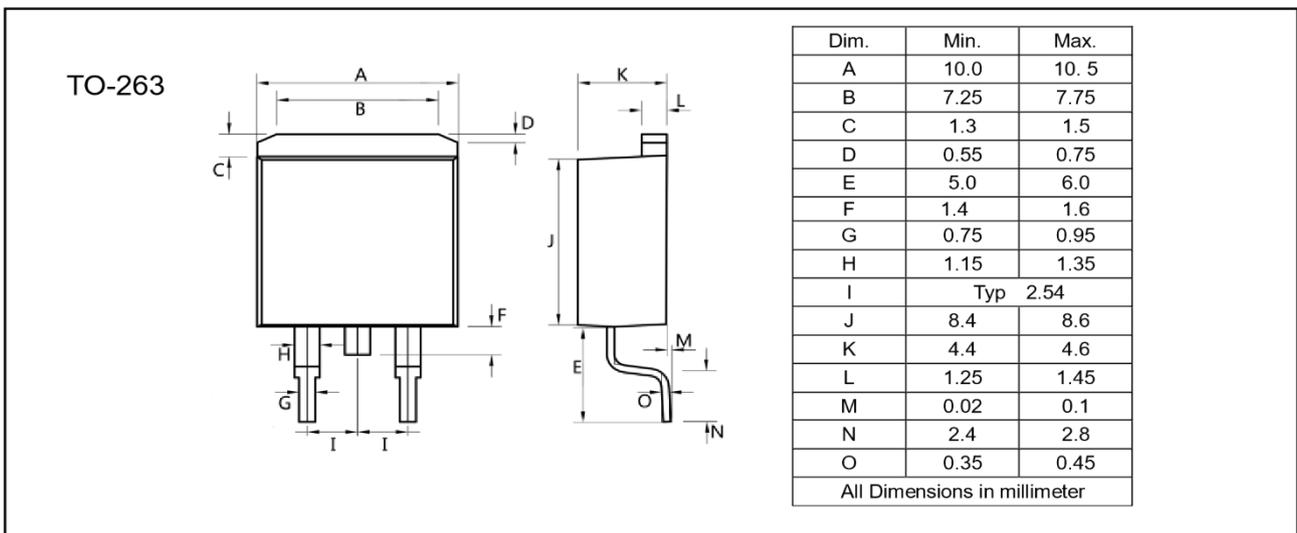
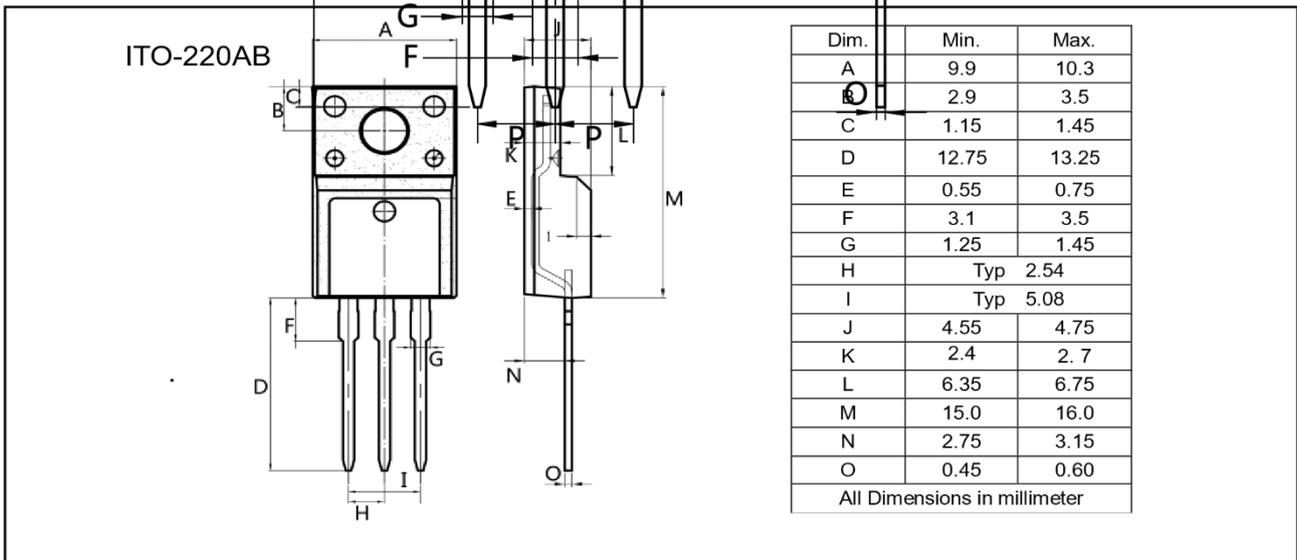
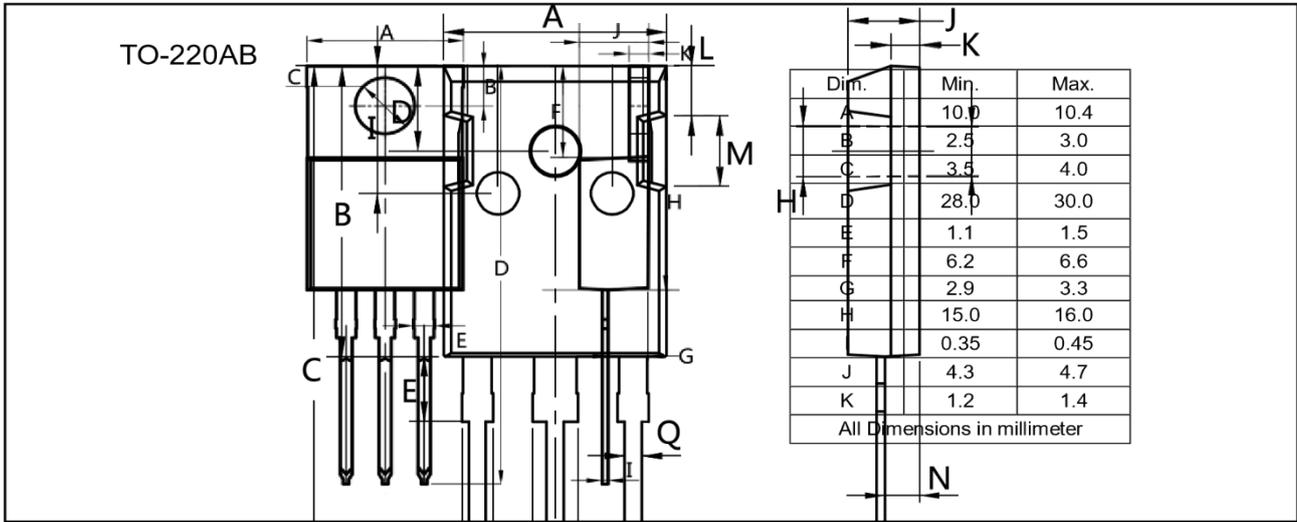
**Figure 10. Maximum Drain Current vs Case Temperature**



**Figure 11. Transient Thermal Response Curve**

**900V N-Channel Enhancement Mode MOSFET**

**Package Mechanical Data-TO-247-3L**



**900V N-Channel Enhancement Mode MOSFET****Attention**

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