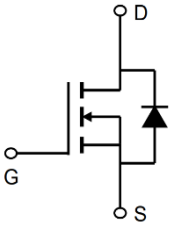
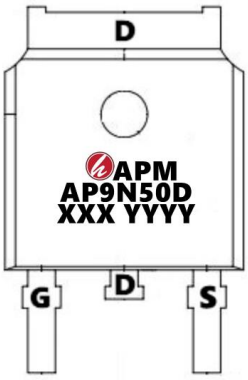
AP9N50D

500V N-Channel Enhancement Mode MOSFET

Description

The AP9N50D is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.





General Features

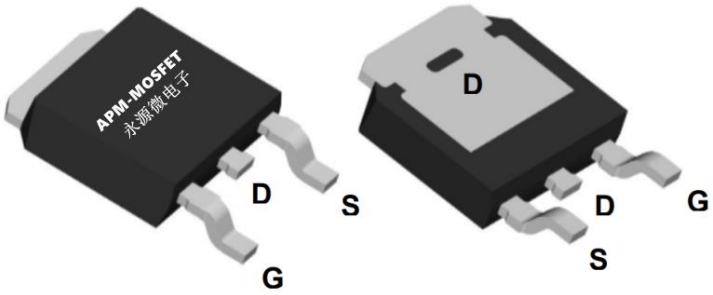
V_{DS} = 500V I_D =9A

$R_{DS(ON)}$ < 720mΩ @ V_{GS}=10V （**Type：630mΩ**）

Application

Uninterruptible Power Supply(UPS)

Power Factor Correction (PFC)



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP9N50D	TO-252-3L	AP9N50D XXX YYYY	2500

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Value	Unit
VDSS	Drain-Source Voltage (V_{GS} = 0V)	500	V
ID	Continuous Drain Current	9	A
IDM	Pulsed Drain Current (note1)	36	A
VGS	Gate-Source Voltage	±30	V
E_{AS}	Single Pulse Avalanche Energy (note2)	347	mJ
IAR	Avalanche Current (note1)	9	A
E_{AR}	Repetitive Avalanche Energy note1)	22	mJ
P_D	Power Dissipation (T_C = 25ºC)	178	W
TJ, Tstg	Operating Junction and Storage Temperature Range	-55~+150	ºC
RthJC	Thermal Resistance, Junction-to-Case	0.7	ºC/W
RthJA	Thermal Resistance, Junction-to-Ambient	62.5	ºC/W

500V N-Channel Enhancement Mode MOSFET

Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	500	535	-	V
IDSS	Zero Gate Voltage Drain Current	V_{DS}=500V, V_{GS}=0V,T_J=25℃	-	-	1	μA
IGSS	Gate to Body Leakage Current	V_{DS}=0V, V_{GS}= ±30V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D=250μA	2	3	4	V
RDS(on)	Static Drain-Source on-Resistance	V_{GS} =10V, I_D =4.5A	-	630	720	mΩ
Ciss	Input Capacitance	V_{DS}=25V, V_{GS}=0V, f=1.0MHz	-	1100	-	pF
Coss	Output Capacitance		-	106	-	pF
Crss	Reverse Transfer Capacitance		-	32	-	pF
Q_g	Total Gate Charge	V_{DD}=400V, I_D=9A, V_{GS}=10V	-	19.5	-	nC
Qgs	Gate-Source Charge		-	4.6	-	nC
Qgd	Gate-Drain(“Miller”) Charge		-	7.1	-	nC
td(on)	Turn-on Delay Time	V_{DD}=250V, I_D=9A, R_G=25Ω	-	24	-	ns
tr	Turn-on Rise Time		-	44	-	ns
td(off)	Turn-off Delay Time		-	55	-	ns
t_f	Turn-off Fall Time		-	35	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	9	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	36	A
VSD	Drain to Source Diode Forward Voltage	V_{GS}=0V, I_{SD}=9A	-	-	1.4	V
trr	Reverse Recovery Time	V_{GS}=0V, I_S=9A, di/dt=100A/μs	-	332	-	ns
Q_{rr}	Reverse Recovery Charge		-	3.5	-	μC

Note :

1、The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.

2、The EAS data shows Max. rating . IAS=6A, VDD = 50V, RG = 25 Ω, Starting TJ = 25 ºC

3、The test condition is Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%

4、The power dissipation is limited by 150℃ junction temperature

5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

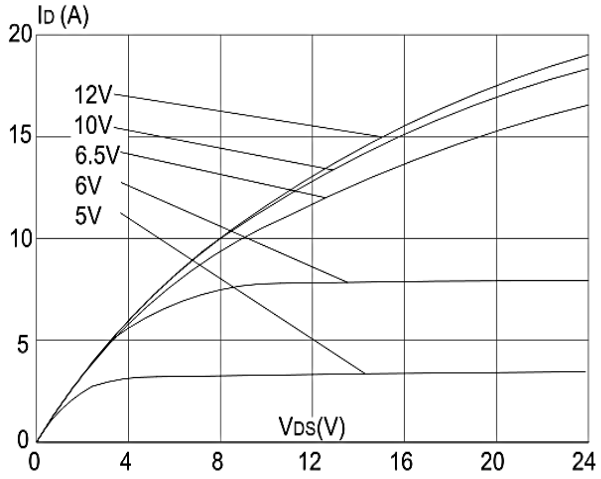


Figure1: Output Characteristics

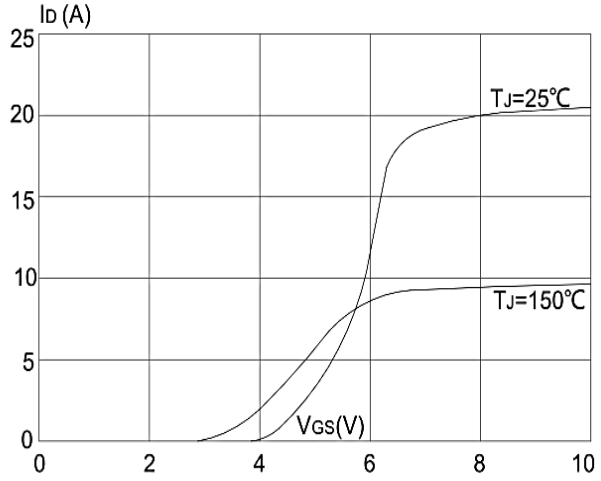


Figure 2: Typical Transfer Characteristics

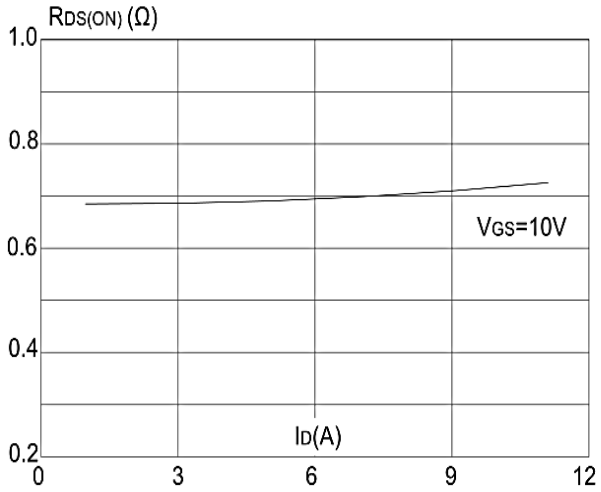


Figure 3:On-resistance vs. Drain Current

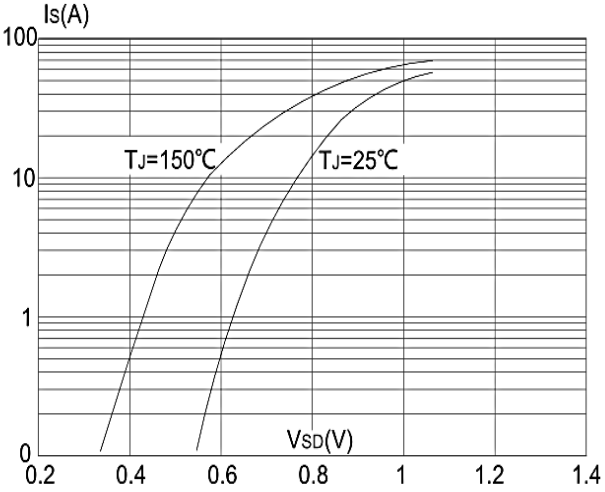


Figure 4: Body Diode Characteristics

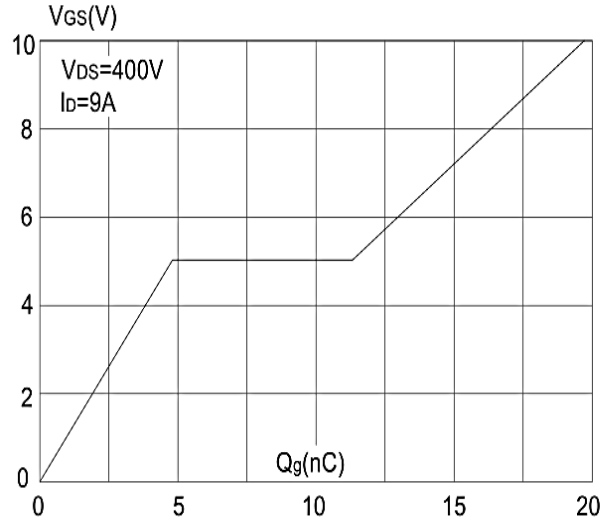


Figure 5: Gate Charge Characteristics

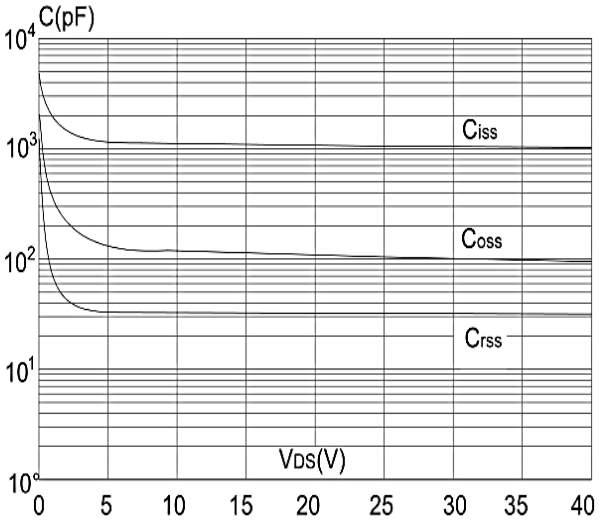


Figure 6: Capacitance Characteristics

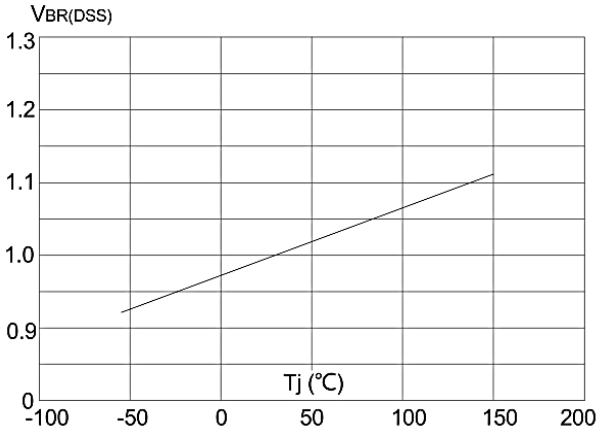


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

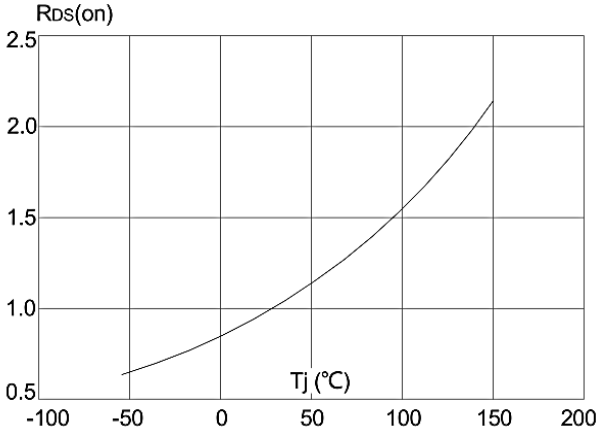


Figure 8: Normalized on Resistance vs Junction Temperature

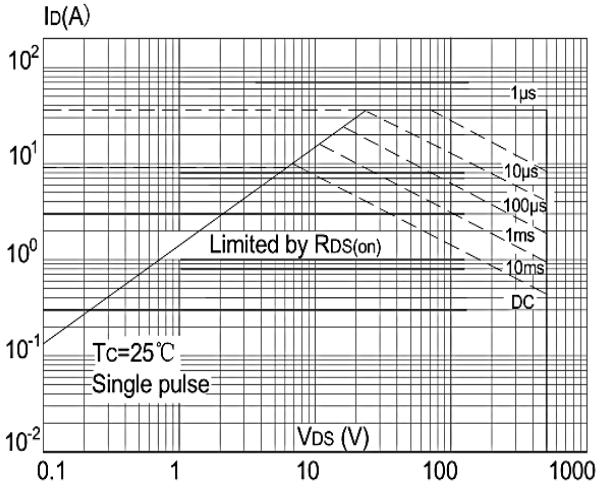


Figure 9: Maximum Safe Operating Area vs. Case Temperature

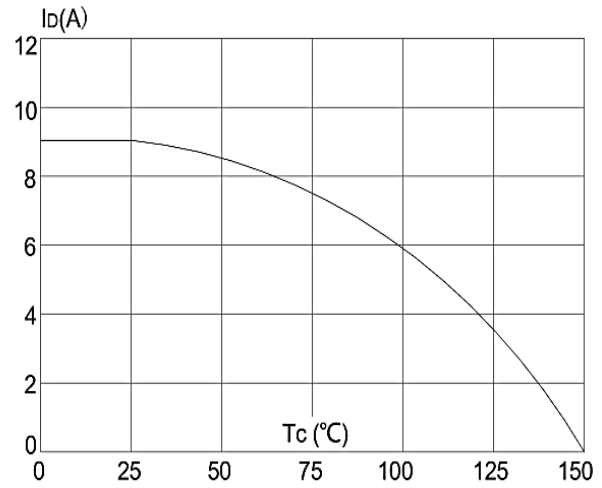


Figure 10: Maximum Continuous Drain Current

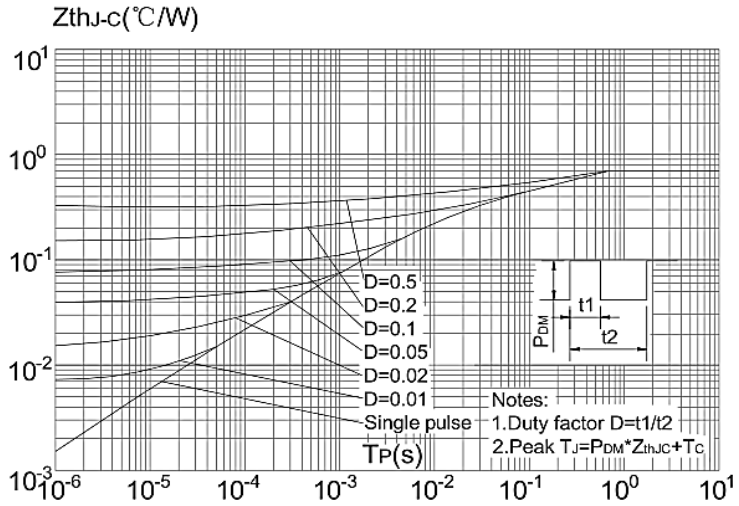
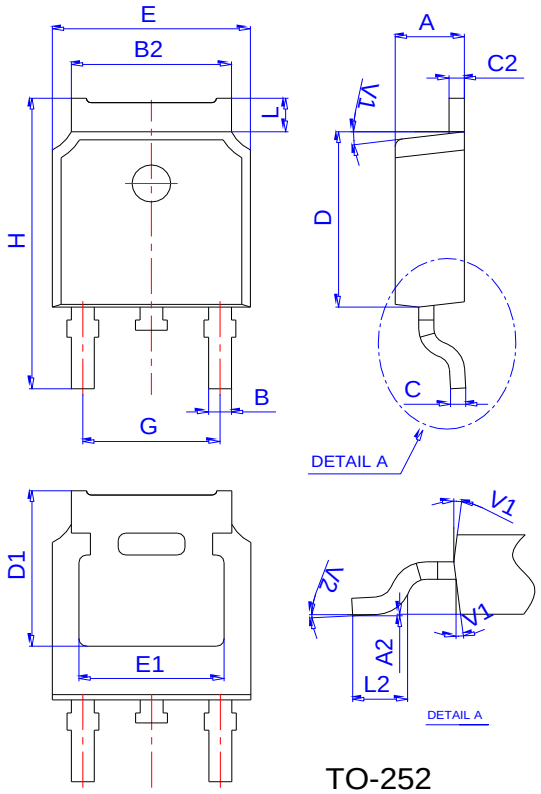


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

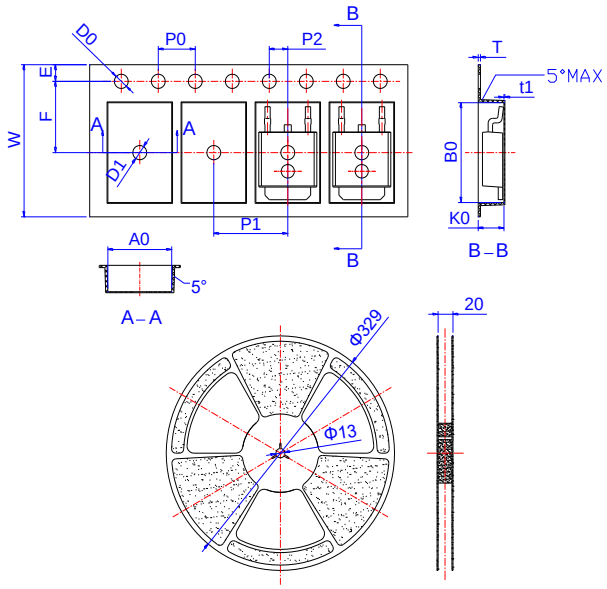
Package Mechanical Data:TO-252-3L



TO-252

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Reel Specification-TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583

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500V N-Channel Enhancement Mode MOSFET

Edition	Date	Change
Rve1.0	2021/1/31	Initial release