



AP778

DATA SHEET

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GENERAL DESCRIPTION

AP778 is a motion detector IC, which can detect a object moving toward or going away from the sensor connected to **AP778**. The sensor is formed simply by two metal plates. This IC uses the interaction of the metal plates to detect a moving object. In order to meet the requirement of different application, this IC has 3 kinds of input pins that can be used to control the range of sensitivities, the response time, and the output time duration. A regulator circuit is designed in **AP778** to provide a stable power supply for the IC. **BUSY** is an output pin that will be activated when electric field variation is detected. **OUTA**, **OUTB**, **OUTC** and **OUTD** are output pins that can be used to drive LED or used as the other busy pins. **SLPOLAR** is an input pin, which can control the polarity of **STANDBY**, **BUSY**, **OUTA**, **OUTB**, **OUTC** and **OUTD**. There is a shutdown timer built in **AP778**. If **PWRONN** is connected to **VDD**, the system will shut down in about 4 minutes, if nothing is detected. If pin **PWRONN** is connected to **VSS**, the shutdown function is inhibited. **LODIS** is an input pin. If **LODIS** is connected to **VSS**, **AP778** will shut down in 2 minutes if there is not input trigger signal.

FEATURES

1. Response time is adjustable
2. Output Duration is adjustable
3. Sensitivity is adjustable
4. Two kinds of input/output polarity
5. Auto shutdown circuit designed in
6. Output pattern is mask programmable
7. Built-in regulator circuit
8. Low cost Sensor
9. Detect two kinds of motion direction.

ABSOLUTE MAXIMUM RATING

Power supply 5V
 Input Voltage VSS -0.3V to VDD +0.3V
 Operating Temperature 0°C to 70°C
 Storage Temperature -65°C to 125°C

ELECTRICAL CHARACTERISTICS

System	Description	Test Condition	Limit			unit
			Min.	Typ.	Max.	
VDD	Supply Voltage		2.4	3.0	5.0	V
V _{IL}	Input Voltage Low	VDD = 3V	-	-	0.3VDD	V
V _{IH}	Input Voltage High	VDD = 3V	0.7VDD			V
VGN		VDD = 3V C _{VGN} = 2.2uF	-	2.20		V
I _{OP}	Operating Current	VDD = 3V OSCA = 155Khz OSC _{VIN2} = 4.3 MHz		0.3		mA
I _{STD}	Shut Down Current	VDD = 3V			1	uA
OSCA	Operating Frequency	VDD = 3V Rosc = 330K		155		kHz

Application Consideration

The PC board layout is important in the application. The most critical is analog circuit: VGN. VDD and VSS on two sides of VGN are analog voltage source. The current of the other circuit can not go through the VGN circuit. The interference of digital circuit must take into consideration when there is a motor. In this case , it's better to connect a 0.1uf capacitor between VDD(pin5) and VSS(pin24),this capacitor should be closed to VDD and VSS as possible. The current supplied to the motor should go to the battery directly.

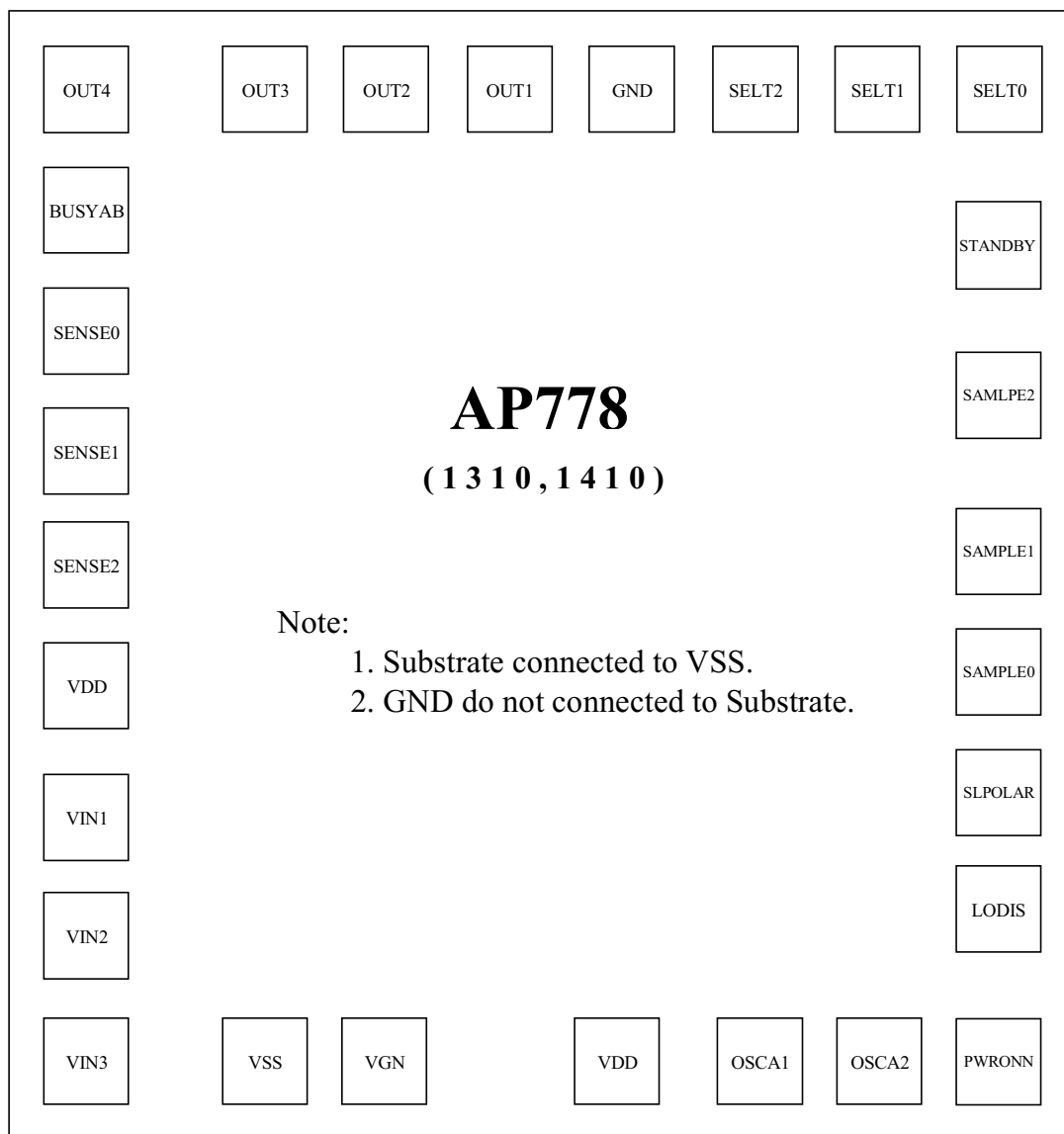
Because the capacitor between VIN1 and VIN2 is 0.5pf only, the parasitical capacitance is very critical. The parasitical capacitance should be reduced to minimal. The space between two metals will determine the sensitivity directly. Bigger capacitor between VIN1 and VIN2 will reduce the sensitivity. SENSE0 SENSE1 and SENSE2 are sensitivity setting input pins. (0, 0, 0) is the most sensitive, (1, 1, 1) is the least sensitive. These inputs have internal pull up transistor. Setting (0, 0, 0) is not recommended if noise immunity is important. Sample2 is a noise protection pin, sample2=1 means high noise rejection. The connecting wire between VIN1,VIN3 and metal plates is important also. The space between two wires should kept fixed, to avoid false trigger.

Standby input can be connected to BUSYAB BUSYB or BUSYA. Standby input can also be connected external MCU or speech IC.

PIN ASSIGNMENT OF AP778-01

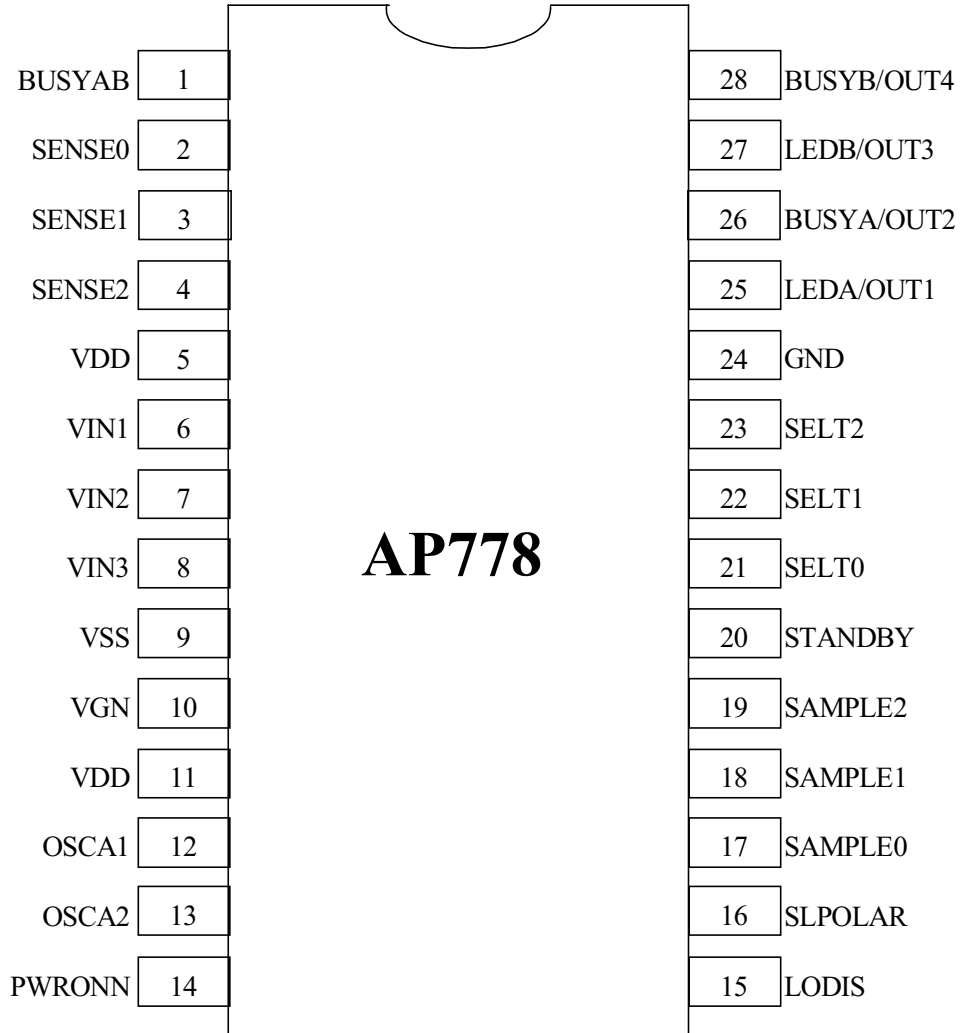
Pin No.	Pin Name	Description
1	BUSYAB	BUSY pin is used to indicate that the system is activated. The polarity of this pin is determined by SLPOLAR pin. When SLPOLAR = 1, this pin is high active. Either moving toward or going away from sensor will be activated this pin.
2~4	SENSE0 ~ SENSE2	Sensitivity selects input pins.
5	VDD	Positive power supplies terminal of digital circuit.
6	VIN1	Sensor input1.
7	VIN2	Sensor input2.
8	VIN3	Electric field detector input3; this pin connected to the sensor through a resistor.
9	VSS	Analog Negative power supplies terminal.
10	VGN	The output of regulator, a 2.2uF capacitor is connected between this pin and ground.
11	VDD	Analog Positive power supplies terminal.
12, 13	OSCA2~OSCA1	Oscillator circuit. Provides clock signal for the system.
14	PWRONN	When connect this pin to VDD, AP778 will enter shutdown state if nothing is detected for a period of time. When connect this pin to VSS, AP778 will not shutdown.
15	LODIS	Low sensitivity disable input pin. If connect this pin to VSS, AP778 will enter Low Sensitivity mode, if there is not trigger signal detected.
16	SLPOLAR	Polarity pin. Used to change the polarity of BUSYAB, BUSYB, LEDB, BUSYA, LEDA, OUTD and STANDBY.
17~19	Samlpe2~Sample0	Response time select pins.
20	STANDBY	This pin can be used to disable the detecting process of AP778 . If connect this pin to BUSY, then detecting process will be disable. When SLPOLAR pin is high, this pin is high disable.
21~23	SELT0~SELT2	Output time duration control pin.
24	GND	Negative power supplies terminal of digital circuit.
25	LEDA/OUT1	LED output pin, which indicates BUSYA is activated.
26	BUSYA/OUT2	This pin is OUT2, which is used as a BUSY pin, when an object moving toward the sensor.
27	LEDB/OUT3	LED output pin, which indicates BUSYB is activated.
28	BUSYB/OUT4	This pin is OUT4, which is used as a BUSY pin, when an object moving away from the sensor.

BONDING PAD DIAGRAM



P A D	X, Y U n I t : u m	P A D	X, Y U n I t : u m
BUSYAB	(98 , 1163)	LODIS	(1213 , 287)
SENSE0	(98 , 1013)	SLPOLAR	(1213 , 437)
SENSE1	(98 , 863)	SAMPLE0	(1213 , 587)
SENSE2	(98 , 713)	SAMPLE1	(1213 , 737)
VDD	(98 , 563)	SAMPLE2	(1213 , 930)
VIN1	(98 , 398)	STANDBY	(1213 , 1120)
VIN2	(98 , 248)	SELT0	(1213 , 1313)
VIN3	(98 , 98)	SELT1	(1063 , 1313)
VSS	(298 , 98)	SELT2	(913 , 1313)
VGN	(447 , 98)	GND	(763 , 1313)
VDD	(734 , 98)	OUT1	(613 , 1313)
OSCA1	(913 , 98)	OUT2	(463 , 1313)
OSCA2	(1063 , 98)	OUT3	(313 , 1313)
PWRONN	(1213 , 98)	OUT4	(98 , 1313)

PIN CONFIGURATION (28 PIN SKINNY)



OPTION SELECT

SENSE2	SENSE1	SENSE0		SAMPLE2	SAMPLE1	SAMPLE0	
0	0	0	最靈敏	0	0	0	Sample rate的寬度最窄
0	0	1		1	0	0	
0	1	0	次靈敏	0	0	1	次窄
0	1	1		1	0	1	
1	0	0		0	1	0	次寬
1	0	1		1	1	0	
1	1	0		0	1	1	Sample rate 的寬度最寬
1	1	1	最不靈敏	1	1	1	

OSCA=175KHZ

SELT2	SELT1	SELT0	手靠近或離開	手離開		手靠近	
			BUSYAB (Sec)	BUSYB (Sec)	LEDB (Sec)	BUSYA (Sec)	LEDA (Sec)
0	0	0	1.5	1.5	0.18	1.5	0.18
0	0	1	3	3	0.18	3	0.18
0	1	0	4.5	4.5	0.18	4.5	0.18
0	1	1	6	6	0.18	6	0.18
1	0	0	7.5	7.5	0.18	7.5	0.18
1	0	1	9	9	0.18	9	0.18
1	1	0	10.5	10.5	0.18	10.5	0.18
1	1	1	12	12	0.18	12	0.18

Auto Shutdown Timing

OSCA2=175khz Shutdown timing=4.8分鐘

Auto Low sense Timing

OSCA2=175khz Low sense timing=2.5分鐘

AP778 應用須知：

1. Sample2是抗雜訊（noise）能力的選擇PIN。當Sample2=1時（Sample2浮接）具有較高的抗雜訊能力；反之，當Sample2接地時，抗雜訊能力較低。Sample2=0時，感應距離較遠，但相對地受干擾的機率也會稍微提高。一般而言，建議Sample2=1。Sample1與Sample0則是反應時間常數的設定，（Sample1, Sample0）=（0，0）時，反應時間較快；兩個PIN都浮接時反應較慢。

2. OSCA2，OSCA1是控制整個系統的振盪電路，此頻率的快慢直接（線性比例）影響到Shout-down，Low Sensitivity time，Response time，SET0 ~SET2，BUSY與LED時間。

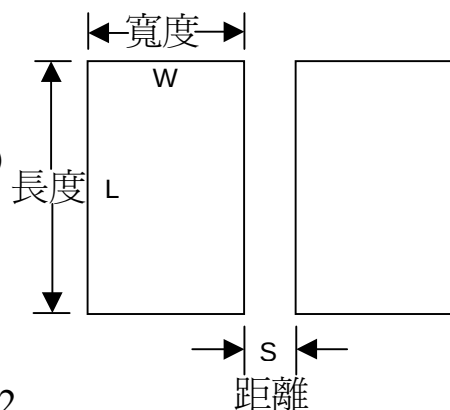
f_{OSCA} 與 f_{VIN} 之間也有一定的關係存在，假設OSCA之電阻為 $300K\Omega$ ， f_{VIN} 不能超過60倍，否則系統無法工作。OSCA電阻為 $300K\Omega$ ， $f_{OSCA} \sim 170KHz$ ，如果 $f_{VIN} > 10MHz$ 則系統無法工作。但在一般設計上，都不會將 f_{VIN} 設定在最大值，有關此點將在以下各節詳述。

3. 如何量測 f_{VIN} ：

在VIN1、VIN2與VIN3之間，形成一個類似RC振盪器的電路。由於VIN1與VIN2間的外接電容只有約1pf。而VIN1與VIN3的感應金屬片其電容也只有不到1pf。所以在量測時，如果以probe直接量測，VIN3則由於probe的輸入電容的影響，所量測的頻率會較實際的頻率低很多。較少干擾的量測方法如下：將示波器（oscilloscope）的地線與probe端，夾住一個 $680\mu H$ 的電感，將其移近感應片的輸出端（VIN3），示波器的垂直刻度在20mv，則其所量到的頻率所受之影響將為較小。

4. 感應片與VIN之關係：

感應片之材質應為金屬導體，銅片與鋁片都是良好的選擇。感應片之長度（L），寬度（W）與兩感應片間之距離（S）都會影響感應距離。長度與寬度增加，都會增加感應距離，但其變化並非線性的。金屬片間距離減小，也會使VIN的頻率與感應距離增加。但最小距離也須維持。一般而言，距離約在0.5cm其到1cm之間。感應片的大小與VIN2



，VIN1間的外加電容有相當的關係。VIN3與VIN1感應片的電容應較VIN2與VIN1間的電容為小，才能維持頻率的穩定。

AP778 應用須知：

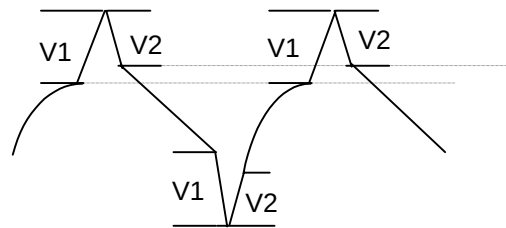
從經驗得知，感應片的 $L=5\text{cm}$ ， $W=2.5\text{cm}$ ， $S=0.5\text{cm}$ 時，VIN1與VIN2間的電容為 1.5pf ， $R=120\text{K}\Omega$ 時， f_{VIN} 約為 5MHz 。一般而言，系統工作在此頻率可以得到一個較穩定的狀況。一般來講當一個電路板完成，再裝入絨毛或塑膠玩具後，VIN的頻率會再增加，所以將系統設計在頻率的上限時，當外圍的環境改變後，整個感應距離可能會大幅縮短，甚至無法偵測。從電路板的VIN1與VIN3端連接到感應片的兩根導線，其間也具有電容，所以也會影響頻率與感應距離。為減小其電容，兩導線的距離應該遠一點會比較好。金屬片必須要固定好，不能搖動，連接導線必須為硬線，才不會搖動。而且導線之長度必須保持一固定值，生產才會順利。

5. 如何維持 f_{VIN} 的穩定與提高感應距離：

首先必須盡量減小雜散電容，VIN1，VIN2，VIN3的Bonding wire 間須保持距離且Bonding wire愈短愈好，為減小VDD對VIN1的干擾，在PCB板上，VIN1與VDD間加一條VSS線，將其作隔離。PCB的基座接到VSS，但是各個input pin打線打到GND上，而不打到基座上，以避免數位電路對類比電路之干擾。馬達的外殼接到地線上，使其受外來noise干擾減到最小。

6. 如何決定電容與電阻值：

用示波器直接量測VIN1的波形，如右圖所示。VIN2與VIN1的電容 C_x 選擇，使得V1電壓較V2為大（ $V_2 \sim 0.8V_1$ ），再選擇電阻 R_x （VIN1與VIN3），使得 $f_{\text{VIN}} \sim 5\text{MHz}$ （用 $680\mu\text{h}$ 電感量測），如此便可得到適當的感應距離與穩定度。



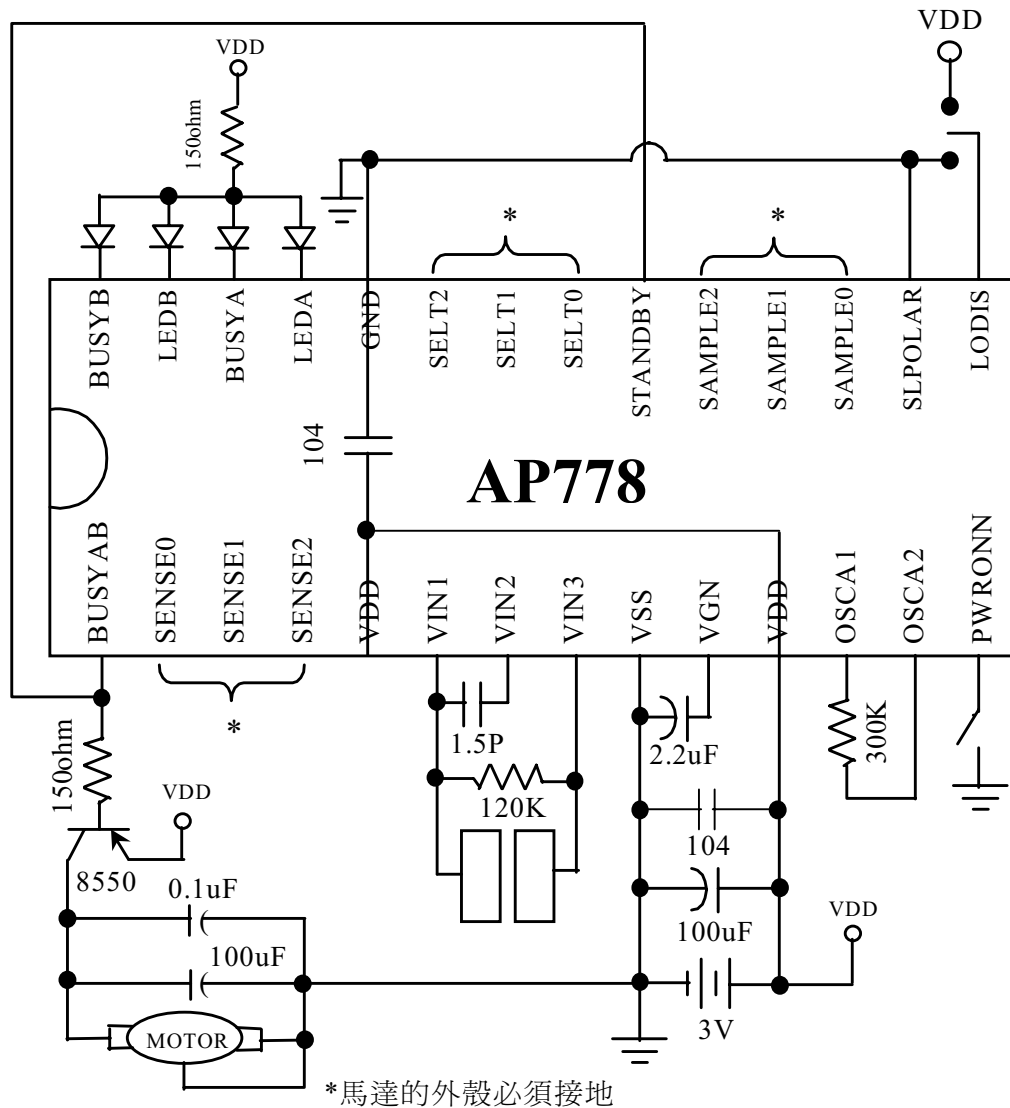
7. 當 C_x 與感應片之電容值漸接近時， f_{VIN} 的頻率會隨 C_x 值產生很大的頻率變化。如果 $C_x \sim 1.5\text{pf}$ ，則其準度可能需求在 $\pm 0.1\text{pf}$ ，此種電容可要求電容供應商代為sorting。由於每一批IC其雜散電容（寄生電容）值會有一定之公差，所以針對每個Lot的IC，最好要量出其最佳之 C_x ，量產才能順利。當然，如果感應距離的要求不是很長， C_x 的要求就可以較為寬鬆。

8. GND與VSS：

GND為數位電路的地，VSS為類比電路的地。VGN與VSS構成類比電路的電源供應器（power supply）。為維持類比電路的穩定，VSS只拉到VGN電容的地與基座。

APPLICATION CIRCUIT I

SLPOLAR=VSS



* 此應用電路不容易受馬達干擾,如輸出無極性之要求,建議使用此電路。

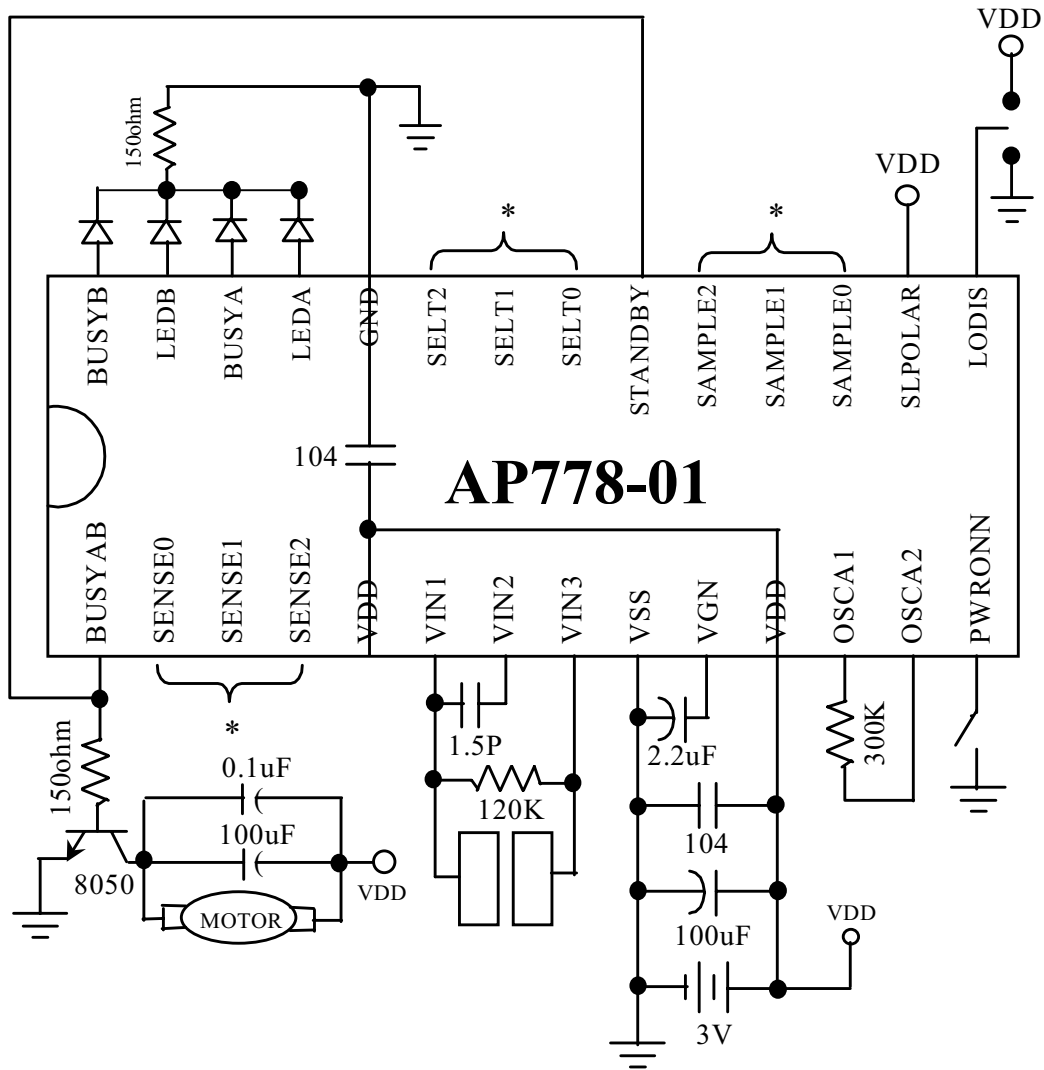
****SELT2~0,SAMPLE2~0,SENSE2~0 must connect to VSS or Floating ,
(These pins are pull high internally)**

SAMPLE2~0 : 設定SAMPLE RATE 的寬度

SELT2~0：設定 BUSYAB,BUSYB,BUSYA,LEDB,LEDA 的時間

SENSE2~0：設定靈敏度 (建議使用 001)

APPLICATION CIRCUIT II SLPOLAR=VDD



* 此應用電路比較容易受馬達干擾,如輸出無極性之要求,建議使用
CIRCUIT I 應用電路

** SELT2~0,SAMPLE2~0,SENSE2~0 must connect to VSS or Floating ,
These pins are pull high internally)

SAMPLE2~0 : 設定SAMPLE RATE 的寬度

SELT2~0 : 設定 BUSYAB,BUSYB,BUSYA,LEDB,LEDA 的時間

SENSE2~0 : 設定靈敏度 (建議使用 001)