

200V N-Channel Enhancement Mode MOSFET

Description

The AP70N20MP is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.

General Features

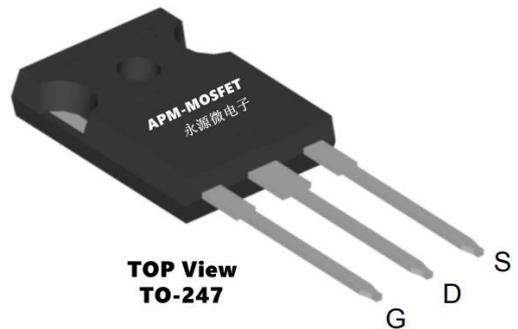
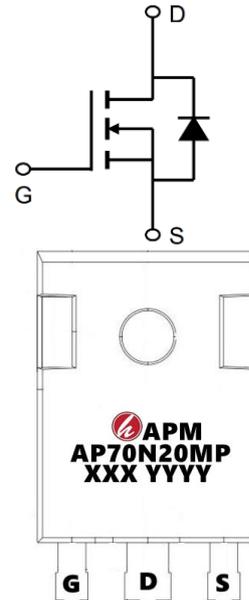
$V_{DS} = 200V$ $I_D = 70A$

$R_{DS(ON)} < 38m\Omega$ @ $V_{GS}=10V$ (Type: 30m Ω)

Application

Uninterruptible Power Supply(UPS)

Power Factor Correction (PFC)



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP70N20MP	TO-247-3L	AP70N20MP	500

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Value	Unit
		TO-247-3L	
V_{DSS}	Drain-Source Voltage ($V_{GS} = 0V$)	200	V
I_D	Continuous Drain Current	70	A
I_{DM}	Pulsed Drain Current (note1)	280	A
V_{GS}	Gate-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy (note2)	1800	mJ
I_{AR}	Avalanche Current (note1)	25	A
E_{AR}	Repetitive Avalanche Energy (note1)	20	mJ
P_D	Power Dissipation ($T_C = 25^\circ C$)	367	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	$-55 \sim +150$	$^\circ C$
R_{thJC}	Thermal Resistance, Junction-to-Case	1.5	$^\circ C/W$
R_{thJA}	Thermal Resistance, Junction-to-Ambient	40	$^\circ C/W$

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Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μA	200	220	--	V
IDSS	Zero Gate Voltage Drain Current	V _{DS} = 200V, V _{GS} = 0V, T _J = 25°C	--	--	5	μA
		V _{DS} = 160V, V _{GS} = 0V, T _J = 125°C	--	--	100	
IGSS	Gate-Source Leakage	V _{GS} = ±20V	--	--	±100	nA
VGS(th)	Gate-Source Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	2.0	3.0	4.0	V
RDS(on)	Drain-Source On-Resistance (Note3)	V _{GS} = 10V, I _D = 9A	--	30	38	mΩ
C _{iss}	Input Capacitance	V _{GS} = 0V, V _{DS} =25V, f=1.0MHz	--	3538	--	pF
C _{oss}	Output Capacitance		--	657	--	
C _{rss}	Reverse Transfer Capacitance		--	280	--	
Q _g	Total Gate Charge	V _{DD} = 160V, I _D = 50A, V _{GS} = 10V	--	244	--	nC
Q _{gs}	Gate-Source Charge		--	16	--	
Q _{gd}	Gate-Drain Charge		--	144	--	
td(on)	Turn-on Delay Time	V _{DD} =100V, I _D =50A, R _G =25 Ω	--	53	--	ns
t _r	Turn-on Rise Time		--	65	--	
td(off)	Turn-off Delay Time		--	689	--	
t _f	Turn-off Fall Time		--	230	--	
I _s	Continuous Body Diode Current	T _C = 25 °C	--	--	50	A
ISM	Pulsed Diode Forward Current		--	--	200	
V _{SD}	Body Diode Voltage	T _J = 25°C, I _{SD} = 50A, V _{GS} = 0V	--	--	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0V, I _s = 50A, di _F /dt = 100A /μs	--	208	--	ns
Q _{rr}	Reverse Recovery Charge		--	2.04	--	μC

Note :

- 1、 The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、 The EAS data shows Max. rating . I_{AS} = 25A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25 °C
- 3、 The test condition is Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%
- 4、 The power dissipation is limited by 150°C junction temperature
- 5、 The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

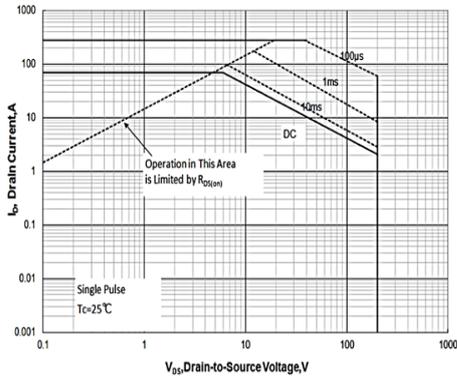


Figure 1 Maximum Forward Bias Safe Operating Area

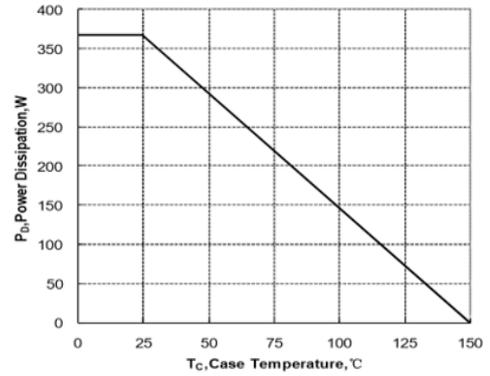


Figure 2 Maximum Power dissipation vs Case Temperature

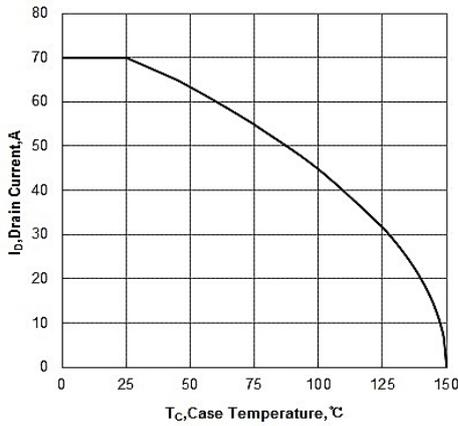


Figure 3 Maximum Continuous Drain Current vs Case Temperature

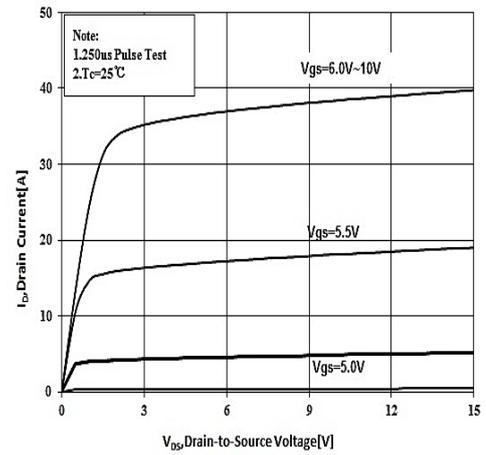


Figure 4 Typical Output Characteristics

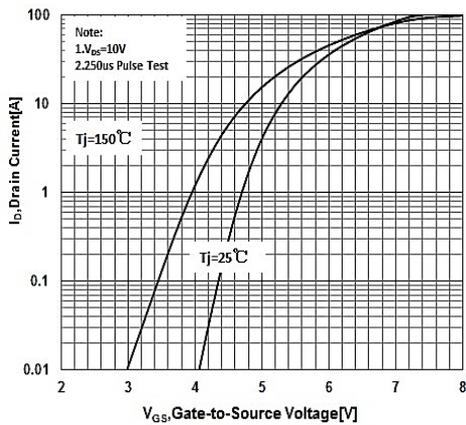


Figure 5: Typical Transfer Characteristics

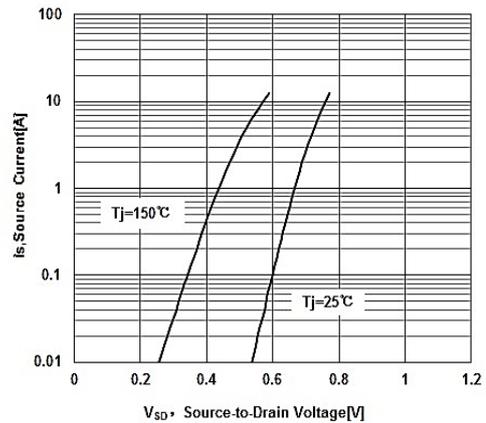


Figure 6: Typical Body Diode Transfer Characteristics

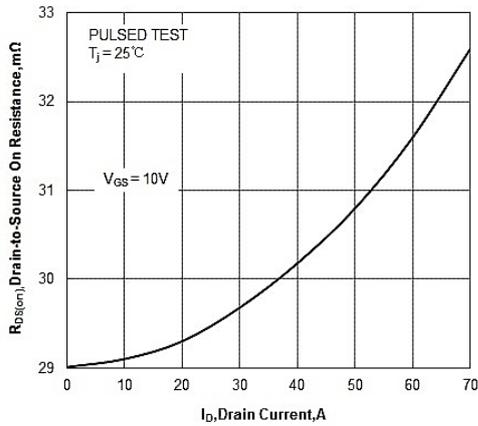


Figure 7: Source ON Resistance vs Drain Current

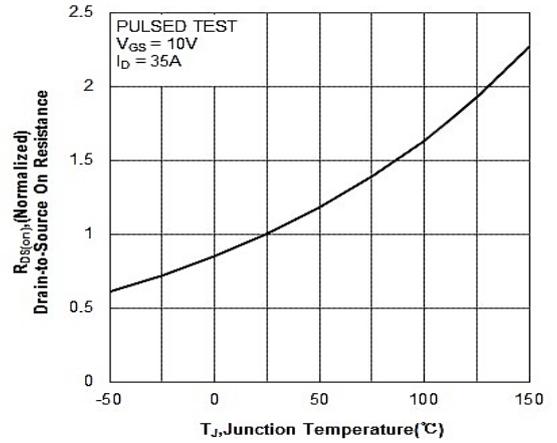


Figure 8: Source on Resistance vs Junction Temperature

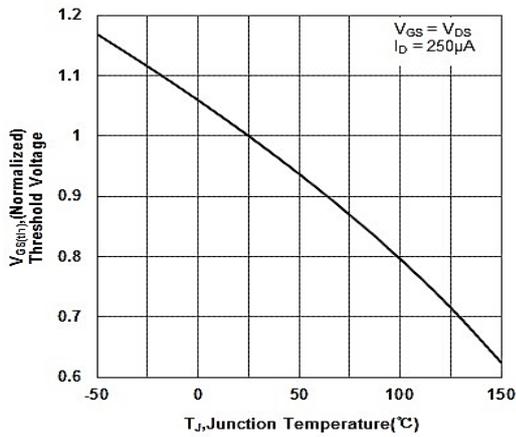


Figure 9 Typical Theshold Voltage vs Junction Temperature

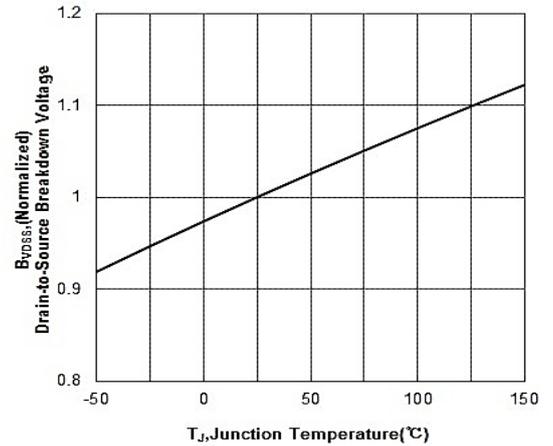


Figure 10 Typical Breakdown Voltage vs Junction Temperature

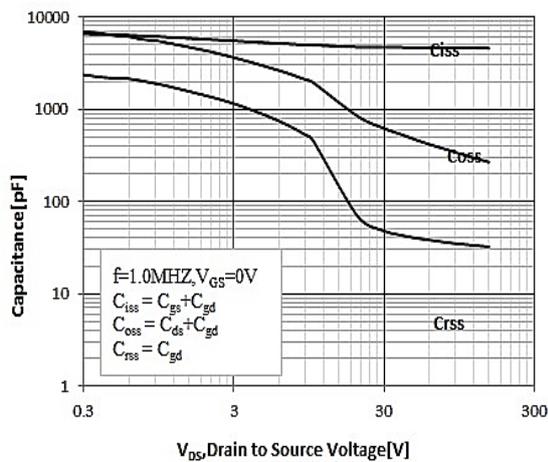


Figure 11 Typical Capacitance vs Drain to Source Voltage

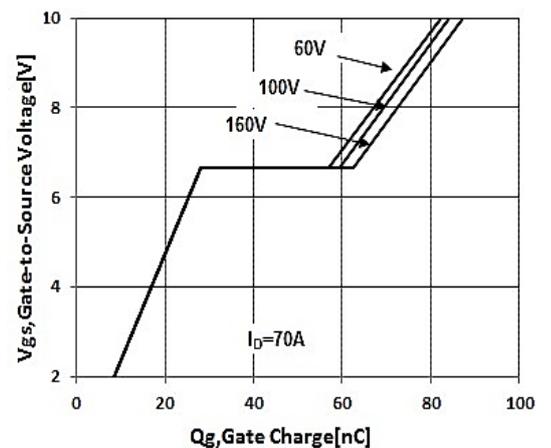
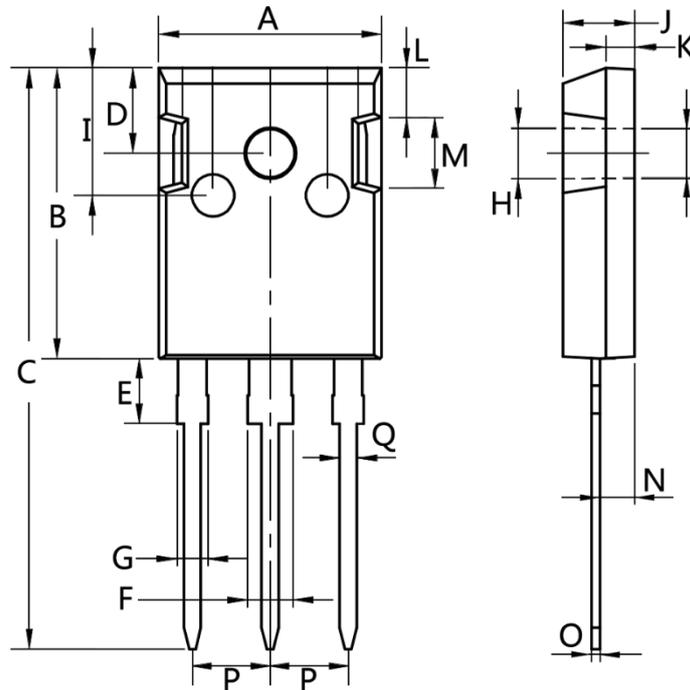


Figure 12 Typical Gate Charge vs Gate to Source Voltage

Package Mechanical Data-TO-247-3L



Dim.	Min.	Max.
A	15.0	16.0
B	20.0	21.0
C	41.0	42.0
D	5.0	6.0
E	4.0	5.0
F	2.5	3.5
G	1.75	2.5
H	3.0	3.5
I	8.0	10.0
J	4.9	5.1
K	1.9	2.1
L	3.5	4.0
M	4.75	5.25
N	2.0	3.0
O	0.55	0.75
P	Typ 5.08	
Q	1.2	1.3

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Edition	Date	Change
Rve1.0	2019/1/31	Initial release
Rve1.1	2021/9/26	Change of specification forma

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