AP6G02LI

20V N+P-Channel Enhancement Mode MOSFET

Description

The AP6G02LI uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

V_{DS} = 20V I_D =7.5A

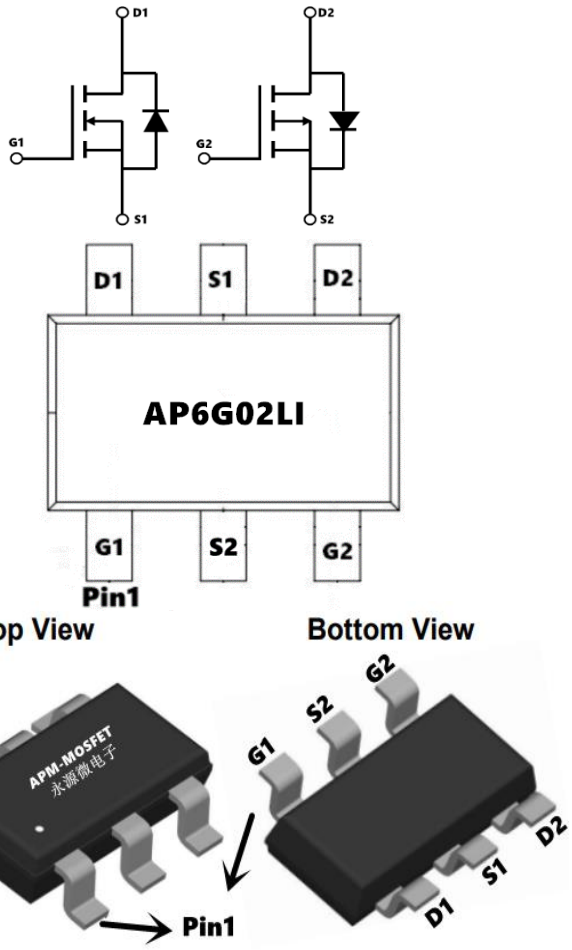
$R_{DS(ON)}$ < 35mΩ @ V_{GS}=4.5V （**Type：28mΩ**）

V_{DS} = -20V I_D =-6.8A

$R_{DS(ON)}$ < 40mΩ @ V_{GS}=-4.5V（**Type：35mΩ**）

Application

BLDC



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP6G02LI	SOT23-6L	AP6G02LI	3000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	N-Ch	P-Ch	Units
VDS	Drain-Source Voltage	20	-20	V
VGS	Gate-Source Voltage	±12	±12	V
I_D@T_A=25℃	Continuous Drain Current, V_{GS} @ 10V[1]	7.5	-6.8	A
I_D@T_A=70℃	Continuous Drain Current, V_{GS} @ 10V[1]	5.2	-4.5	A
IDM	Pulsed Drain Current[2]	24	-28	A
EAS	Single Pulse Avalanche Energy[3]	24	68	mJ
P_D@T_A=25℃	Total Power Dissipation[4]	1.5		W
TSTG	Storage Temperature Range	-55 to 150		℃
T_J	Operating Junction Temperature Range	-55 to 150		℃
R_{θ}JA	Thermal Resistance Junction-Ambient [1]	105		℃/W
R_{θ}JC	Thermal Resistance Junction-Case[1]	45		℃/W

20V N+P-Channel Enhancement Mode MOSFET

N-Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	20	22	---	V
RDS(ON)	Static Drain-Source On-Resistance[2]	V_{GS}=4.5V , I_D=3A	---	28	35	mΩ
		V_{GS}=2.5V , I_D=2A	---	32	40	mΩ
VGS(th)	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =250uA	0.5	0.75	1.2	V
IDSS	Drain-Source Leakage Current	V_{DS}=16V , V_{GS}=0V , T_J=25℃	---	---	1	uA
		V_{DS}=16V , V_{GS}=0V , T_J=55℃	---	---	5	
IGSS	Gate-Source Leakage Current	V_{GS}=±12V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=5V , I_D=3A	---	10.5	---	S
Q_g	Total Gate Charge (4.5V)	V_{DS}=15V , V_{GS}=4.5V , I_D=3A	---	4.6	---	nC
Qgs	Gate-Source Charge		---	0.7	---	
Qgd	Gate-Drain Charge		---	1.5	---	
Td(on)	Turn-On Delay Time	V_{DD}=10V , V_{GS}=4.5V , R_G=3.3Ω,I_D=3A	---	1.6	---	ns
T_r	Rise Time		---	42	---	
Td(off)	Turn-Off Delay Time		---	14	---	
T_f	Fall Time		---	7	---	
Ciss	Input Capacitance	V_{DS}=15V , V_{GS}=0V , f=1MHz	---	310	---	pF
Coss	Output Capacitance		---	49	---	
Crss	Reverse Transfer Capacitance		---	35	---	
IS	Continuous Source Current[1,4]	V_G=V_D=0V , Force Current	---	---	3.6	A
VSD	Diode Forward Voltage[2]	V_{GS}=0V , I_S=1A , T_J=25℃	---	---	1.2	V

Note :

1、The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、The power dissipation is limited by 150℃ junction temperature

4、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

P-Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	I_D = -250μA, V_{GS} = 0V	-20	-	-	V
IDSS	Zero Gate Voltage Drain Current	V_{DS} = -20V, V_{GS} = 0V	-	-	1.0	μA
IGSS	Gate-Body Leakage Current	V_{DS} = 0V, V_{GS} = ±12V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250μA	-0.5	-0.7	-1.0	V
RDS(ON)	Static Drain-Source ON-Resistance(3)	V_{GS} = -4.5V, I_D = -4A	-	35	40	mΩ
		V_{GS} = -2.5V, I_D = -3A	-	40	66	mΩ
Ciss	Input Capacitance	V_{GS} = 0V, V_{DS} = -10V, f = 1MHz	-	534	-	pF
Coss	Output Capacitance		-	62	-	pF
Crss	Reverse Transfer Capacitance		-	50	-	pF
Q_g	Total Gate Charge	V_{GS} = 0 to -4.5V V_{DS} = -10V, I_D = -2A	-	5.6	-	nC
Q_{gs}	Gate Source Charge		-	1	-	nC
Q_{gd}	Gate Drain("Miller") Charge		-	1	-	nC
td(on)	Turn-On DelayTime	V_{GS} = -4.5V, V_{DD} = -10V I_D= -2A, R_{GEN} = 3Ω	-	5	-	ns
t_r	Turn-On Rise Time		-	21	-	ns
td(off)	Turn-Off DelayTime		-	110	-	ns
t_f	Turn-Off Fall Time		-	239	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	-3	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-12	A
VSD	Drain to Source Diode Forward Voltage	V_{GS} = 0V, I_S = -4.2A	-	-	-1.2	V
trr	Body Diode Reverse Recovery Time	I_F = -2A, di/dt = 100A/us	-	64	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	10	-	nC

Note :

1、The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、The power dissipation is limited by 150℃ junction temperature

4、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

N-Channel Typical Characteristics

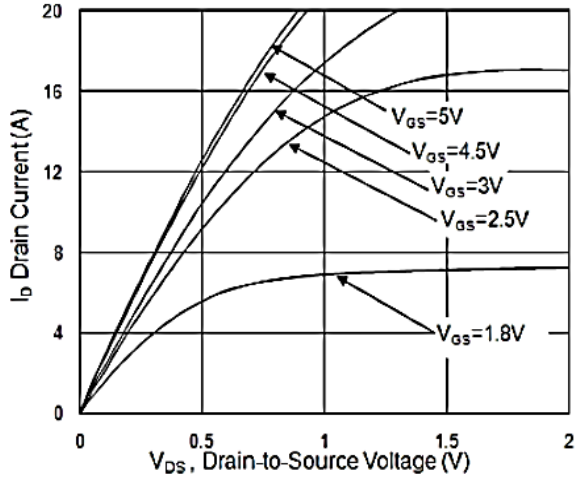


Fig.1 Typical Output Characteristics

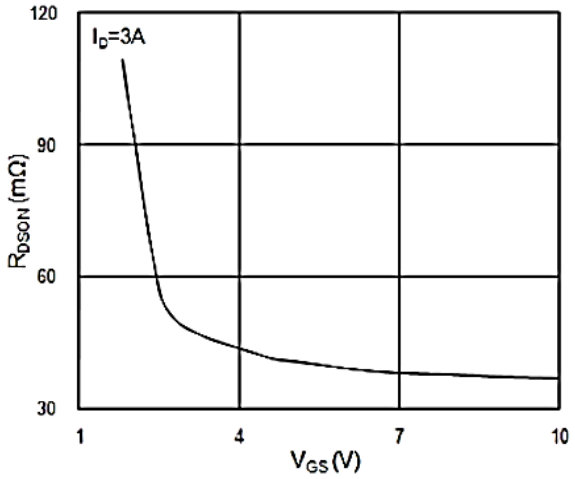


Fig.2 On-Resistance vs. G-S Voltage

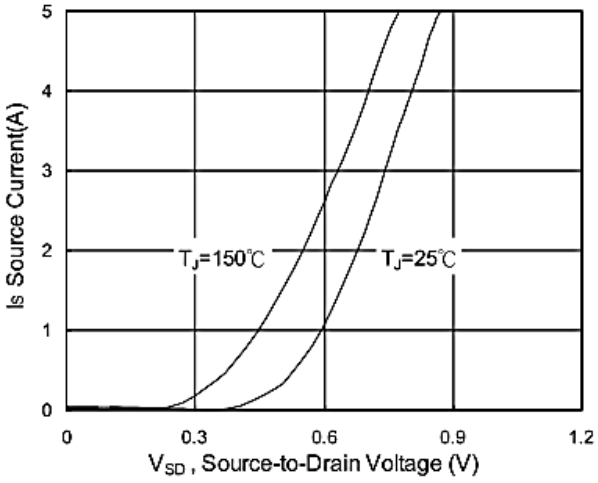


Fig.3 Source Drain Forward Characteristics

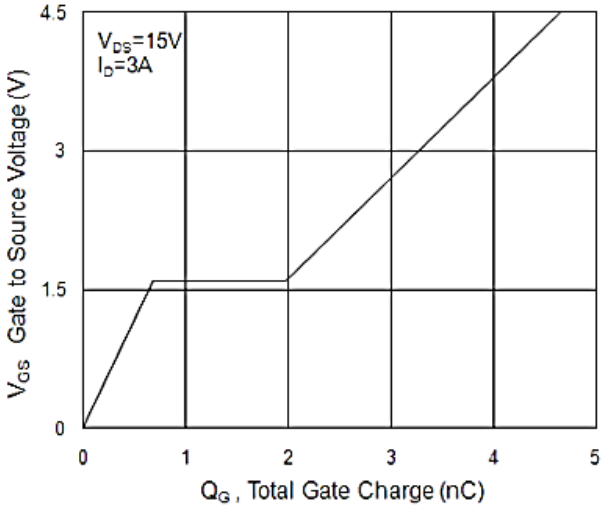


Fig.4 Gate-Charge Characteristics

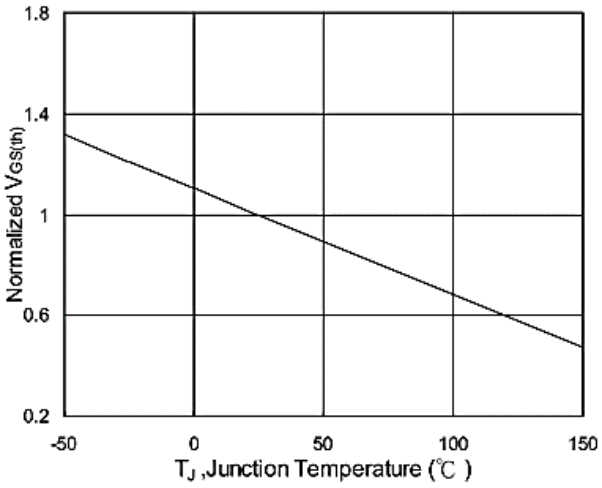


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

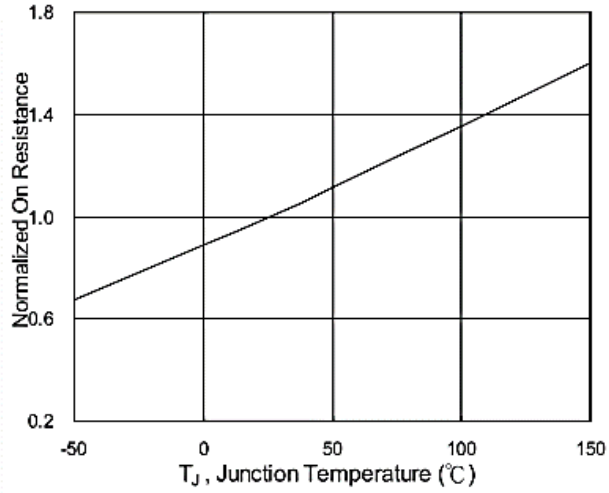


Fig.6 Normalized R_{DSON} vs. T_J

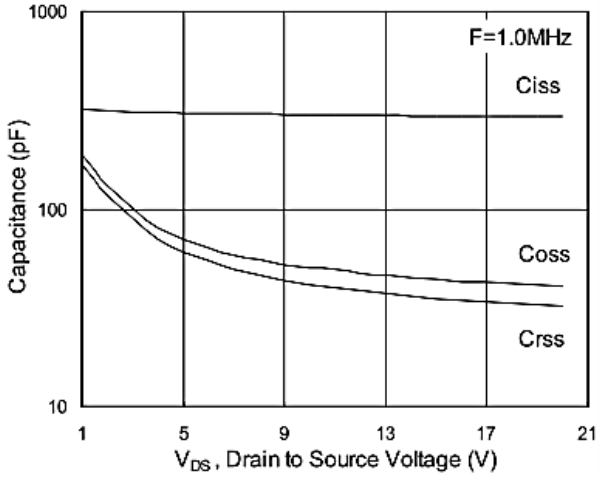


Fig.7 Capacitance

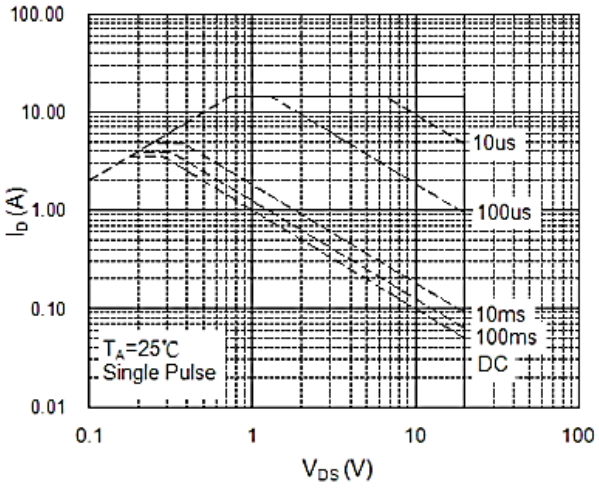


Fig.8 Safe Operating Area

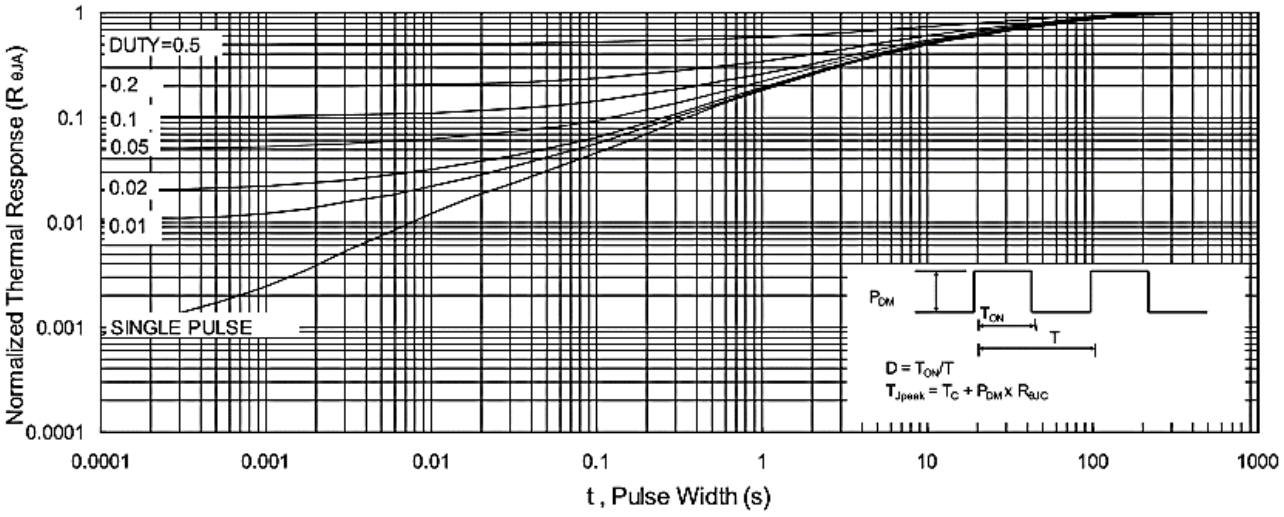


Fig.9 Normalized Maximum Transient Thermal Impedance

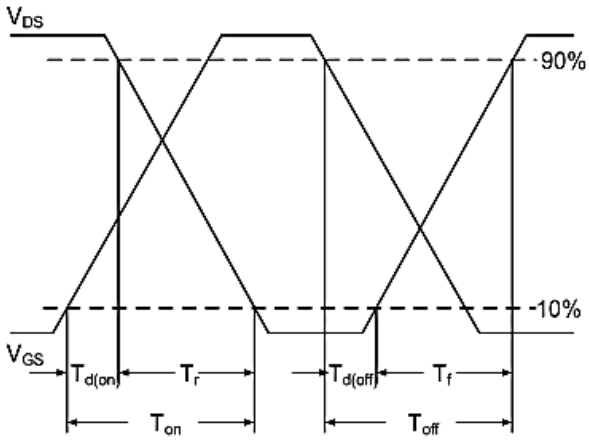


Fig.10 Switching Time Waveform

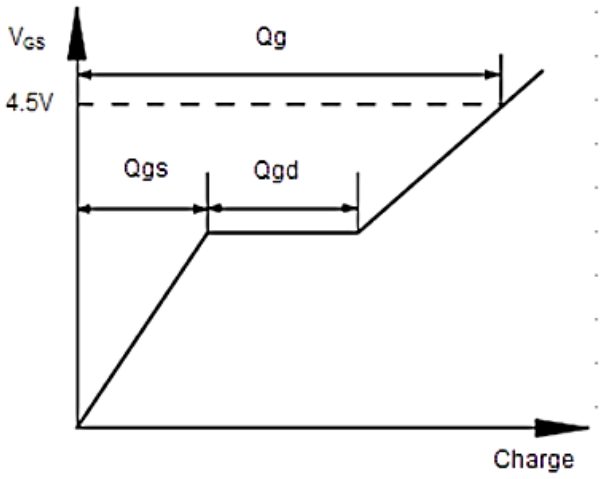


Fig.11 Gate Charge Waveform

P-Channel Typical Characteristics

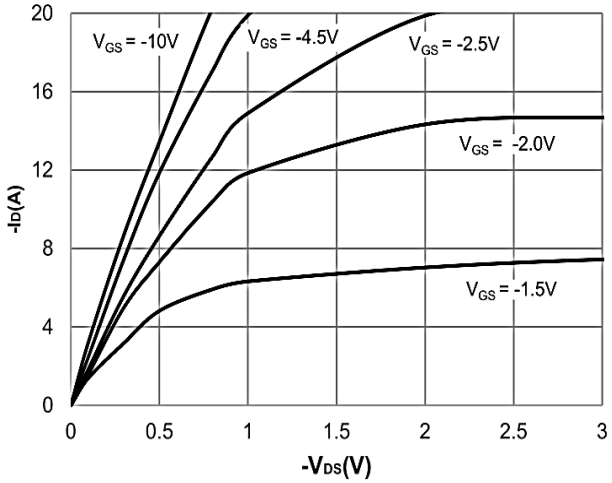


Figure 1: Output Characteristics

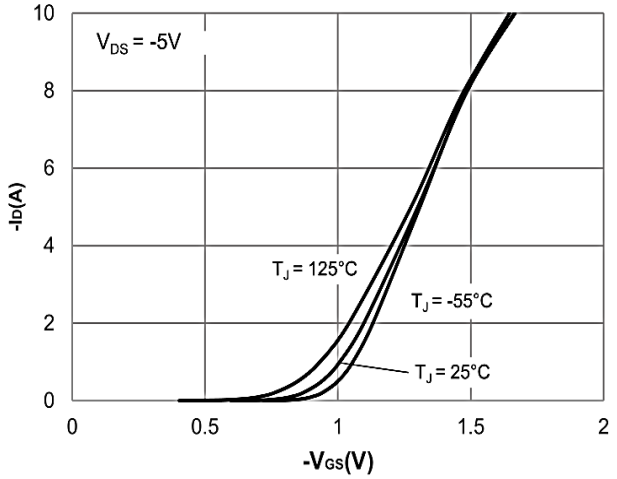


Figure 2: Typical Transfer Characteristics

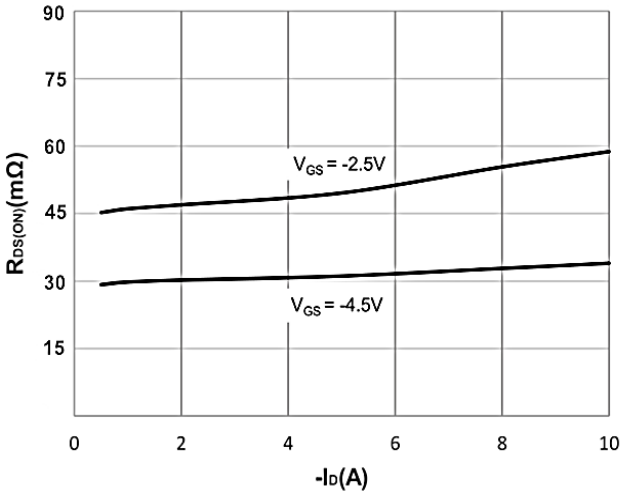


Figure 3: On-resistance vs. Drain Current

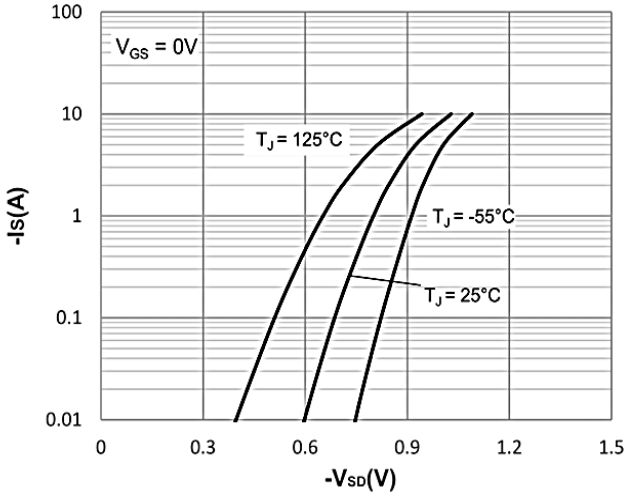


Figure 4: Body Diode Characteristics

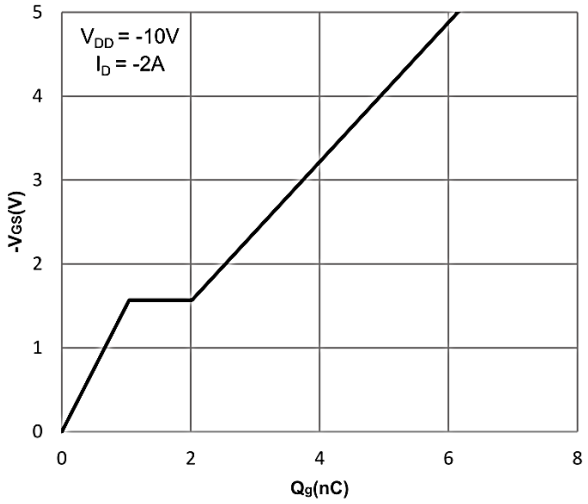


Figure 5: Gate Charge Characteristics

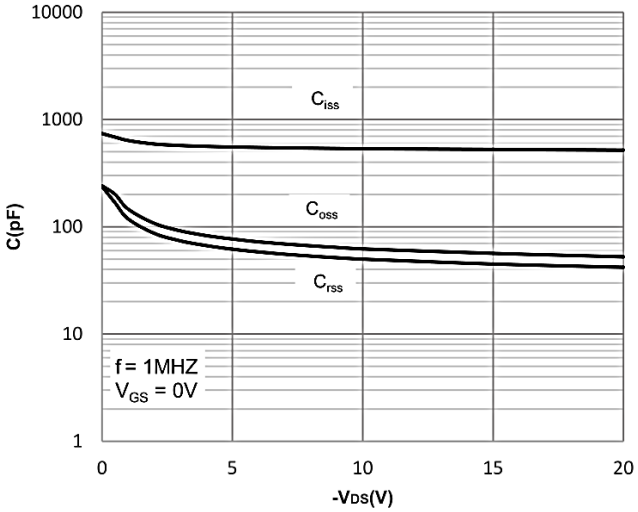


Figure 6: Capacitance Characteristics

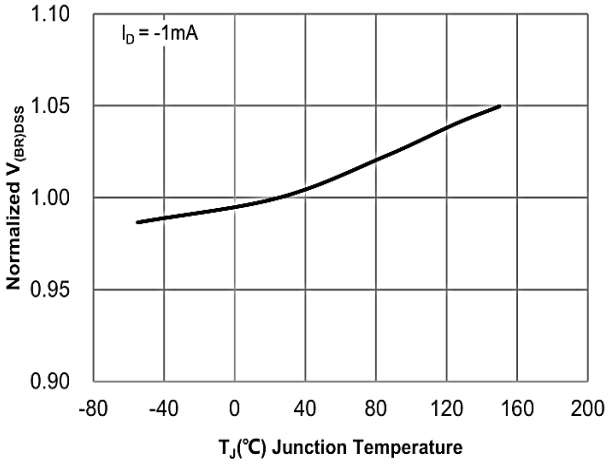


Figure 7: Normalized Breakdown voltage vs. Junction Temperature

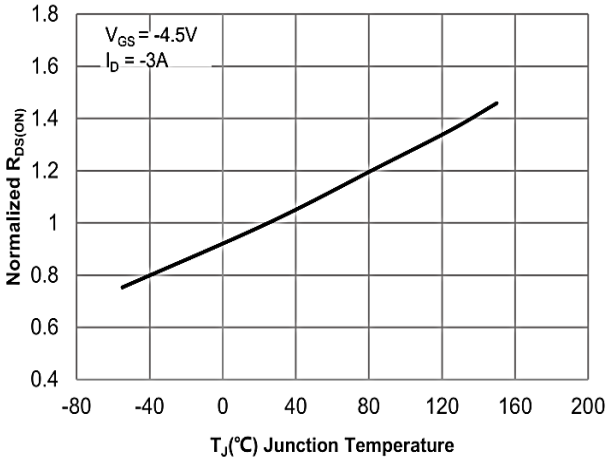


Figure 8: Normalized on Resistance vs. Junction Temperature

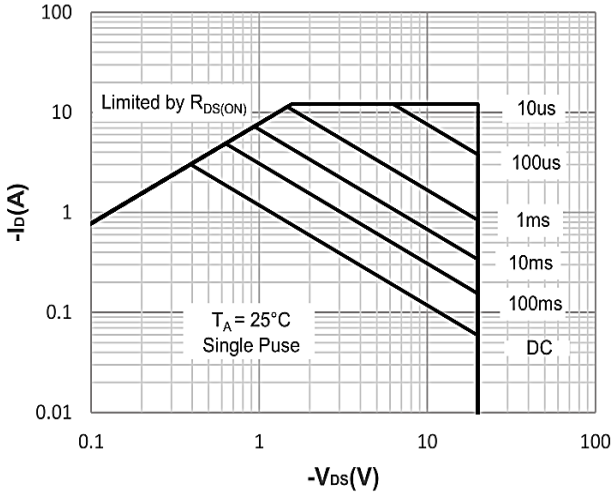


Figure 9: Maximum Safe Operating Area

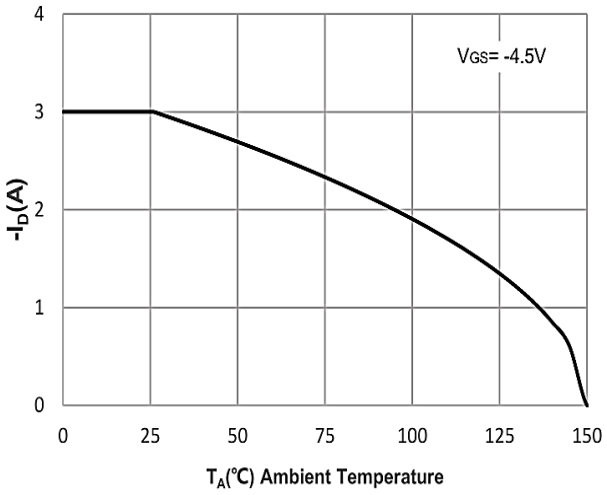


Figure 10: Maximum Continuous Drian Current vs. Case Temperature

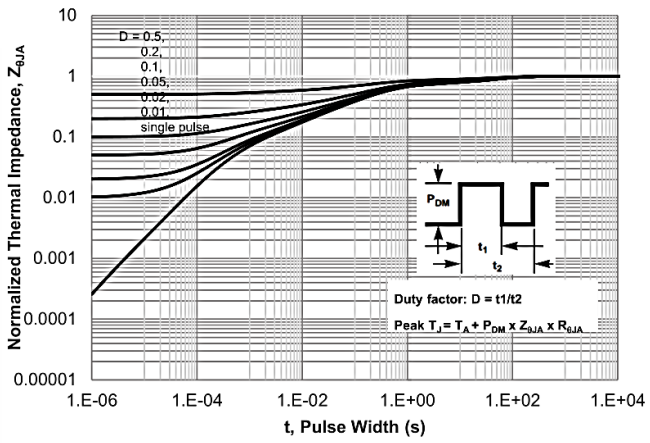


Figure 11: Normalized Maximum Transient Thermal Impedance

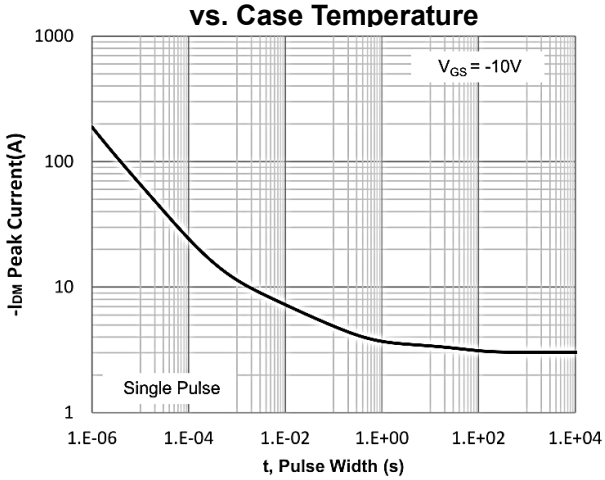
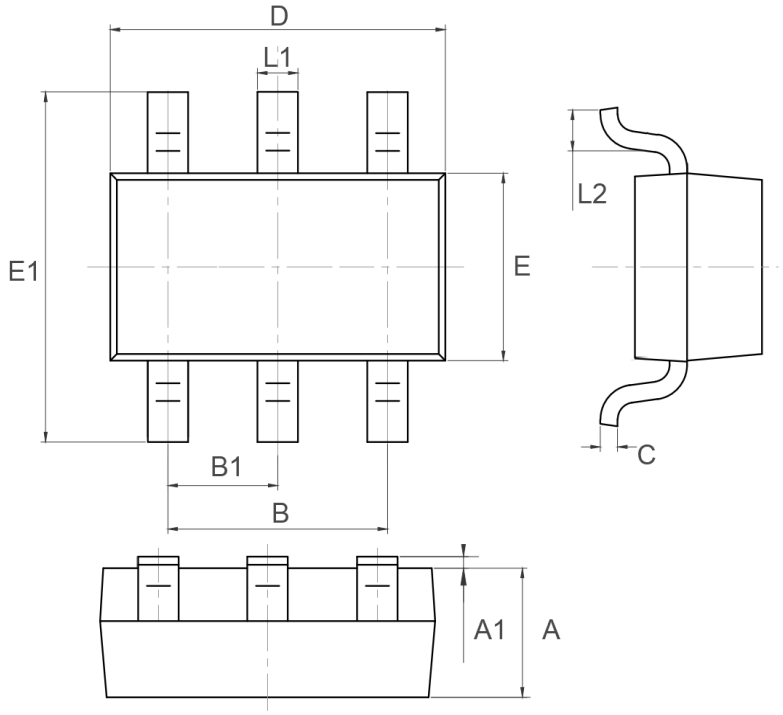


Figure 12: Peak Current Capacity

Package Mechanical Data-SOT23-6L



Symbol	Dim in mm		
	Min	Typ	Max
A	1	1.1	1.2
A1	0	0.05	0.1
B	1.8	1.9	2
B1	0.95TYP		
C	0.1	0.15	0.2
D	2.82	2.92	3.02
E	1.5	1.6	1.7
E1	2.65	2.8	2.95
L1	0.3	0.4	0.5
L2	0.3	0.45	0.6

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Edition	Date	Change
REV1.0	2024/5/21	Initial release