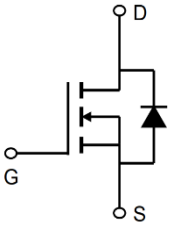
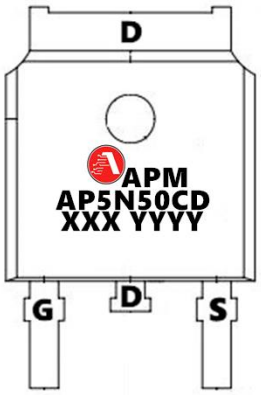
AP5N50CD

500V N-Channel Enhancement Mode MOSFET

Description

The AP5N50CD is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.





General Features

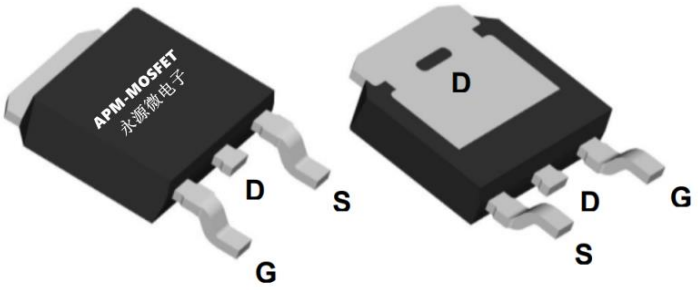
V_{DS} = 500V I_D =4.8A

$R_{DS(ON)}$ < 3.2Ω @ V_{GS}=10V （**Type：2.6Ω**）

Application

Uninterruptible Power Supply(UPS)

Power Factor Correction (PFC)



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP5N50CD	TO-252-3L	AP5N50CD XXX YYYY	2500

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Value	Unit
VDSS	Drain-Source Voltage (VGS = 0V)	500	V
ID	Continuous Drain Current	4.8	A
IDM	Pulsed Drain Current (note1)	15	A
VGS	Gate-Source Voltage	±30	V
EAS	Single Pulse Avalanche Energy (note2)	57	mJ
IAR	Avalanche Current (note1)	2.4	A
EAR	Repetitive Avalanche Energy note1)	6.4	mJ
PD	Power Dissipation (TC = 25ºC)	32.9	W
TJ, Tstg	Operating Junction and Storage Temperature Range	-55~+150	ºC
RthJC	Thermal Resistance, Junction-to-Case	6.25	ºC/W
RthJA	Thermal Resistance, Junction-to-Ambient	62.5	ºC/W

Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	500	550	--	V
IDSS	Zero Gate Voltage Drain Current	V_{DS}= 650V, V_{GS}= 0V, T_J=25ºC	--	--	1	μA
IGSS	Gate-Source Leakage	V_{GS} = ±30V	--	--	±100	nA
VGS(th)	Gate-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	2.0	3.0	4.0	V
RDS(on)	Drain-Source On-Resistance (Note3)	V_{GS} = 10V, I_D = 2.0A	--	2.6	3.2	Ω
C_{iss}	Input Capacitance	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz	--	310	--	pF
C_{oss}	Output Capacitance		--	39	--	
C_{rss}	Reverse Transfer Capacitance		--	6	--	
Q_g	Total Gate Charge	V_{DD}=400V, I_D = 3A, V_{GS} = 10V	--	8	--	nC
Q_{gs}	Gate-Source Charge		--	1.2	--	
Q_{gd}	Gate-Drain Charge		--	5	--	
td(on)	Turn-on Delay Time	V_{DD}=250V, I_D = 3A, R_G = 25Ω	--	7.8	--	ns
t_r	Turn-on Rise Time		--	33	--	
td(off)	Turn-off Delay Time		--	23	--	
t_f	Turn-off Fall Time		--	59	--	
IS	Continuous Body Diode Current	T_C = 25 ºC	--	--	3.0	A
ISM	Pulsed Diode Forward Current		--	--	12	A
V_{SD}	Body Diode Voltage	T_J = 25ºC, I_{SD} = 3A, V_{GS} = 0V	--	--	1.4	V
trr	Reverse Recovery Time	V_{GS} = 0V,I_S = 3A, di_F/dt =100A /μs	--	80	--	ns
Q_{rr}	Reverse Recovery Charge		--	1.8	--	μC

Note :

1、The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.

2、The EAS data shows Max. rating . IAS = 2.4A, VDD = 50V, RG = 25 Ω, Starting TJ = 25 ºC

3、The test condition is Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%

4、The power dissipation is limited by 150℃ junction temperature

5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

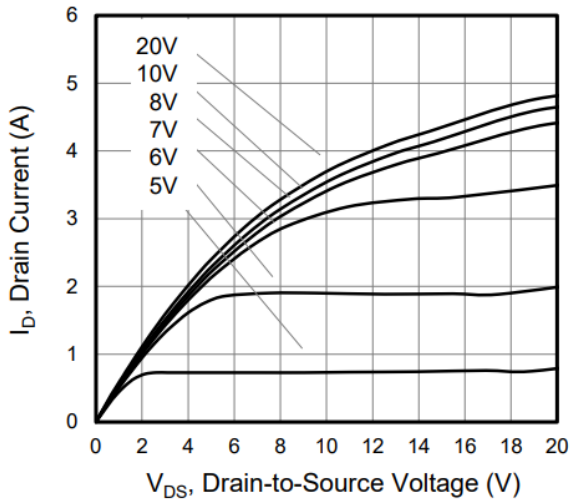


Figure 1. Output Characteristics (T J = 25ºC)

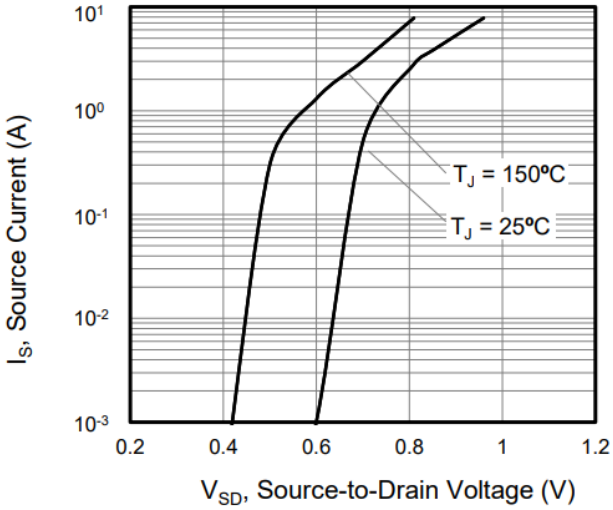


Figure 2. Body Diode Forward Voltage

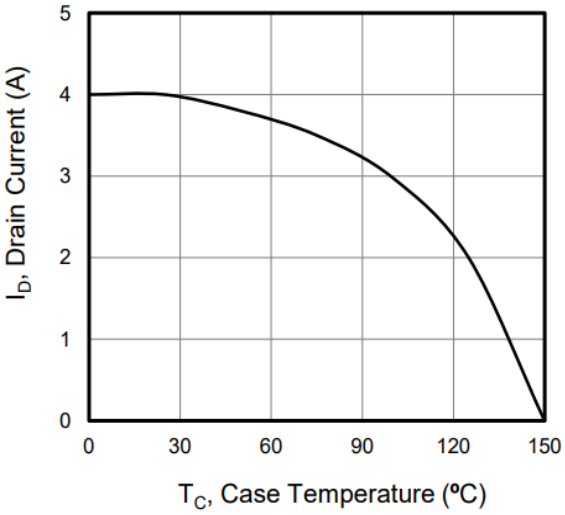


Figure 3. Drain Current vs. Temperature

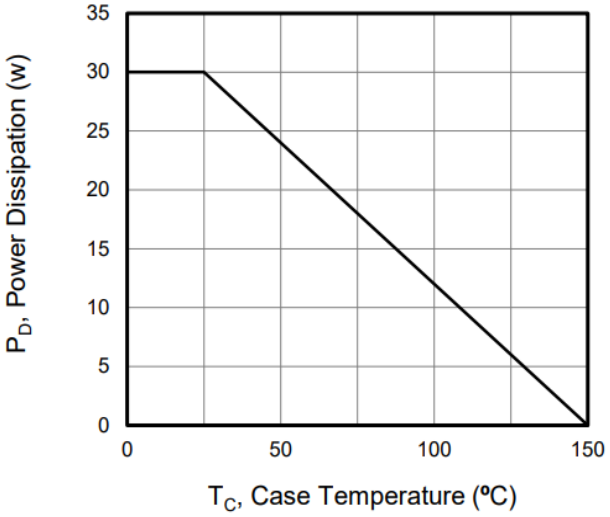


Figure 4. BV DSS Variation vs. Temperature

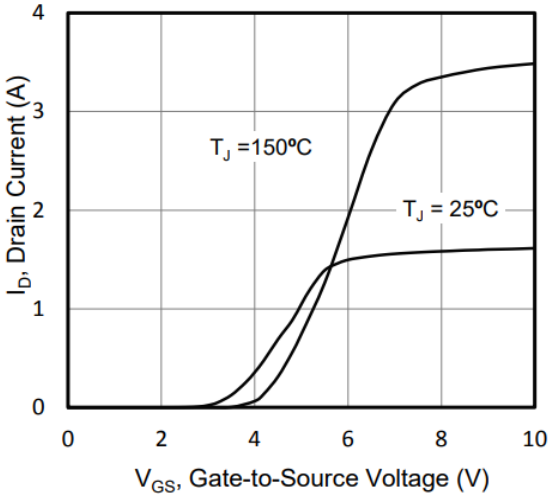


Figure 5. Transfer Characteristics

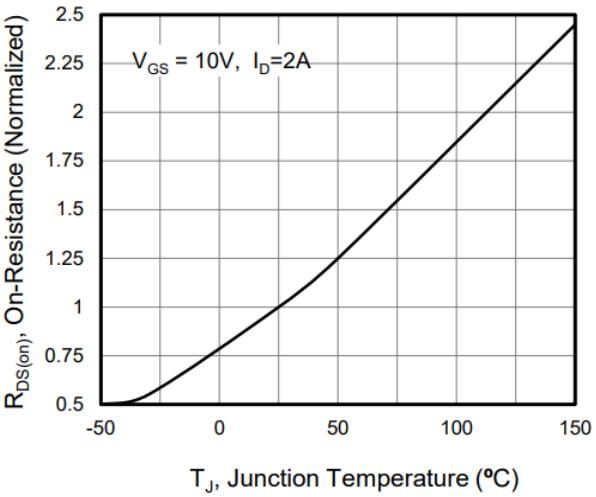


Figure 6. On-Resistance vs. Temperature

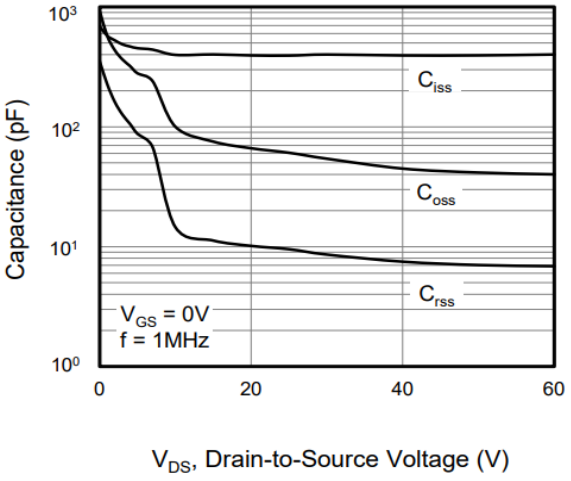


Figure 7. Capacitance

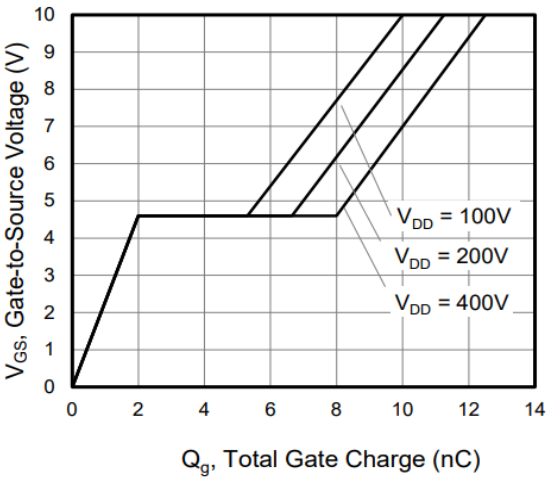


Figure 8. Gate Charge

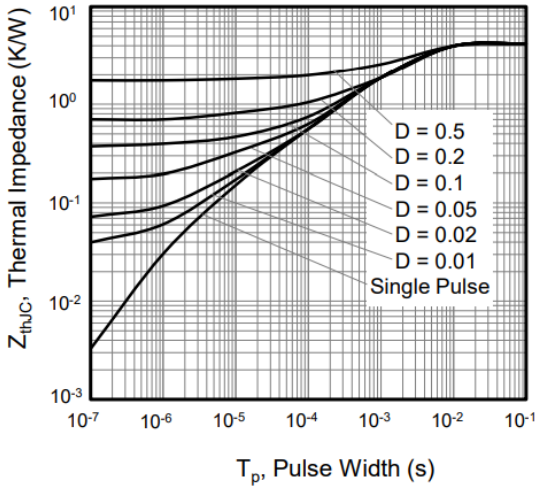
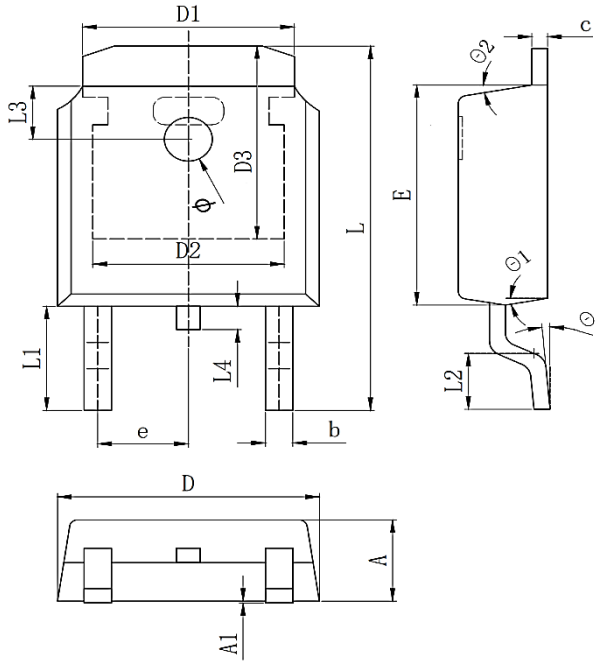


Figure 9. Transient Thermal Impedance

Package Mechanical Data-TO-252-3L



Symbol	Dim in mm		
	Min	Typ	Max
A	2.1	2.3	2.5
A1	0	0.064	0.128
b	0.64	0.75	0.86
c	0.45	0.52	0.6
D	6.4	6.6	6.8
D1	5.33REF		
D2	4.83REF		
D3	5.25REF		
E	5.9	6.1	6.3
e	2.286TYP		
L	9.8	10.1	10.4
L1	2.888REF		
L2	1.4	1.5	1.7
L3	1.65REF		
L4	0.6	0.8	1
ϕ	1.1	1.2	1.3
θ	0°		10°
θ1	5°		10°
θ2	5°		10°

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Edition	Date	Change
REV1.0	2023/4/31	Initial release