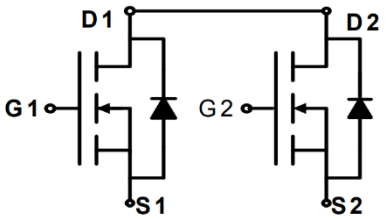
AP50H02DF3

20V N+N-Channel Enhancement Mode MOSFET

Description

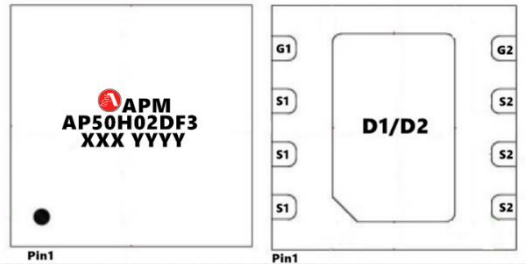
The AP50H02DF3 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.



General Features

V_{DS} = 20V I_D =50A

$R_{DS(ON)}$ < 8.5mΩ @ V_{GS}=4.5V （Type：6.2mΩ）

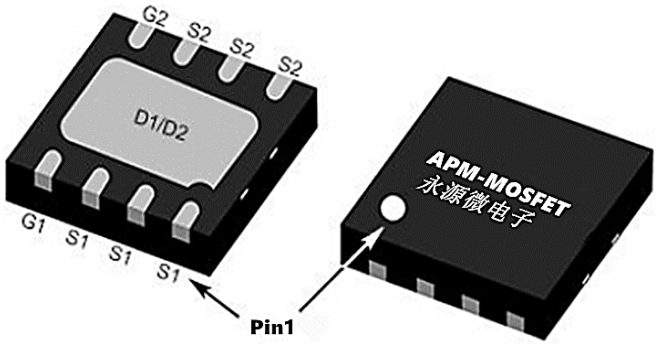


Application

3.3V MCU Drive

Load switch

Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP50H02DF3	DFN3*3-8L	AP50H02DF XXX YYYY	5000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Max.	Units
VDSS	Drain-Source Voltage	20	V
VGSS	Gate-Source Voltage	±12	V
ID@TA=25℃	Continuous Drain Current, VGS @ 4.5V	50	A
ID@TA=70℃	Continuous Drain Current, VGS @ 4.5V	30	A
IDM	Pulsed Drain Current note1	120	A
EAS	Single Pulsed Avalanche Energy note2	147.6	mJ
PD@TA=25℃	Power Dissipation	37	W
TJ, TSTG	Operating and Storage Temperature Range	-55 to +175	℃
RθJA	Thermal Resistance Junction-Ambient [1]	85	℃/W
RθJC	Thermal Resistance, Junction to Case	2	℃/W

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	20	24	-	V
IDSS	Zero Gate Voltage Drain Current	V_{DS}=20V, V_{GS}=0V,	-	-	1.0	μA
IGSS	Gate to Body Leakage Current	V_{DS}=0V, V_{GS}=±12V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	0.4	0.7	1.1	V
RDS(on)	Static Drain-Source on-Resistance note3	V_{GS}=4.5V, I_D=25A	-	6.2	8.5	mΩ
		V_{GS}=2.5V, I_D=10A	-	8.8	13	
C_{iss}	Input Capacitance	V_{DS}=10V, V_{GS}=0V, f=1.0MHz	-	1458	-	pF
Coss	Output Capacitance		-	238	-	pF
Crss	Reverse Transfer Capacitance		-	212	-	pF
Q_g	Total Gate Charge	V_{DS}=10V, I_D=25A, V_{GS}=4.5V	-	19	-	nC
Q_{gs}	Gate-Source Charge		-	3	-	nC
Q_{gd}	Gate-Drain(“Miller”) Charge		-	6.4	-	nC
td(on)	Turn-on Delay Time	V_{DS}=10V, I_D=10A, R_{GEN}=3Ω, V_{GS}=4.5V	-	10	-	ns
t_r	Turn-on Rise Time		-	21	-	ns
td(off)	Turn-off Delay Time		-	39	-	ns
t_f	Turn-off Fall Time		-	19	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	50	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	200	A
VSD	Drain to Source Diode Forward Voltage	V_{GS}=0V, I_S=30A	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	IF=20A,dI/dt=100A/μs	-	25	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	20	-	nC

Note :

1、The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、The test condition is T_J=25℃, V_{DD}=10V, V_G=4.5V, L=0.5mH, R_G=25Ω, I_{AS}=12A

4、The power dissipation is limited by 150℃ junction temperature

5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

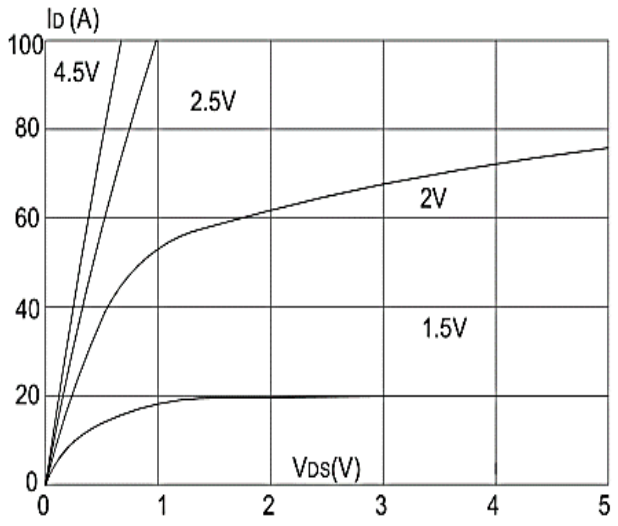


Figure1: Output Characteristics

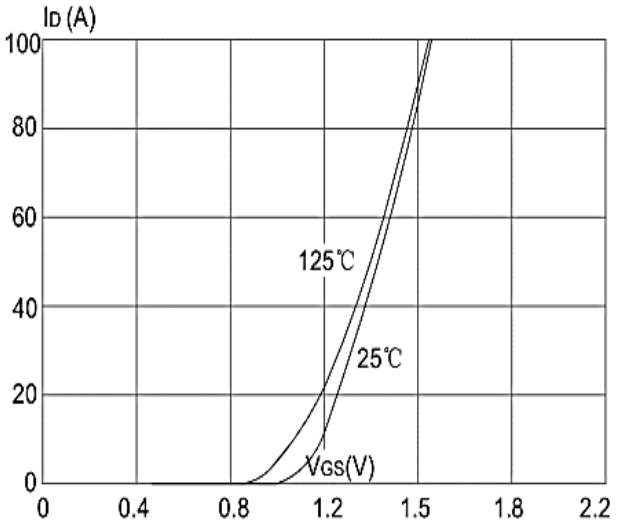


Figure 2: Typical Transfer Characteristics

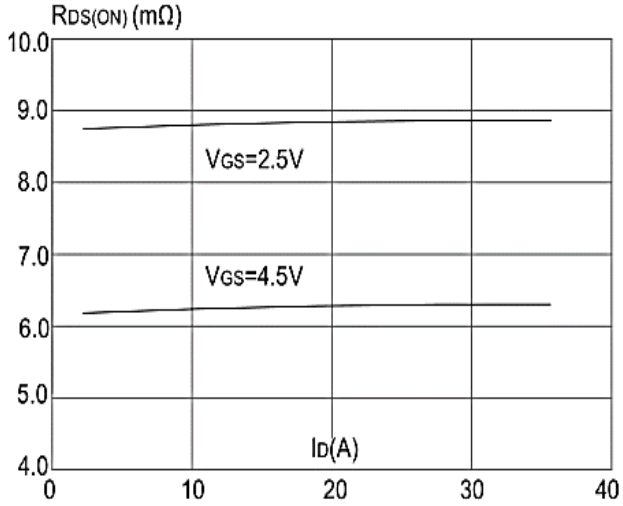


Figure 3:On-resistance vs. Drain Current

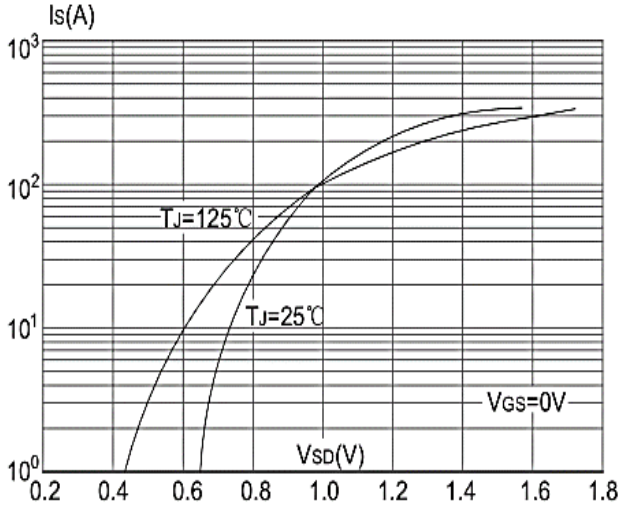


Figure 4: Body Diode Characteristics

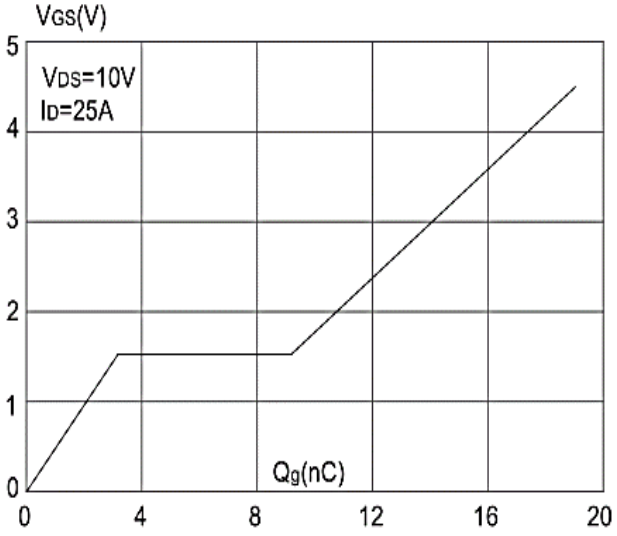


Figure 5: Gate Charge Characteristics

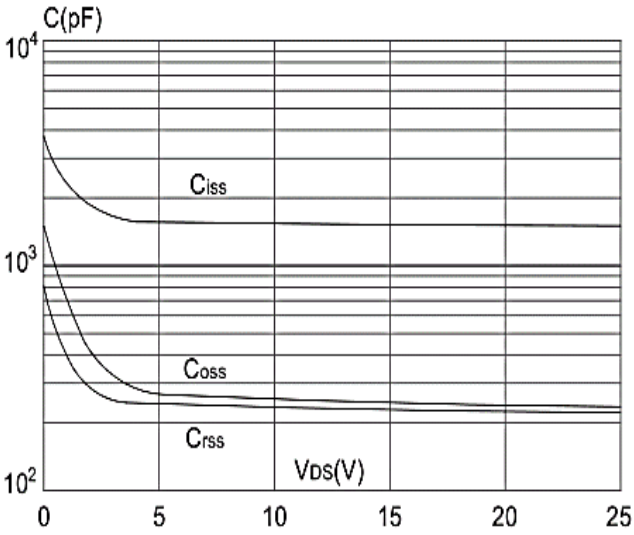


Figure 6: Capacitance Characteristics

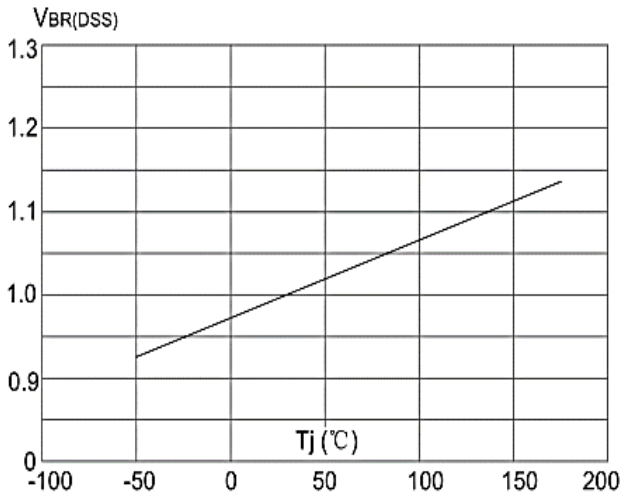


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

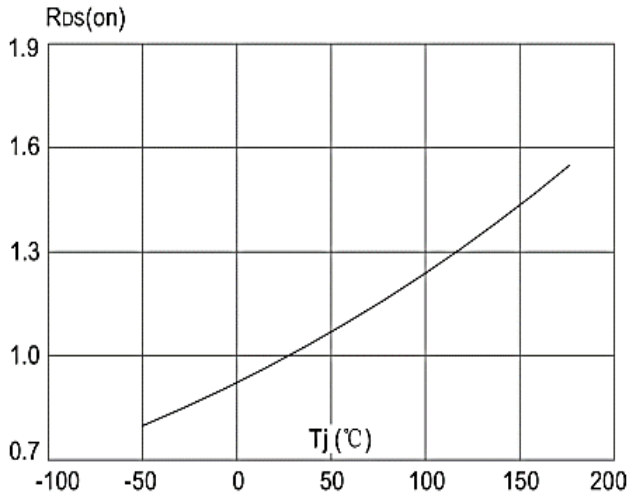


Figure 8: Normalized on Resistance vs Junction Temperature

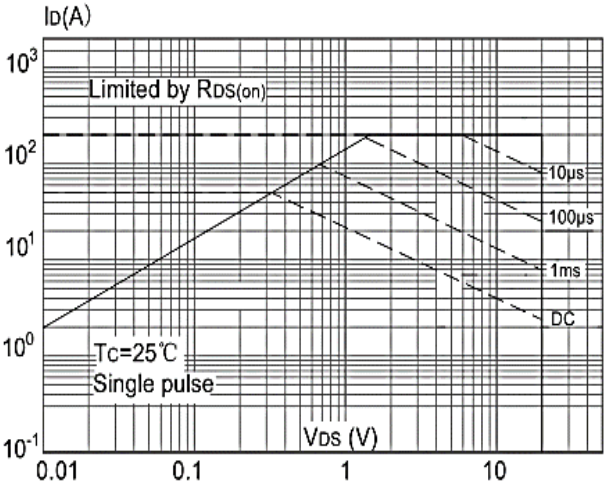


Figure 9: Maximum Safe Operating Area vs. Case Temperature

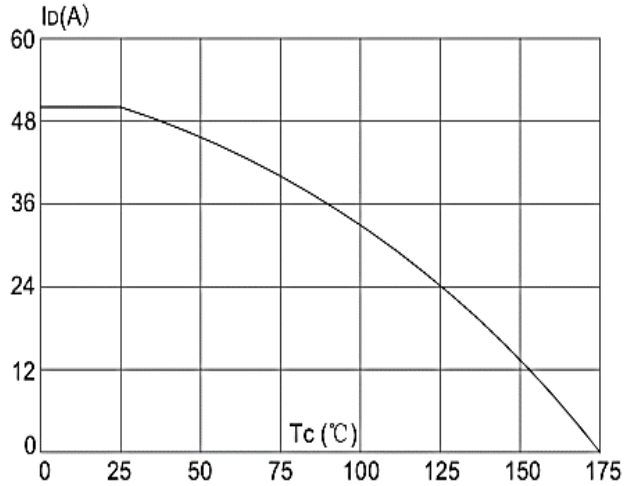


Figure 10: Maximum Continuous Drain Current

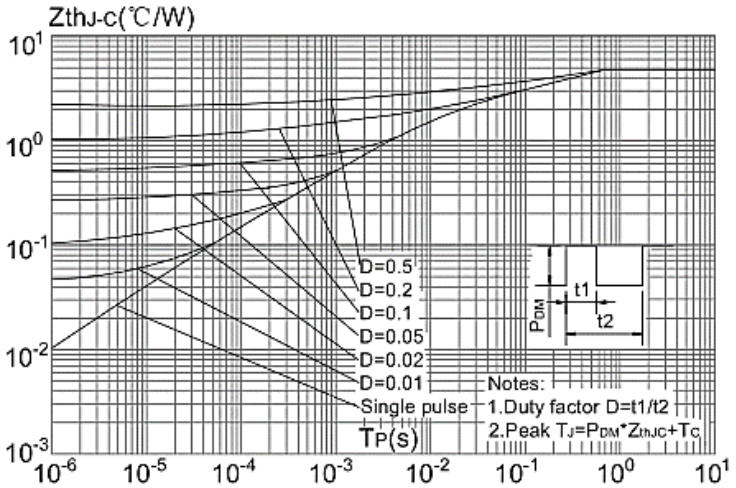
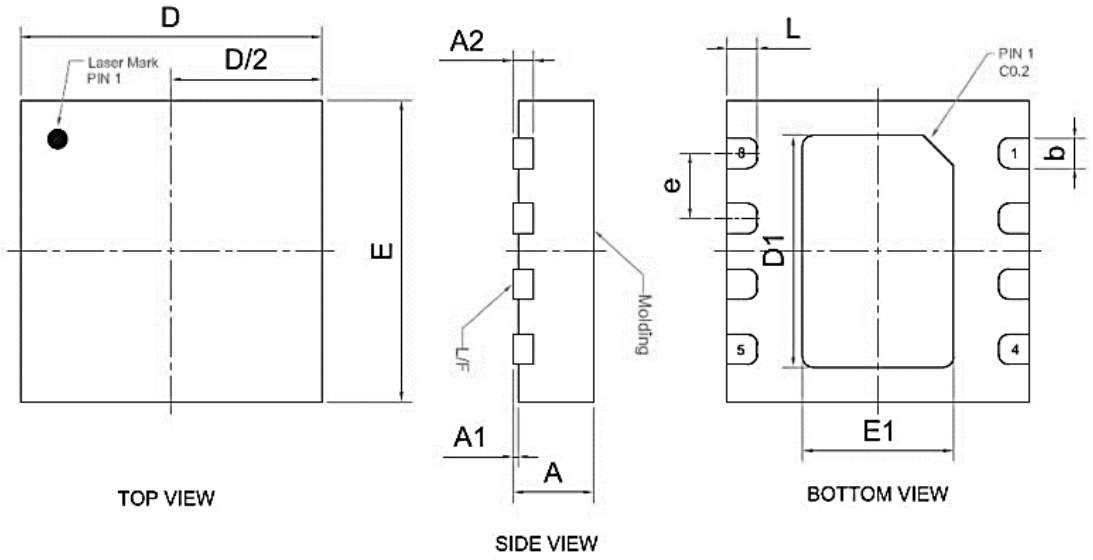


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

Package Mechanical Data-DFN3X3-8L



Symbol	Dim in mm	
	Min	Max
A	0.70	0.80
A1	0.00	0.05
A2	0.203REF	
b	0.25	0.35
D	2.90	3.10
E	2.90	3.10
D1	2.20	2.40
E1	1.40	1.60
L	0.20	0.40
e	0.65BSC	

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20V N+N-Channel Enhancement Mode MOSFET

Edition	Date	Change
REV1.0	2024/3/31	Initial release