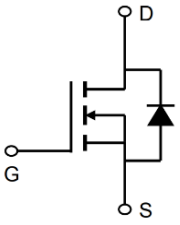
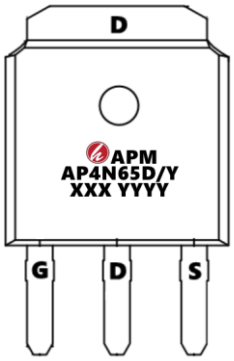
AP4N65D/Y

650V N-Channel Enhancement Mode MOSFET

Description

The AP4N65D/Y is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.





General Features

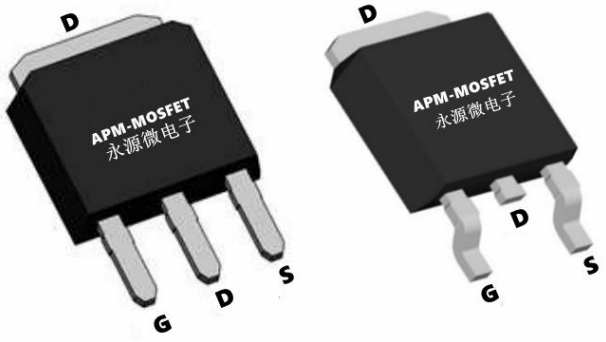
V_{DS} = 650V I_D =4A

$R_{DS(ON)}$ < 2.4Ω @ V_{GS}=10V （Type：2.0Ω）

Application

Uninterruptible Power Supply(UPS)

LED



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP4N65D	TO-252-3L	AP4N65D XXX YYYY	2500
AP4N65Y	TO-251S-3L	AP4N65Y XXX YYYY	4000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Value	Unit
VDSS	Drain-Source Voltage (V_{GS} = 0V)	650	V
ID	Continuous Drain Current	4	A
IDM	Pulsed Drain Current (note1)	25	A
VGS	Gate-Source Voltage	±30	V
E_{AS}	Single Pulse Avalanche Energy (note2)	80	mJ
IAR	Avalanche Current (note1)	16	A
E_{AR}	Repetitive Avalanche Energy note1)	4.5	mJ
P_D	Power Dissipation (T_C = 25ºC)	35	W
TJ, Tstg	Operating Junction and Storage Temperature Range	-55~+150	ºC
RthJC	Thermal Resistance, Junction-to-Case	5.1	ºC/W
RthJA	Thermal Resistance, Junction-to-Ambient	62.5	ºC/W

650V N-Channel Enhancement Mode MOSFET

Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	650			V
$\Delta BV_{DSS}/\Delta T_J$	BreakdownVoltageTemperatureCoefficient	I_D=250μA, Referenced to 25°C		0.64		V/°C
IDSS	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0 V			1	μA
		V_{DS} = 520 V, TC = 125°C			10	μA
IGSSF	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V			100	nA
IGSSR	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V			-100	nA
VGS(TH)	Gate Threshold voltage	V_{DS}=V_{GS}, I_D =250 uA	2.0		4.0	V
RDS(On)	Drain-Source on-state resistance	V_{GS}=10 V, I_D =2A, T_J = 25°C		2.0	2.4	Ω
gFS	Forward Transconductance	V_{DS}=40 V, I_D=2 A (Note 4)		3.8		S
C_{iss}	Input capacitance	V_{DS}=25V, V_{GS}=0 V, f=1.0 MHz		415		pF
C_{oss}	Output capacitance			58		pF
C_{rss}	Reverse transfer capacitance			1.4		pF
td(on)	Turn On Delay Time	V_{DD}=325V, ID=4A, R_G=25Ω (Note 4, 5)		7		ns
t_r	Rising Time			22		ns
td(off)	Turn Off Delay Time			15		ns
t_f	Fall Time			23		ns
Q_g	Total Gate Charge	V_{DS} = 520 V, ID = 4 A, V_{GS} = 10 V (Note 4, 5)		13		nC
Q_{gs}	Gate-Source Charge			4.9		nC
Q_{gd}	Gate-Drain Charge			2.3		nC
ISM	Maximum Pulsed Drain-Source Diode Forward Current				16	A
V_{SD}	Diode Forward Voltage	V_{GS}= 0 V, I_S = 4 A			1.2	V
trr	Reverse Recovery Time	V_{GS} = 0 V, I_S = 4 A, dI_F / dt = 100 A/μs Note 4)		378		ns
Q_{rr}	Reverse Recovery Charge			1.35		μC

Note :

1、The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.

2、The EAS data shows Max. rating . L=4.1Mh IAS=18A, VDD=50V, RG=25Ω, Starting TJ = 25 ºC

3、The test condition is Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%

4、The power dissipation is limited by 150℃ junction temperature

5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

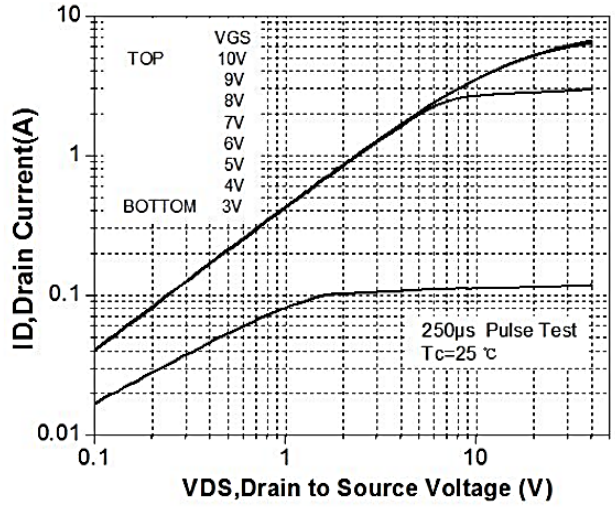


Figure 1. On-Region Characteristics

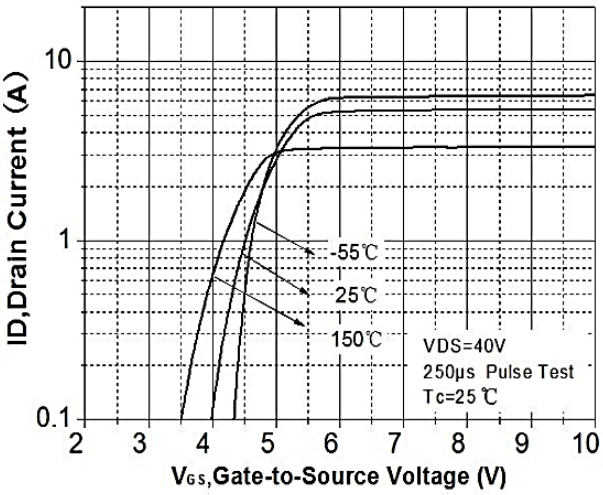


Figure 2. Transfer Characteristics

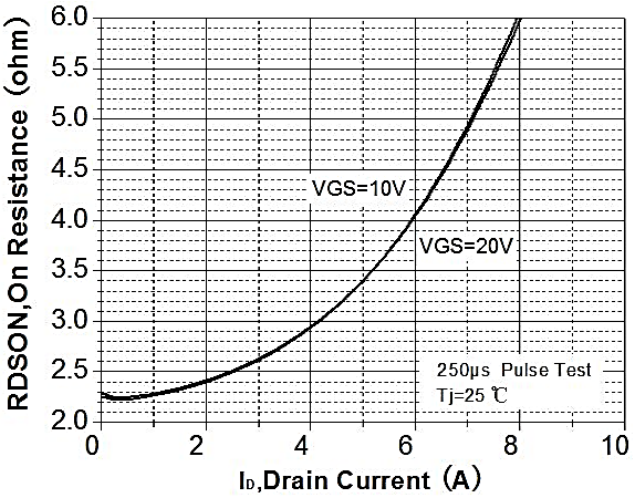


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

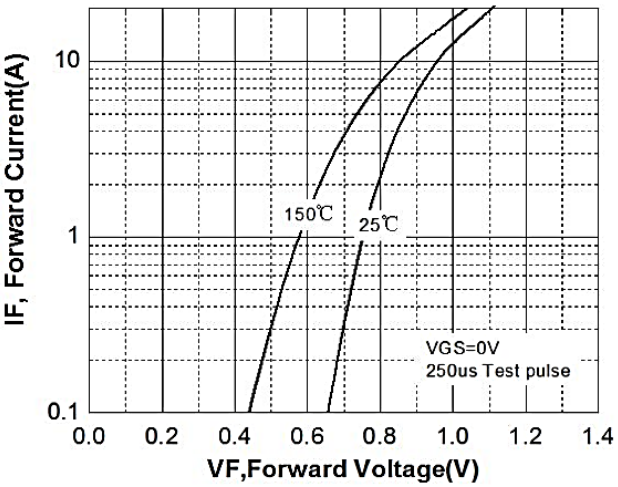


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

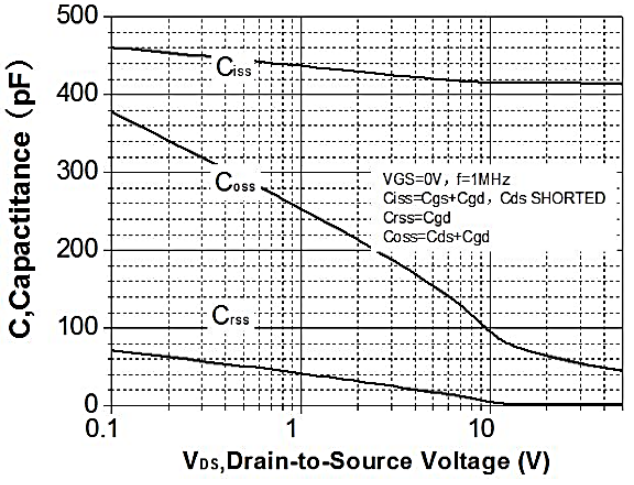


Figure 5. Capacitance Characteristics

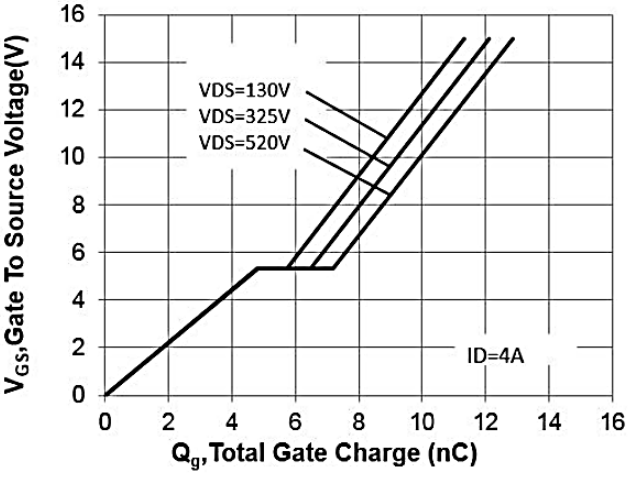


Figure 6. Gate Charge Characteristics

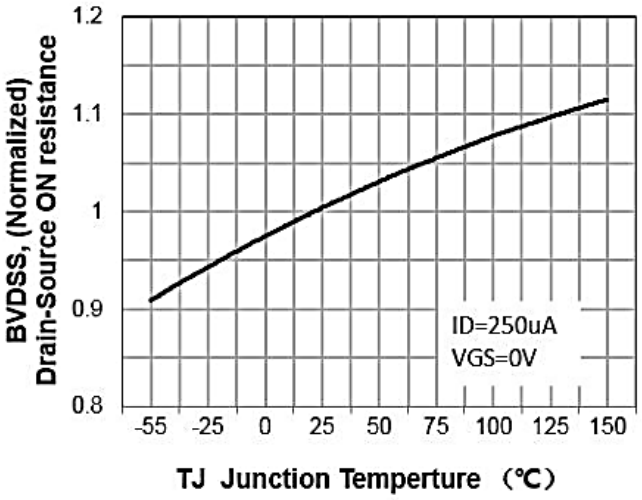


Figure 7. Breakdown Voltage Variation vs Temperature

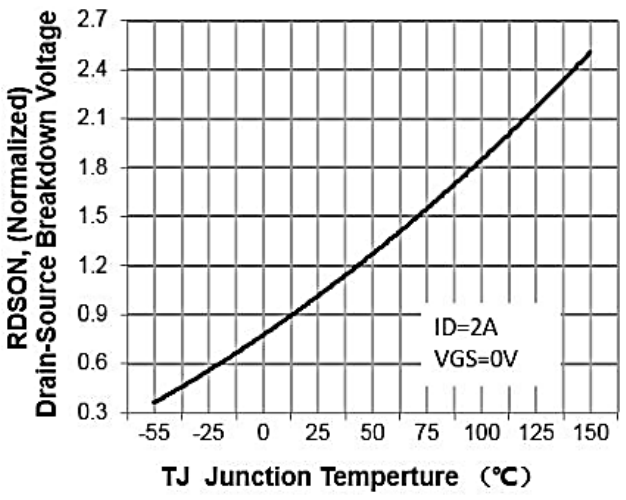


Figure 8. On-Resistance Variation vs Temperature

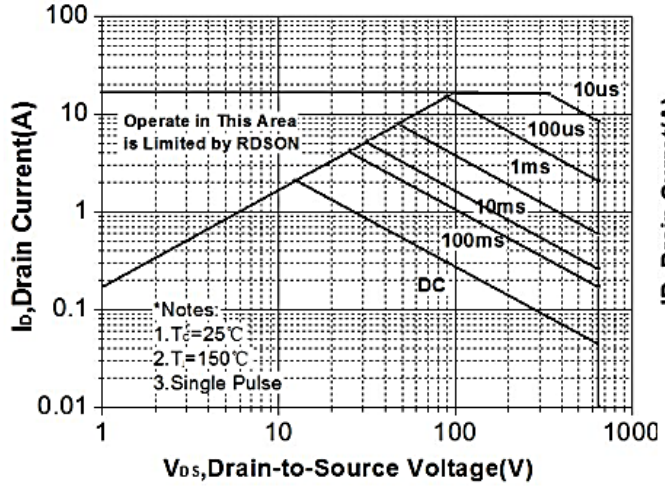


Figure 9. Maximum Safe Operating Area

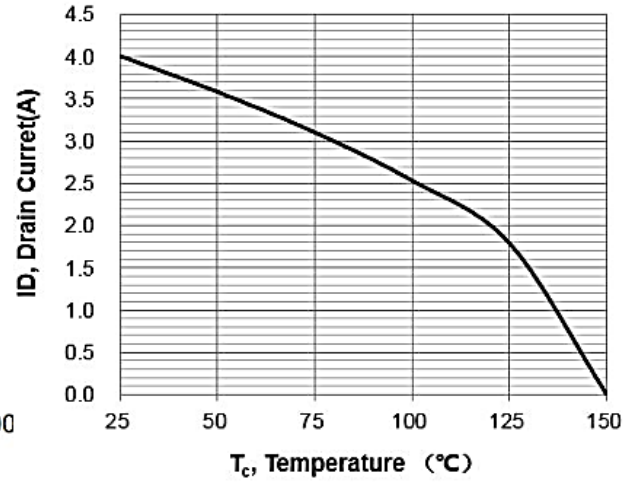


Figure 10. Maximum Drain Current vs Case Temperature

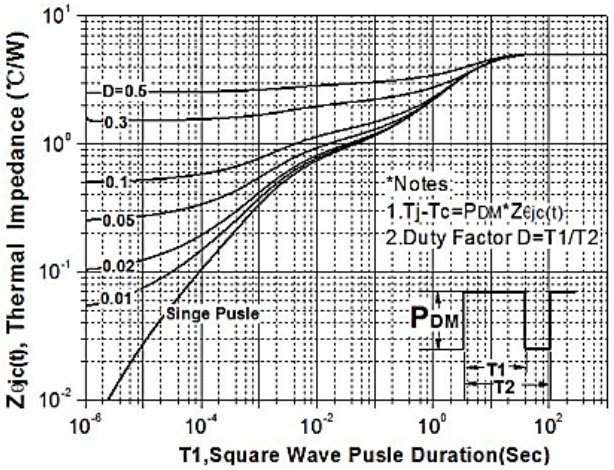
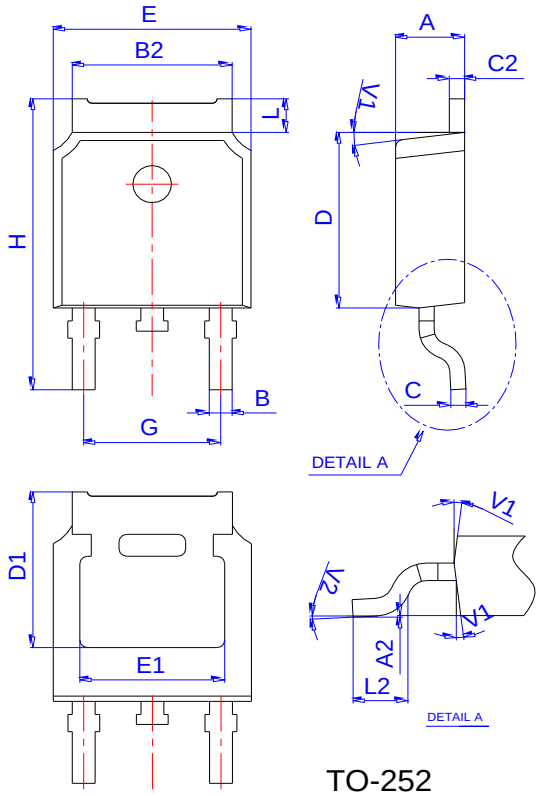


Figure 11. Transient Thermal Response Curve

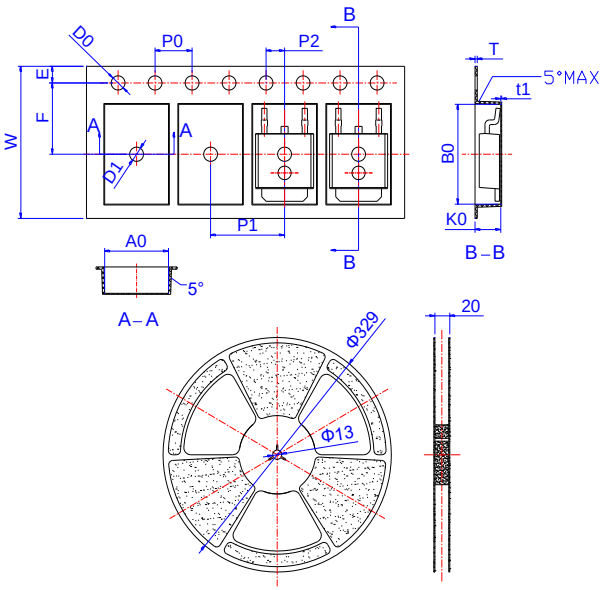
Package Mechanical Data:TO-252-3L



TO-252

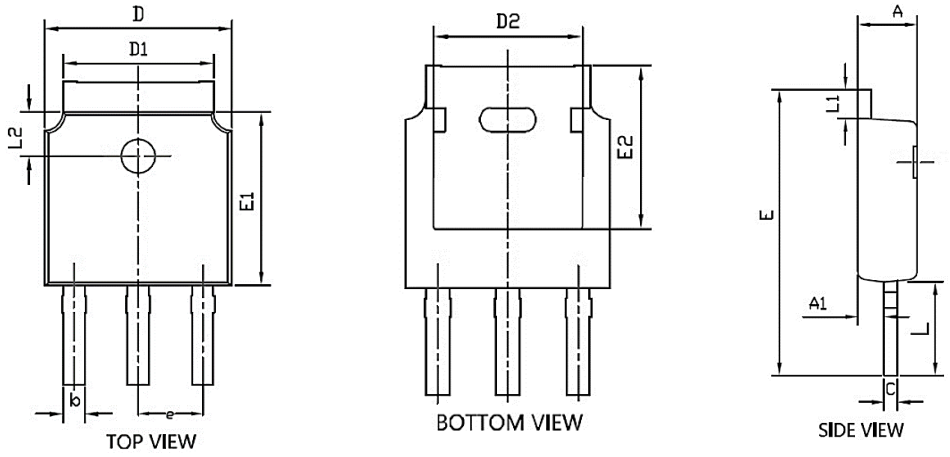
Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Reel Specification-TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583

Package Mechanical Data-TO-251S-3L



Symbol	Common		
	mm		
	Mim	Nom	Max
A	2.2	2.3	2.4
A1	0.9	1.0	1.1
b	0.66	0.76	0.86
C	0.46	0.52	0.58
D	6.50	6.6	6.7
D1	5.15	5.3	5.45
D2	4.6	4.8	4.95
E	10.4	----	11.5
E1	6.0	6.1	6.2
E2	5.400REF		
e	2.286BSC		
L	3.5	4.0	4.3
L1	0.9	---	1.27
L2	1.4	---	1.9

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650V N-Channel Enhancement Mode MOSFET

Edition	Date	Change
Rve1.0	2020/1/31	Initial release
Rve1.1	2022/10/22	Format change