AP4470
Ultra-Low Power Step-up DC/DC Converter
for Energy Harvesting Applications

1. General Description

The AP4470 is an ultra-low consumption power management chip that integrates a step-up DC/DC converter and hysteresis comparators. The AP4470 requires only 0.20V input to start boosting without the need for an external transformer. The AP4470 has hysteresis operation switch that can control the power supply for target devices (sensors, wireless modules, LEDs) while protecting external storage (capacitors), and the target.

1μW DC input is enough to startup the AP4470. Converted output is stored to external storage device and the AP4470 monitors the device. When the voltage of external storage reaches 3.3V, the AP4470 automatically starts supplying to the target device and stops supplying if the voltage drops down to 2.6V. Overvoltage protection function works at 3.55V.
2-types of power indicators offer reset function and trigger switch function with zero standby current. The trigger(Startup FLAG) is achieved by a signal that is output when DC/DC converter becomes active. The reset(Power Good) is a signal that indicates the AP4470 starts supplying, which means external storage's voltage reaches 3.3V.

The AP4470 is ideally suited for several μW to several mW sources energy harvesting. This provides a self-powered wireless sensor node with simple hardware design.

2. Features

- ☐ Startup voltage : Cold start from 0.20V typical
- ☐ DC/DC switching frequency : 60kHz typical at VIN=0.4V
- ☐ Operation Voltage : up to 1.0V (VIN)
  up to 5.5V (VDD1 / VDD2)
  Operation temperature : -30 ~ +85ºC
- ☐ Power Consumption
  DC/DC converter is active : 7μA typical at VIN=0.4V
  DC/DC converter is off : 0.5μA typical at VIN=0.4V
  (The AP4470 supplies power including over charge protection current)
- ☐ DC/DC active indicator
- ☐ Power Good indicator
- ☐ DC/DC disable function
- ☐ On-chip rectifier diode for DC/DC converting (using external diode is also available)
- ☐ Support high impedance power sources up to tens of kΩ
- ☐ Package : 20-pin HWQFN (3.0mm×3.0mm×0.75mm 0.5mm pitch)

3. Applications

- ☐ Energy Harvesting
  - ➢ Wireless Sensor Node
  - ➢ Wearable and Portable Device
- ☐ Zero standby current trigger switch
- ☐ Example of Energy Harvester (several μW to several mW sources)
  - ➢ Ambient Light, Single cell solar battery
  - ➢ Vibration
  - ➢ Thermal
  - ➢ Microbial Fuel Cell

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5. Block Diagram

5.1. Block Diagram

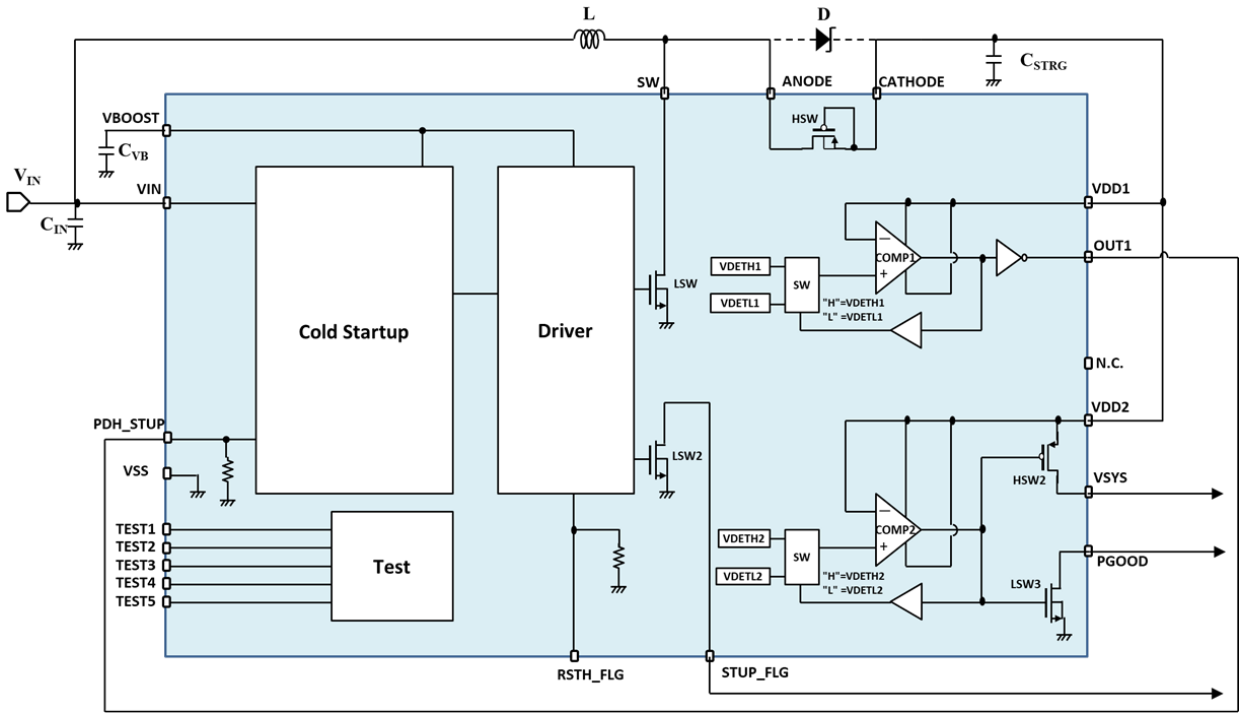


Figure 5.1.1 AP4470 Block Diagram

5.2. Block Function

Block	Description
Cold Startup	The cold startup becomes active by DC voltage from VIN input. This block does DC/DC converting to VBOOST and output converted input to the driver block.
Driver	The driver delivers converted input by the cold startup to the LSW and the LSW2.
LSW	Following output from the driver, the LSW works as a current sink from SW pin.
LSW2	Triggered by a DC/DC converting active signal from the driver, and then output “Low” to STUP_FLG pin.
HSW	The HSW rectifies input from ANODE pin to CATHODE pin. (ANODE pin = anode, CATHODE pin= cathode for diode connection)
COMP1	The COMP1 is a hysteresis comparator circuit for VDD1 input voltage detection. The reference voltages VDETH1 and VDETL1 are provided by an internal circuit. The comparison result is output to OUT1.
COMP2	The COMP2 is a hysteresis comparator circuit for VDD2 input voltage detection. The reference voltages VDETH2 and VDETL2 are provided by an internal circuit. The comparison result is used to control on-chip HSW2 switch and an open drain LSW3 switch.

6. Pin Configuration and Function

6.1. Pin Configuration

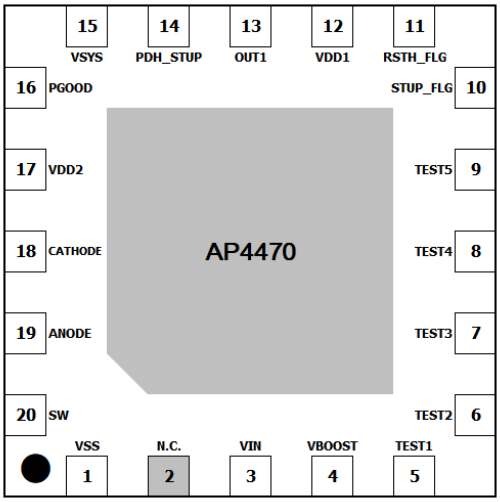


Figure 6.1.1 Pin Configuration (Top view)

6.2. Pin Function

Table 6.2.1 Pin Function Description

Pin #	Pin Name	I/O	Status when PDH_STUP = " High "	Function
1	VSS	G	-	Ground
2	N.C.	-		No connect pin
3	VIN	P	-	Power supply input
4	VBOOST	AO	Hi-Z	This pin is not for current supply to an external circuit.
5	TEST1	-	-	For test purposes. This pin should be connected to VSS.
6	TEST2	-	-	For test purposes. This pin should be connected to VSS.
7	TEST3	-	-	For test purposes. This pin should be connected to VSS.
8	TEST4	-	-	For test purposes. This pin should be connected to VSS.
9	TEST5	-	-	For test purposes. This pin should be connected to VSS.
10	STUP_FLG	AO	Hi-Z	DC/DC converting start flag output pin. Open drain output. STUP_FLG pin outputs "Low" when DC/DC converting is active.
11	RSTH_FLG	DI	10MΩ Pull-down	Disable pin for DC/DC converting start flag function. (10MΩ Pull-down) Enable= "High", Disable="Low"
12	VDD1	P	-	Power supply for COMP1
13	OUT1	DO	-	COMP1 Output pin
14	PDH_STUP	DI	10MΩ Pull-down	Disable pin for the cold startup circuit. (10MΩ Pull-down) Enable= "High" (Cold Startup circuit power down)

15	VSYS	AO	-	HSW2 open drain output of COMP2 This pin is for system power supply
16	PGOOD	AO	-	LSW3 open drain output of COMP2 This pin is for Power Good indicator
17	VDD2	P	-	Power supply for COMP2
18	CATHODE	AO	Hi-Z	On-chip diode cathode pin
19	ANODE	AI	Hi-Z	On-chip diode anode pin
20	SW	AI	Hi-Z	LSW drain pin of DC/DC converter switch
-	TAB	-	-	Connecting the exposed pad (EPAD) that is located on the bottom of the package to VSS is recommended. The pad can be left floating if needed.

AI: Analog input pin	AO: Analog output pin	DI: Digital input pin
DO: Digital output pin	P: Power supply pin	G: Ground pin

All digital input pins must NOT be left open.

6.3. The connection of unused pins

Please follow the tables below for unused AP4470 pins.

- In the case of the on-chip diode (HSW) is not used

Table 6.3.1 On-chip diode is not used

Pin #	Name	I/O	Connection	Remarks
18	CATHODE	AO	Open or VSS	
19	ANODE	AI	Open or VSS	

- In the case of the STUP_FLG is not used

Table 6.3.2 The STUP_FLG is not used

Pin #	Name	I/O	Connection	Remarks
10	STUP_FLG	AO	Open	Open drain output
11	RSTH_FLG	DI	VSS	

- In the case of the COMP1 is not used

Table 6.3.3 COMP1 is not used

Pin #	Name	I/O	Connection	Remarks
12	VDD1	P	Open	
13	OUT1	DO	Open	

- In the case of the COMP2 is not used

Table 6.3.4 COMP2 is not used

Pin #	Name	I/O	Connection	Remarks
15	VSYS	AO	Open	
16	PGOOD	AO	Open	
17	VDD2	P	Open	

7. Absolute Maximum Ratings

Table 7.1 Absolute Maximum Ratings

(VSS=0V; *1)

Parameter		Symbol	Min.	Max.	Unit
Power Supply Volgtage	VIN pin VDD1 pin VDD2 pin	V_{IN}	-0.3	6.5	V
Analog Pin Voltage	ANODE pin SW pin	V_{AIN}	-0.3	6.5	V
Digital Pin Voltage	RSTH_FLG pin PDH_STUP pin	V_{DIN}	-0.3	6.5	V
Input and output current (*2)		I_{IN}	-100	+100	mA
Power dissipation (*3)		Pd	-	2.33 (EPAD->VSS) 0.99 (EPAD->Float)	W
Storage Temperature		T_{STG}	-55	+150	°C
Junction Temperature		T_J	-55	+125	°C

Notes:

*1. All voltages are with reference to VSS = 0 V

*2. This specification is for all pins including VIN, VDD1, VDD2. Positive direction is input to pins.

*3. 74mm□-1.6t-4 layers FR-4 PCB using Sn-3.0Ag-0.5Cu solder.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

8. Recommended Operating Conditions

Table 8.1 Recommended Operating Conditions

(VSS=0V; *4)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operation Temperature	Ta	-30		+85	ºC
Power Supply Volgtage	VIN	-		1.0	V
	VDD1	1.2		5.5	V
	VDD2	1.2		5.5	V

Note:

*4. All voltages are with reference to VSS = 0 V

WARNING: The specifications are applicable within operating range (supply voltage/operating temperature) specified below.

9. Digital DC Characteristics

Table 9.1 Digital DC Characteristics

(VSS=0V; *5)

Parameter		Symbol	Min.	Typ.	Max.	Unit
High level input voltage	(*6) (*7)	V_{IH}	2.0	-	-	V
Low level input voltage	(*6) (*7)	V_{IL}	-	-	0.2×VIN	V
High level input current	V_{IH}= 2.0V (*6) (*7)	I_{IH}	0.05	0.2	0.8	μA
Low level input current	V_{IL}= 0V (*6) (*7)	I_{IL}	-1	-	+1	μA
High level output Voltage	I_{OH}=+100μA (*8)	V_{OH}	0.8×VDD1	-	-	V
Low level output voltage	I_{OL}=-100μA (*9)	V_{OL}			0.2×VDD1	V

Notes:

*5. All voltages are with reference to VSS = 0 V
*6. Digital Input pins: RSTH_FLG, PDH_STUP
*7. There is a protection diode to VDD1.
When higher input than VDD1 voltage is applied, the pin pulls current to the IC.
*8. Digital output pins: OUT1, VDD1 ≧ (V_{DETH1} + 0.1V) = 3.65V
*9. Digital output pins:OUT1, VDD1 ≦ (V_{DETL1} – 0.1V) = 3.35V

10. Electrical Characteristics

Unless otherwise noted, specifications apply for conditions of
Ta = -30 ~ +85ºC,
Load condition : Specified on Chapter 12 unless otherwise specified.

Table 10.1 Analog Characteristics

Parameter		Symbol	Min.	Typ.	Max.	Unit	Description
Cold Startup							
Minimum Input Voltage for Cold Start (*10)		V_{INSTUP}	-	0.20	0.30	V	Ta≧+25ºC
			-	-	0.40	V	
Minimum Input Voltage DC/DC converting up to 3.3V is completed (*11), (*12)		V_{INDCDC}	-	0.24	-	V	Ta=+25ºC
Switching Frequency		f_{SW}	-	60	-	kHz	VIN=0.4V Ta= +25ºC
Low Side Switching Time		T_{ON}	0.75	1.25	1.75	µs	VIN=0.4V
Hysteresis comparator 1 (COMP1)							
Detection Voltage “High”		V_{DETH1}	3.45	3.55	3.595	V	Ta≧+25ºC
Detection Voltage ”Low”		V_{DETL1}	3.35	3.45	3.55	V	Ta≧+25ºC
Hysteresis (V_{DETH1}-V_{DETL1})		V_{HYS1}	0.02	0.10	0.18	V	Ta≧+25ºC
Hysteresis comparator 2 (COMP2)							
Detection Voltage “High”		V_{DETH2}	3.20	3.30	3.40	V	Ta≧+25ºC
Detection Voltage ”Low”		V_{DETL2}	2.50	2.60	2.70	V	Ta≧+25ºC
Hysteresis (V_{DETH2}-V_{DETL2})		V_{HYS2}	0.62	0.70	0.78	V	Ta≧+25ºC
HSW2 On-resistance		R_{ONP}	-	1.5	3.5	Ω	I_{OUT}=10mA I_{OUT} : output from VSYS pin
Current Consumption (*16)							
Quiescent current with over voltage protection consumption (*13)		I_{DD0}	-	0.45	-	µA	VIN=0.2V VDD1=VDD2=3.55V PDH_STUP=3.55V
			-	0.50	6	µA	VIN=0.4V VDD1=VDD2=3.55V PDH_STUP=3.55V
Operation Current	Self consumption (*14) + COMP1/2 consumption	I_{CORE}	-	0.15	-	µA	VIN=0.2V VDD1=VDD2=3.55V PDH_STUP=0V
			-	7	50	µA	VIN=0.4V VDD1=VDD2=3.55V PDH_STUP=0V
	Switching Current (*12) (*15)	I_{SW}	-	3	-	µA	VIN=0.2V VDD1=VDD2=3.55V PDH_STUP=0V
			-	400	-	µA	VIN=0.4V VDD1=VDD2=3.55V PDH_STUP=0V

Notes:
*10. The voltage that STUP_FLG pin outputs “Low”.
*11. On-chip diode (HSW) is used.
COMP1 and COMP2 are active. A 330µF/25V electrolytic capacitor is connected to C_{STRG}.
*12. Guaranteed by design (Not tested)
*13. Including high level input current I_{IH} that is described on Table 9.1 I_{IH}=0.355µA (PDH_STUP pin=3.55V)
*14. Power consumption for VIN pin.
*15. Sink current for SW pin
*16. VSYS pin and OUT1 pin drive currents, PGOOD pin and STUP_FLG pin sink currents are NOT included.

11. Description

11.1. Hysteresis comparator 1 (COMP1)

11.1.1 When VDD1 voltage is increasing (Up phase)

The OUT1 pin will be in undefined status when VDD1 voltage is from VSS to AP4470 minimum operating voltage(1.2V).
As Chapter 11.3.1 and 11.3.2 described, the AP4470 won't accidentally stop DC/DC converting because the PDH_STUP pin is set to "Low" by the on-chip pull-down resistor of PDH_STUP under recommended circuit design.
The OUT1 outputs VSS when VDD1 volgate exceeds minimum operating voltage. When VDD1 voltage reaches to the detection voltage (VDETH1), OUT1 outputs VDD1 voltage.

11.1.2 When VDD1 voltage is decreasing (Down phase)

When VDD1 voltage is higher than the detection voltage (VDETL1), OUT1 outputs VDD1 volatge.
When VDD1 goes under the detection voltage (VDETL1), OUT1 outputs VSS. OUT1 becomes Hi-Z when VDD1 voltege becomes lower than AP4470 minimum operating voltage(1.2V).
Following Figure 11.1.1 shows Hysteresis comparator1 functions.

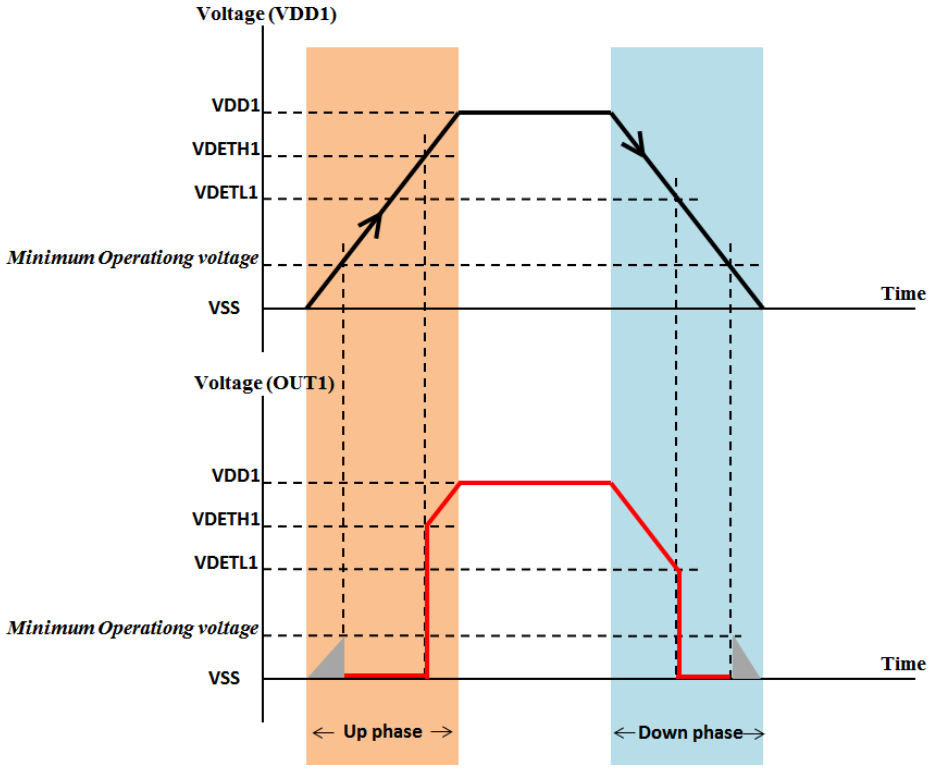


Figure 11.1.1 COMP1 Voltage detection

11.2. Hysteresis comparator 2 (COMP2)

The COMP2 controls on-chip HSW2 switch and open drain LSW3 based on voltage detection results. VSYS pin and PGOOD pin output Hi-Z when VDD2 voltage is from VSS to AP4470 minimum operating voltage(1.2V).

11.3. Startup to DC/DC operation

Figure 11.3.1 shows a typical circuit design. The description of AP4470 functions on this document is based on this circuit.
The AP4470 DC/DC converting function is shown in Figure 11.3.2. The DC/DC converting sequence is shown in Figure 11.3.3 and Figure 11.3 4.
VSYS2 which pull up STUP_FLG is external system power supply. Following Chapter 11.5 describes detail.

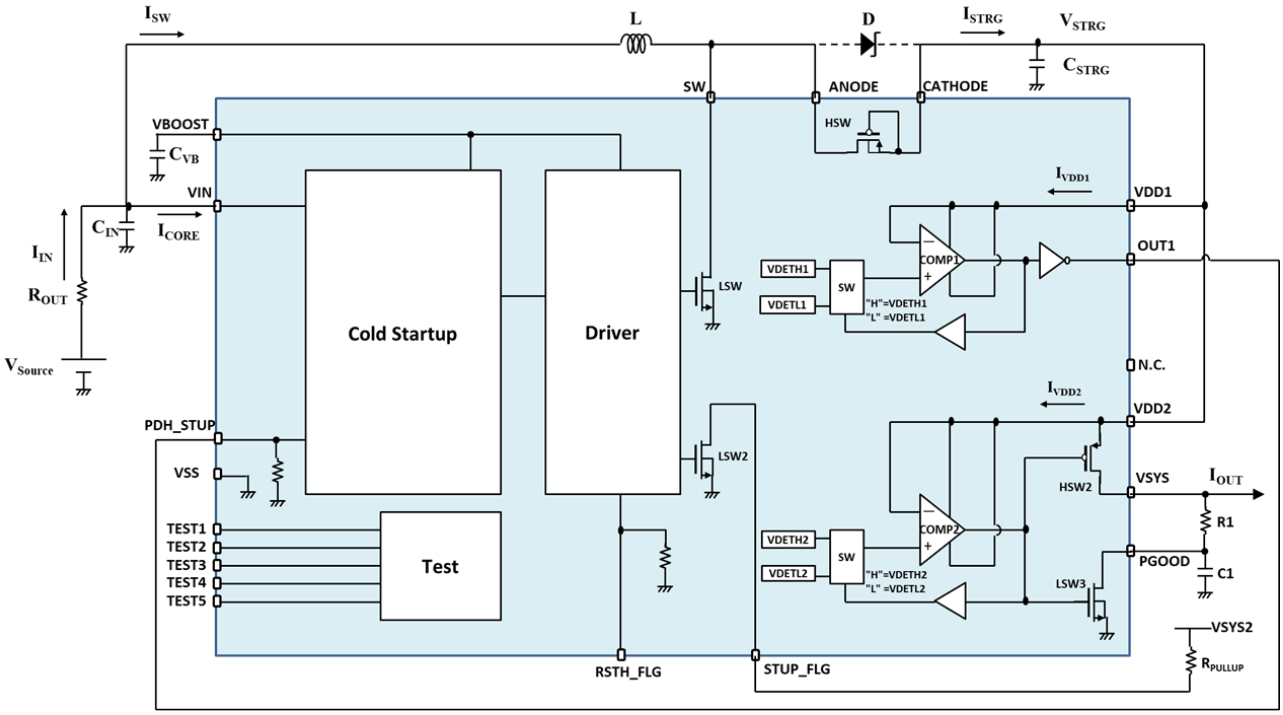


Figure 11.3.1 Typical circuit design

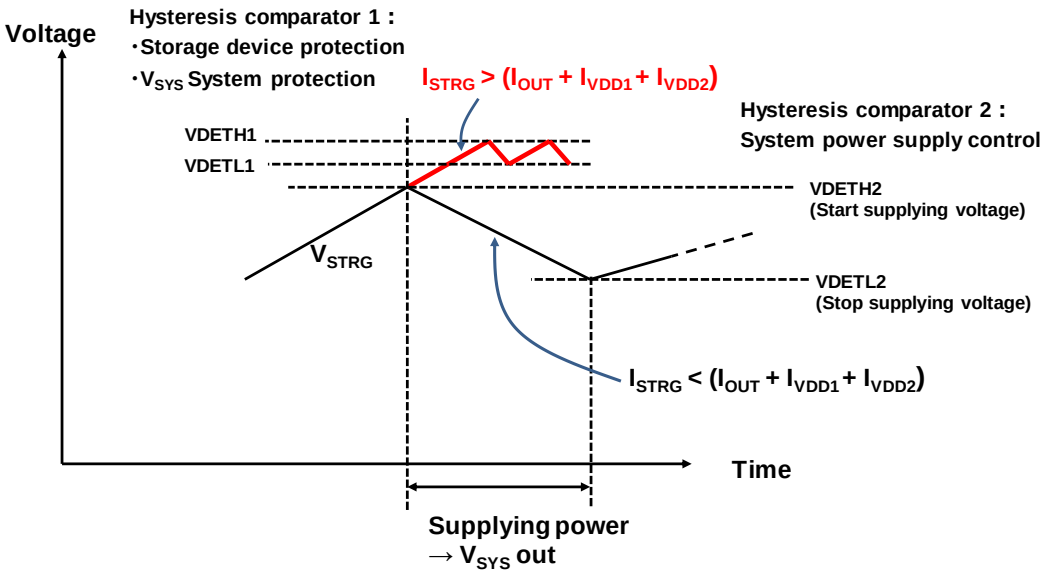


Figure 11.3.2 DC/DC converting function

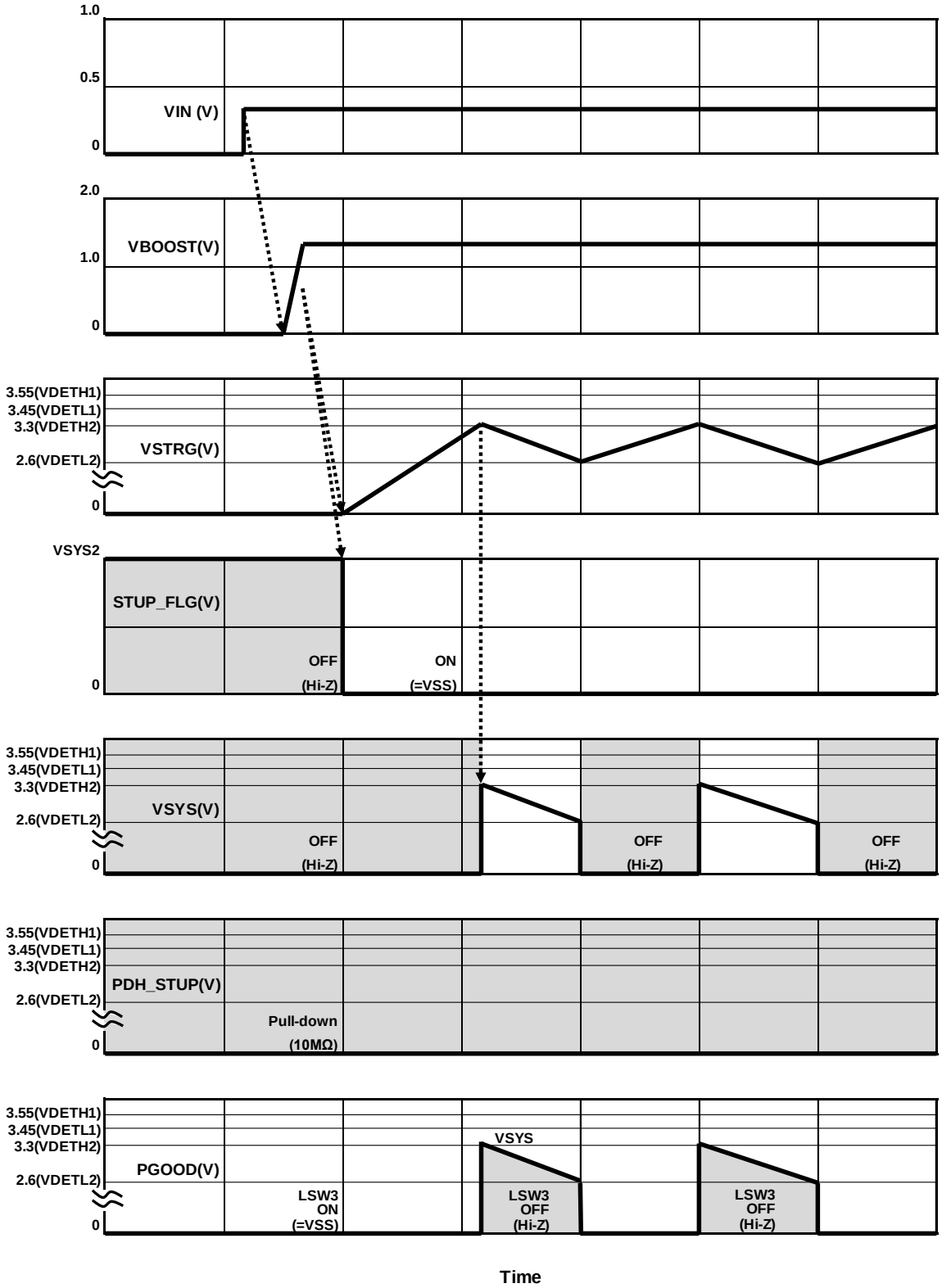


Figure 11.3.3 DC/DC converting sequence 1 (I_{STRG} < (I_{OUT} + I_{VDD1} + I_{VDD2}))

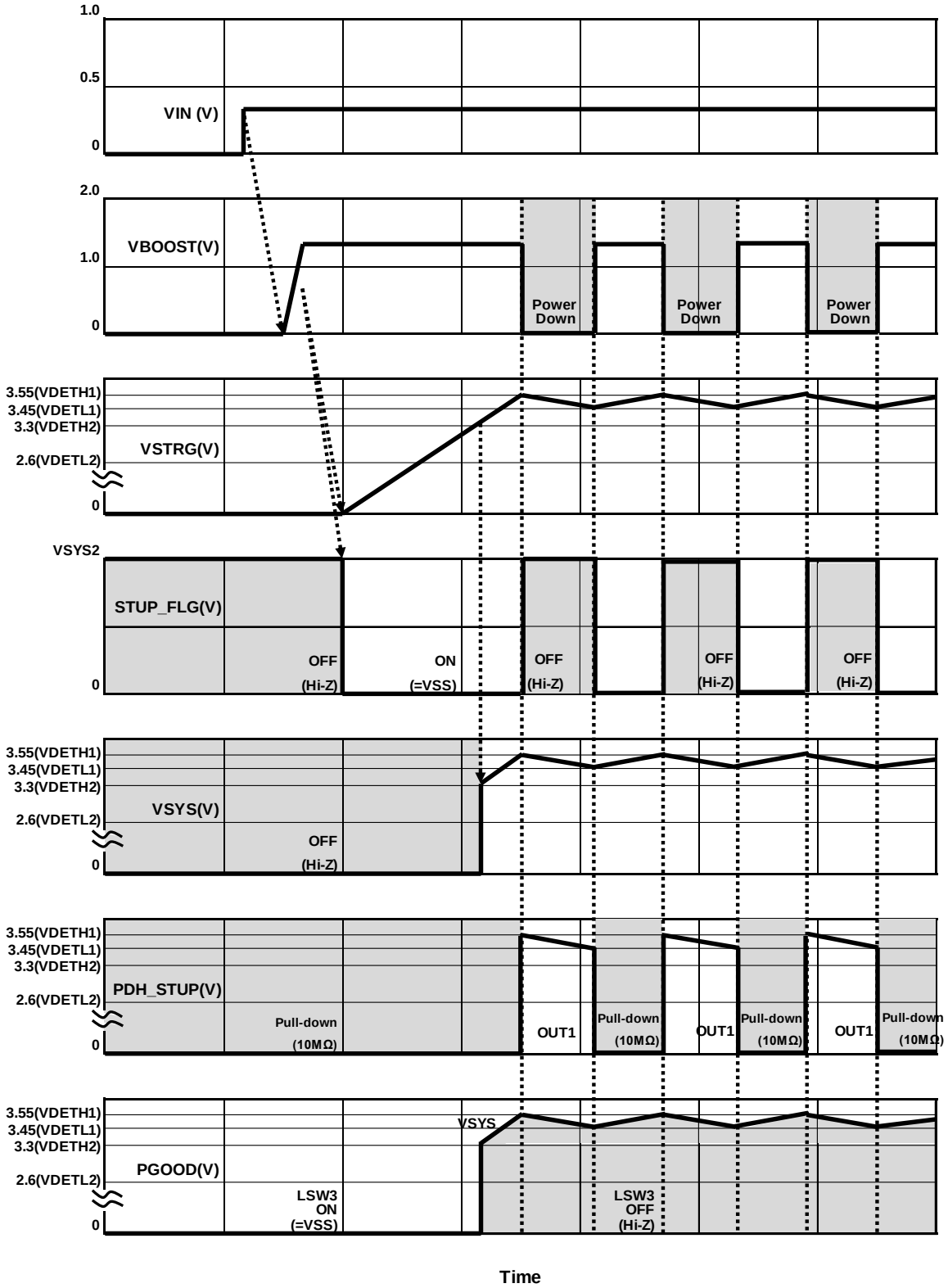


Figure 11.3 4 DC/DC converting sequence 2 (I_{STRG} > (I_{OUT} + I_{VDD1} + I_{VDD2}))

11.3.1 Cold Startup

The AP4470 starts DC/DC converting when more than 0.20V(typical) is applied to VIN pin (VIN ≧ $V_{IN,STUP}$). The input voltage to VIN pin is upconverted to VBOOST pin. The LSW is switched by the VBOOST voltage powered driver circuit and stored energy to an external inductor is charged to C_{STRG} by this switching operation.

For rectifier circuit for this startup, adding an external diode (D) or using the on-chip diode (HSW) should be used, either will work.

11.3.2 DC/DC

11.3.2.1 When ($I_{STRG} > (I_{OUT} + I_{VDD1} + I_{VDD2})$)

When C_{STRG} has no initial charge, V_{STRG} voltage is increasing by DC/DC converting operation while energy is stored to $C_{STRG.}$
When V_{STRG} voltage reaches to V_{DETH2}, the COMP2 turns on the High Side Switch (HSW2) and then, V_{STRG} is supplied to V_{SYS}.

In case in which the OUT1 pin is connected to PDH_STUP pin, the startup will be powered down and DC/DC converting will be stopped when V_{STRG} voltage reaches to V_{DETH1}. In this case, a system that is connected to V_{SYS} will be operated from V_{DETH2} to V_{DETH1}
To connect OUT1 pin and PDH_STUP pin avoids stopping accidentally startup operation because PDH_STUP state is defined to “Low” by the on-chip pull down resistor even if the COMP1 output is unknown (VDD1<1.2V).

When DC/DC operation is stopped, V_{STRG} voltage will be decreased because of leakage current of a storage device, etc.
In case in which the OUT1 pin is connected to PDH_STUP pin, the startup is returned from power down and the AP4470 starts DC/DC operation again when the COMP1 detects V_{STRG} voltage goes down to V_{DETL1}.

11.3.2.2 When ($I_{STRG} < (I_{OUT} + I_{VDD1} + I_{VDD2})$)

If V_{SYS} is supplied under the flowing condition, V_{STRG} voltage will be decreased even though the AP4470 is on DC/DC converting operation.

Current supply from V_{SYS} pin (I_{OUT}) + COMP1 consumption (I_{VDD1}) + COMP2 consumption (I_{VDD2}) are larger than I_{STRG} which is charge current to C_{STRG} via a diode

AND

$V_{STRG} \geqq V_{DETH2}$

When the COMP2 detects V_{STRG} voltage goes down to V_{DETL2}, power supply from V_{SYS} is stopped continuing DC/DC operation. Power supply from V_{SYS} to a system starts again when V_{STRG} voltage become larger than V_{DETH2} ($V_{STRG} \geqq V_{DETH2}$).

11.4. Power Good

System Reset Application Circuit

The output of Power Good (PGOOD) becomes “Low” to “Hi-Z” when the AP4470 starts supplying power from V_{SYS} pin. Connecting a resistor R1 and a capacitor C1, the Power Good function can be used to release system reset using delay that is defined by R1 and C1 time constant.

Figure 11.4.1 shows an example system reset circuit.

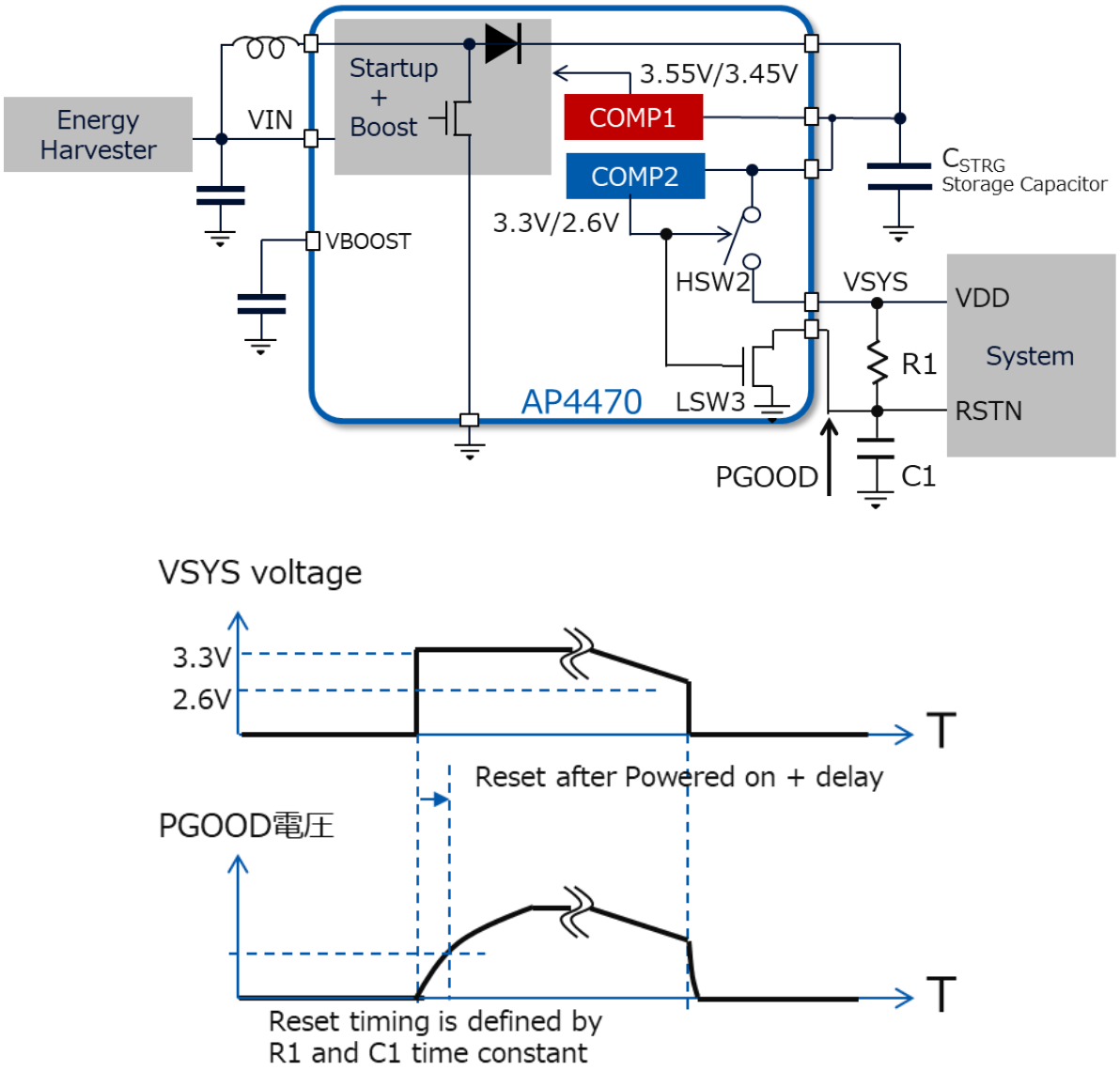


Figure 11.4.1 Power Good function application example

11.5. Startup FLG

Zero Standby Current Trigger Switch Application Circuit.
The STUP_FLG output DC/DC converting status of the AP4470. This can be used trigger switch function with zero standby current if a system has proprietary power supply (VSYS2). Figure 11.5.1 shows a typical circuit for zero standby trigger switch. Using only this switch function doesn't require an external inductor and a storage device.

The AP4470's startup does upconverting VIN input voltage to VBOOST pin. When on-chip driver circuit is powered on by VBOOST voltage, an open drain output goes from "Hi-Z" to "Low".
The example Figure 11.5.1, shows STUP_FLG pin transition from "High (VSYS2)" to "Low (VSS)".
This function can be used to recover from sleep mode using this signal as a trigger. STUP_FLG signal is cleared by RSTH_FLG pin "High" input.

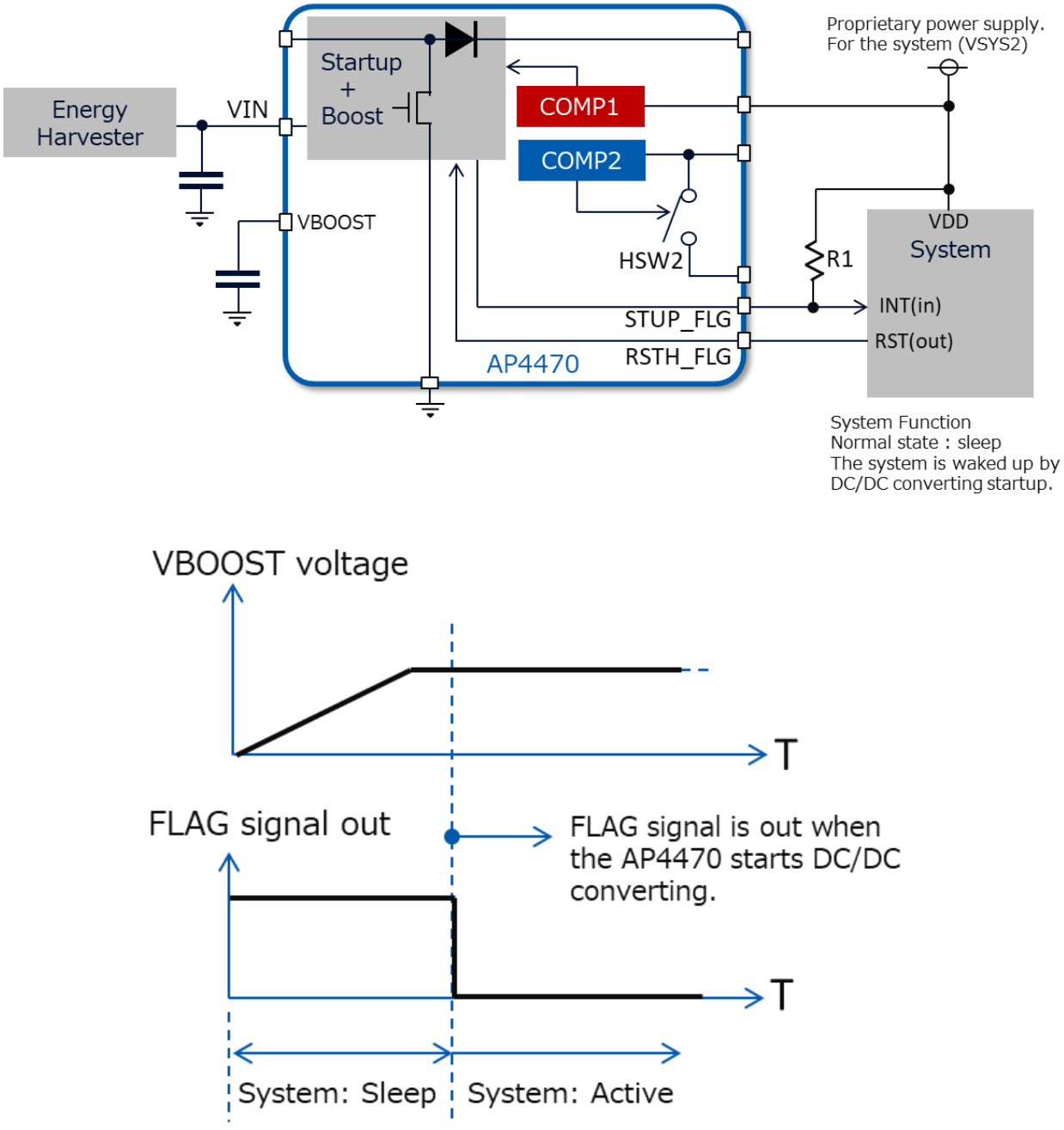


Figure 11.5.1 Zero Standby Current Trigger Switch

12. Test Circuits

12.1. External Circuit Example

Figure 12.1.1 is for reference data measurement. The bill of materials is shown in Table 12.2.1.

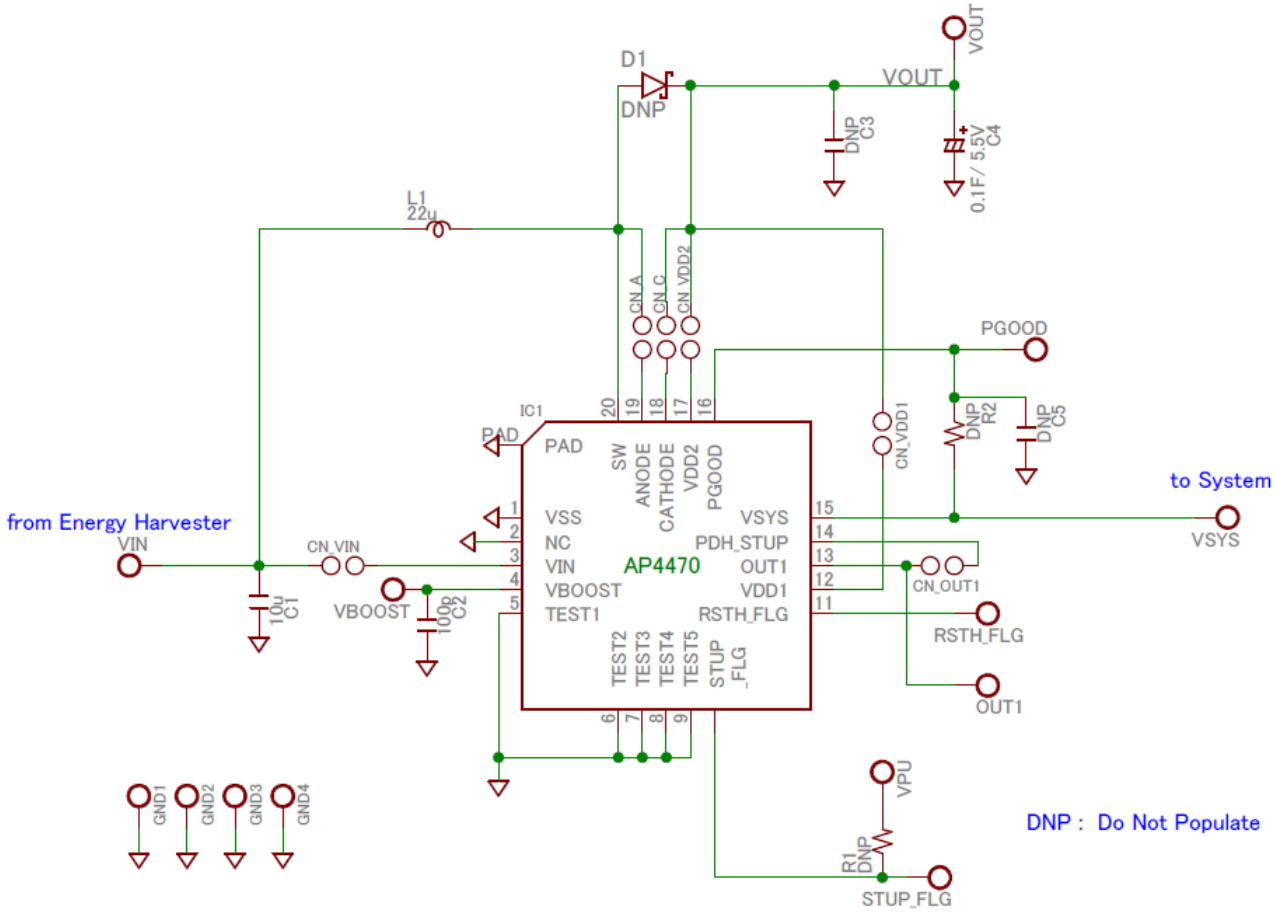


Figure 12.1.1 External circuits for test

Notes:

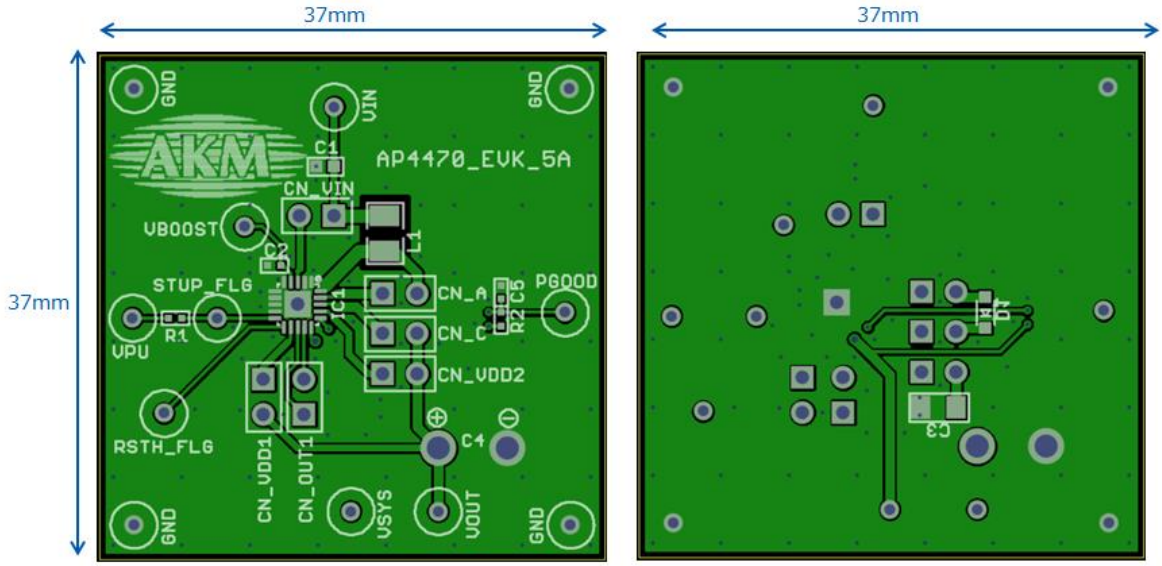
*17. It is recommended to connect the exposed pad (EPAD), that is located on the bottom of the package, to VSS. The pad can be left floating if needed.

*18. If on-chip diode for rectifier circuit is not used, ANODE pin and CATHODE pin both should be tied to VSS or leave them open.

*19. C_{STRG} capacitance value should be optimized based on system load.

*20. The inductor L1 affects DC/DC converting efficiency. The inductor value is chosen based on system load and ranges from 2.2µH to 22µH for most applications. The DC resistance of the L1 inductor directly affects DC/DC converting efficiency. Larger inductor can improve efficiency in particularly low VIN input applications. Please consider the characteristics of inductor for system optimization.

12.2. PCB Guidline



TOP view BOTTOM view

Figure 12.1.1 PCB layout (2layers)

Table 12.2.1 Bill of Materials List

Name	Value	Parts	Description
L1	22μH	LBR2518T220K	Inductor for Step-up DC/DC
R1	DNP		Pull-up resistor for STUP_FLG
R2	DNP		Pull-up resistor for PGOOD
C1	10μH		Capacitor for the VIN source Suppress the fluctuation of the VIN
C2	100pF		Capacitor for VBOOST
C3	DNP		Capacitor for C_{STRG}
C4	0.1F/ 5.5V	FG0H104ZF	Capacitor for C_{STRG}
C5	DNP		Capacitor for PGOOD
D1	DNP		Diode for External rectifier
IC1		AP4470	

*DNP : Do Not Populate (Even if it is not implemented, there is no problem with basic operation)

Notes:

*21. On-chip diode (HSW) for rectifier is used in this circuit. If an external diode for rectifier circuit is used, ANODE pin and CATHODE pin both should leave open and mount a component on D1.

*22. Using low leakage current capacitor is strongly recommended for C3 and C4.

*23. For reference data measurement, NC pin (#2) =VSS.

13. Typical Characteristics

Unless otherwise noted, specifications apply for conditions of

- Test Circuit : PCB/BOM specified on Chapter 12.
- On-chip diode (HSW) is used.
- Ta=25ºC

13.1. Cold Startup

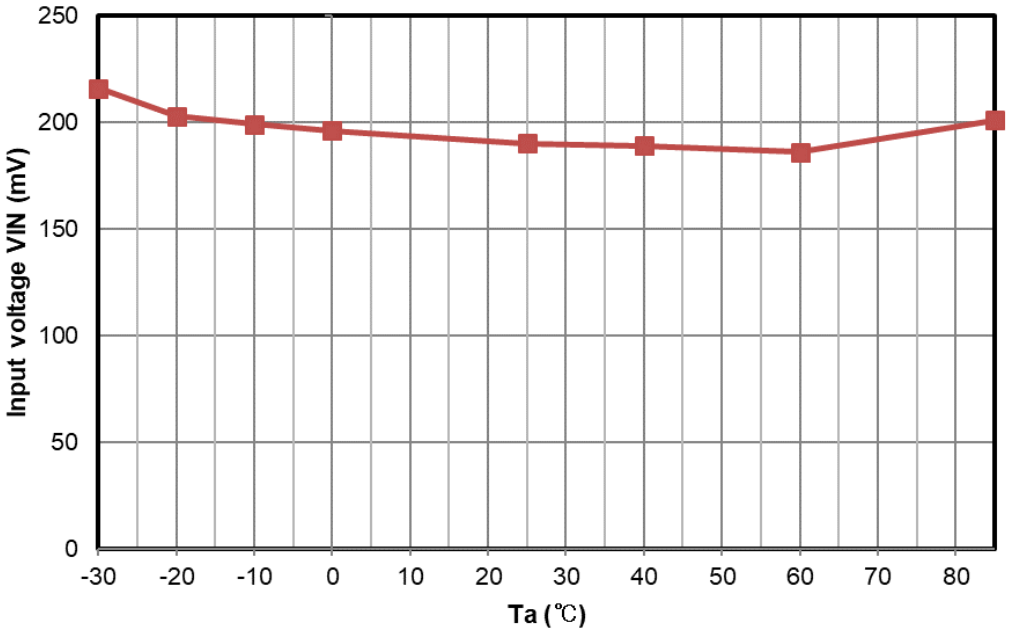


Figure 13.1.1 Minimum input startup voltage vs Temperature

13.2. Switching Frequency

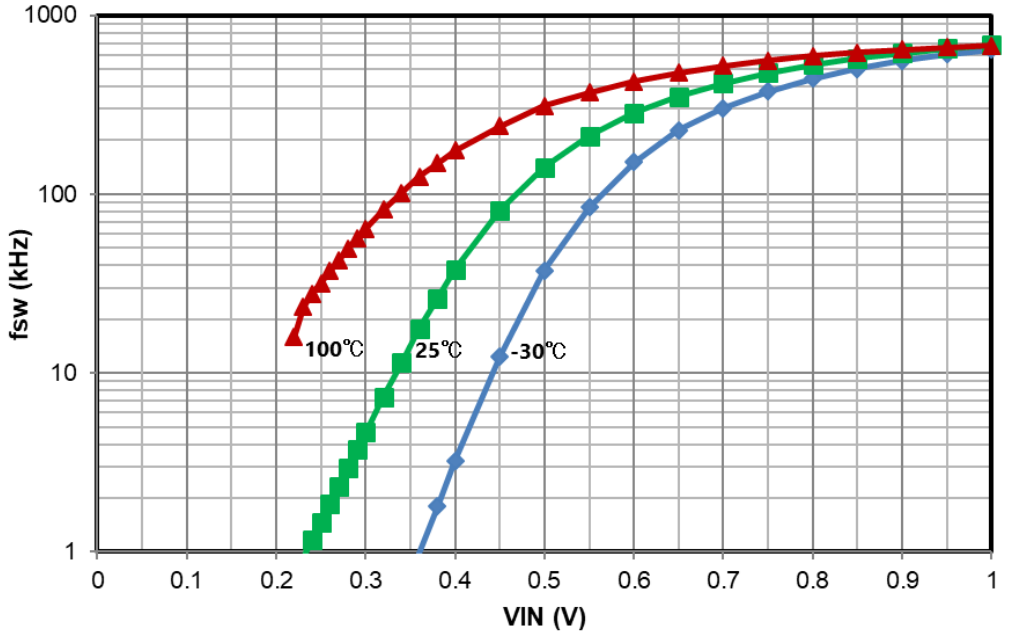


Figure 13.2.1 Switching Frequency vs VIN

13.3. Low side ON pulse width

Low Side Switching Time is constant regardless of VIN and temperature.

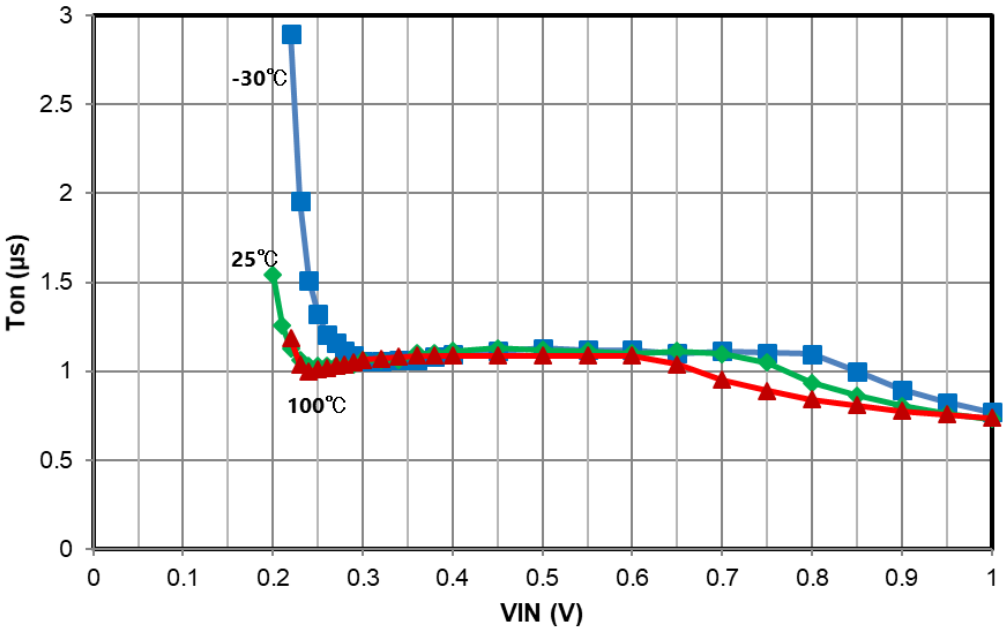


Figure 13.3.1 Low side ON pulse width vs VIN

13.4. COMP1

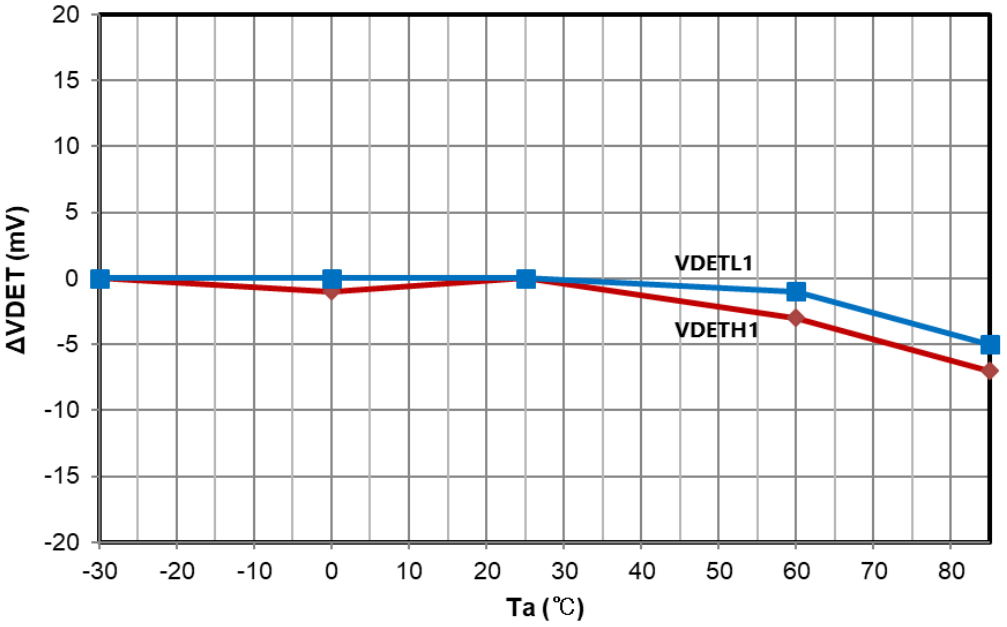


Figure 13.4.1 temperature characteristics of V_{DETH1} and V_{DETL1} normalized at 25ºC

13.5. COMP2

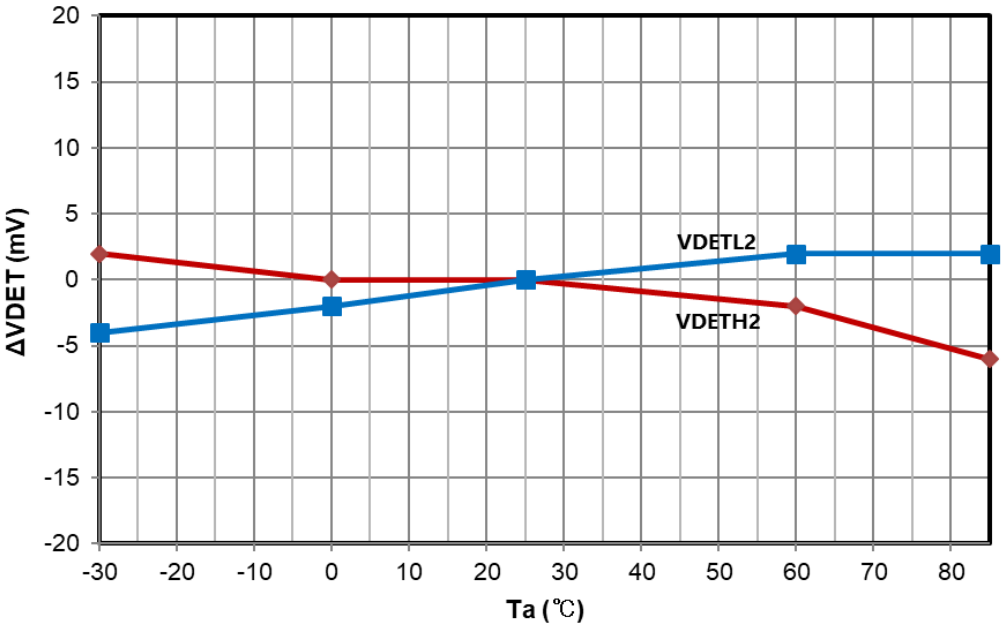


Figure 13.5.1 temperature characteristics of V_{DETH2} and V_{DETL2} normalized at 25ºC

13.6. Current consumption

I_{SW} and I_{STRG} are data at V_{STRG}=1.0V

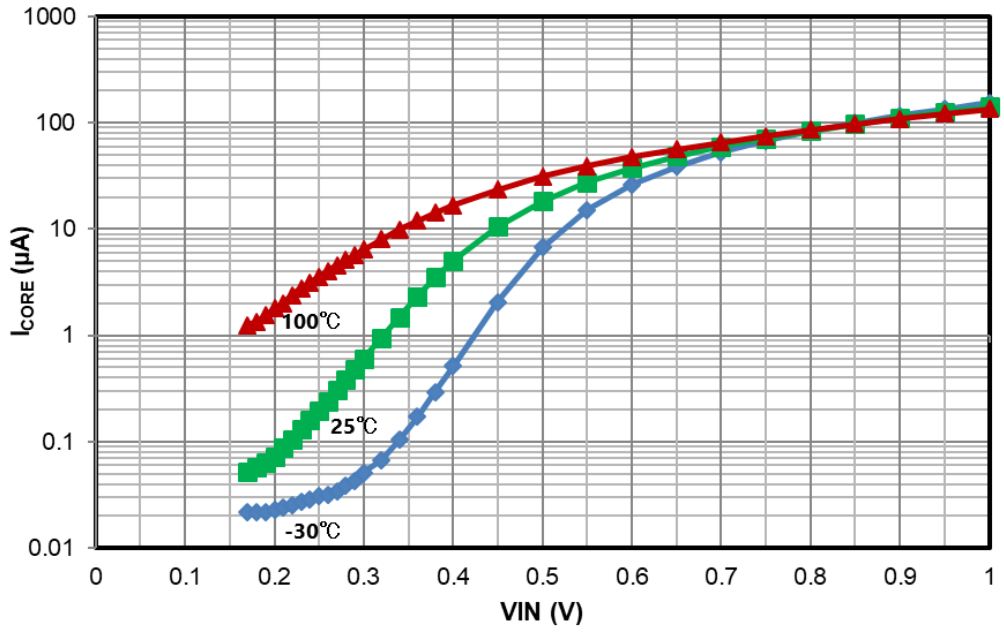


Figure 13.6.1 I_{CORE} vs VIN

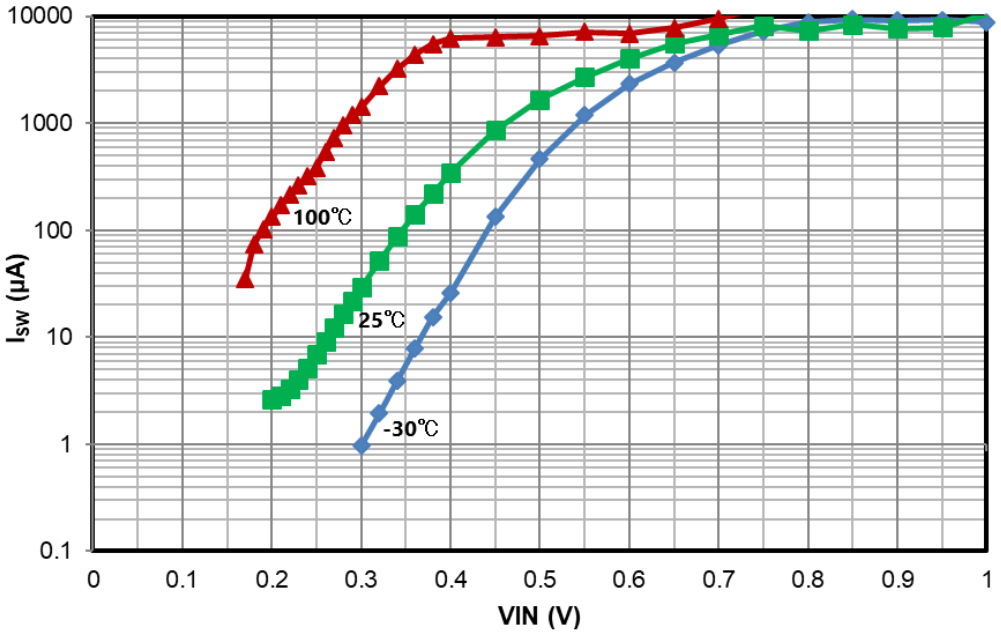


Figure 13.6.2 I_{SW} vs VIN

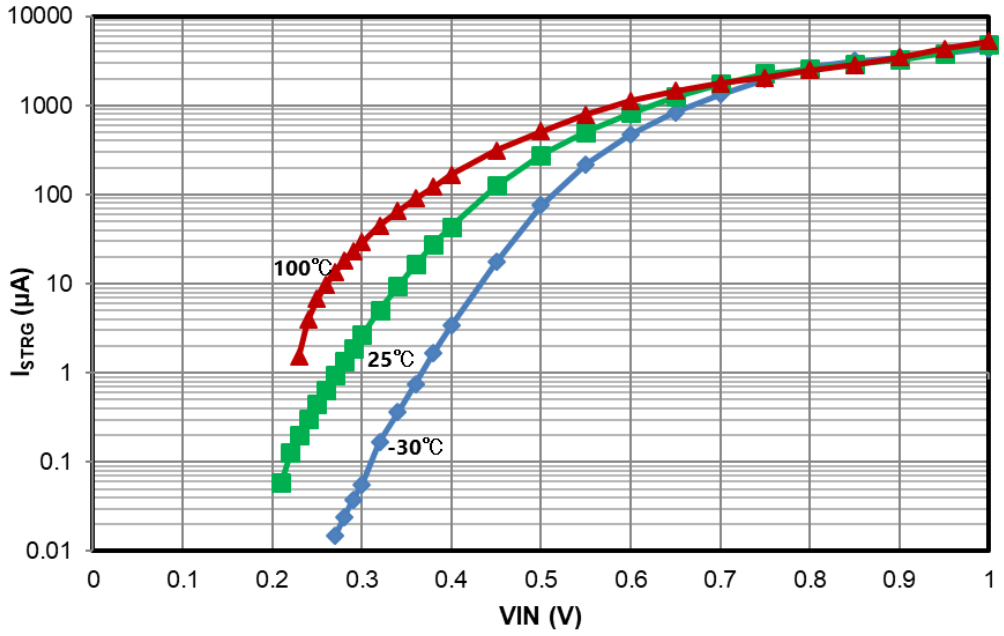


Figure 13.6.3 I_{STRG} vs VIN

13.7. Load curve

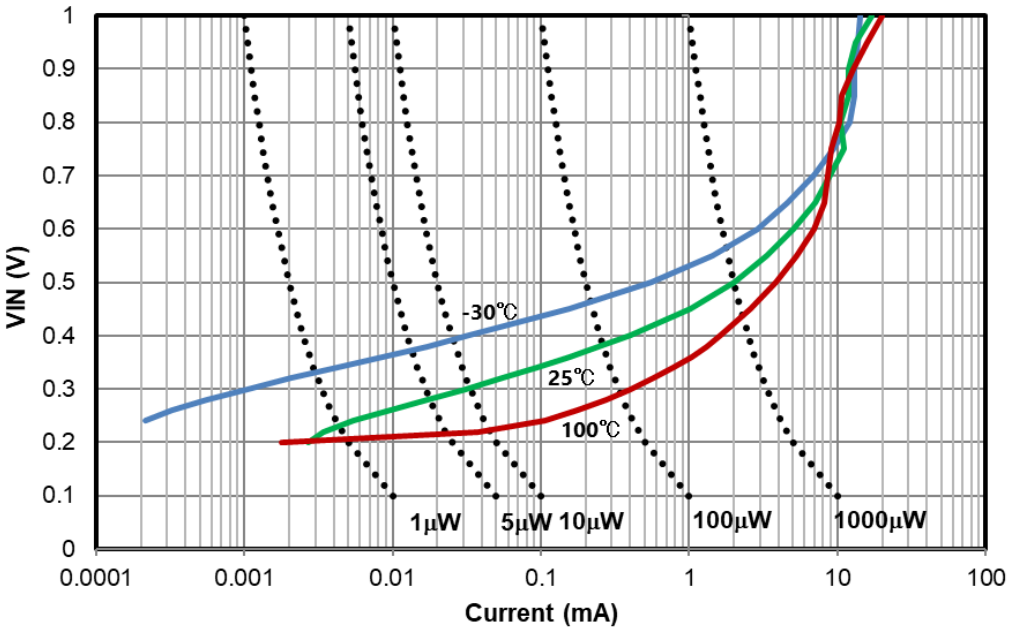


Figure13.7.1 Load curve of Cold Startup

14. Recommended External Circuit

14.1. External Circuit Example

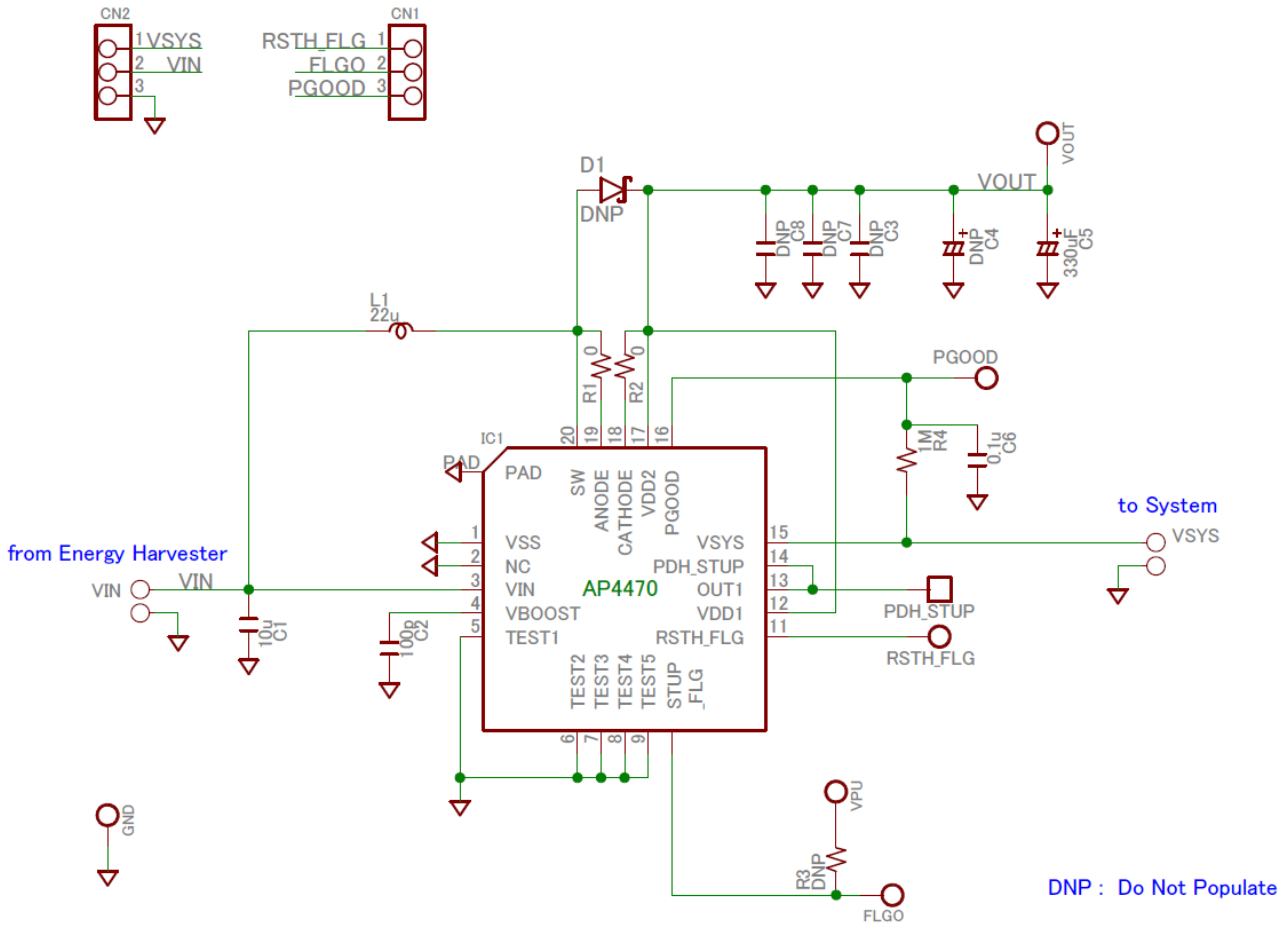


Figure14.1.1 Recommended external circuits

Notes:

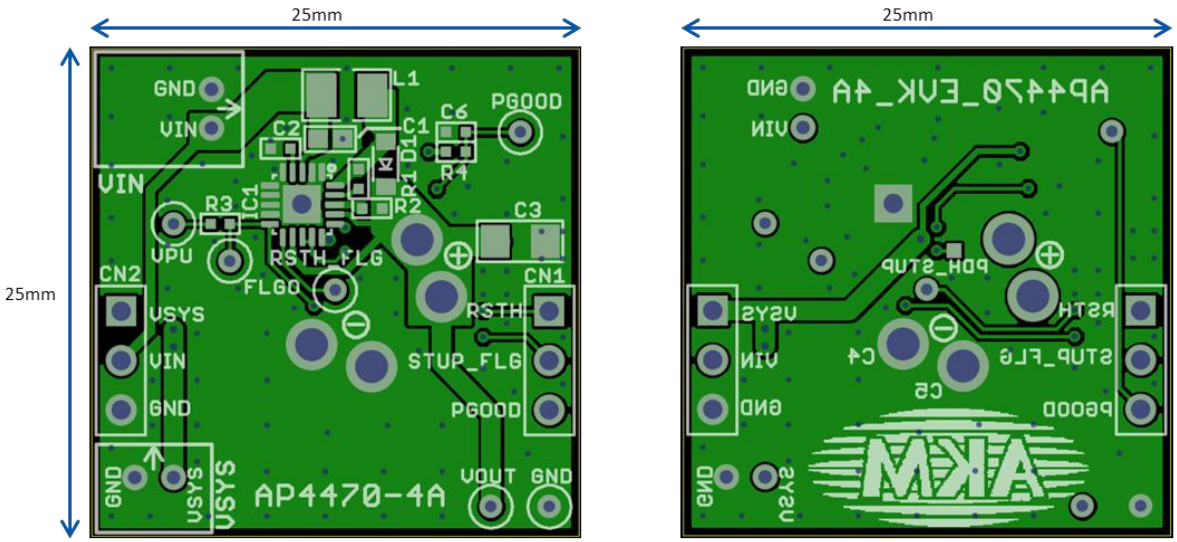
*24. It is recommended to connect the exposed pad (EPAD), that is located on the bottom of the package, to VSS. The pad can be left floating if needed.

*25. If on-chip diode for rectifier circuit is not used, ANODE pin and CATHODE pin both should be tied to VSS or leave them open.

*26. C_{STRG} capacitance value should be optimized based on system load.

*27. The inductor L1 affects DC/DC converting efficiency. The inductor value is chosen based on system load and ranges from 2.2μH to 22μH for most applications. The DC resistance of the L1 inductor directly affects DC/DC converting efficiency. Larger inductor can improve efficiency in particularly low VIN input applications. Please consider the characteristics of inductor for system optimization.

14.2. Reference PCB



TOP view BOTTOM view

Figure14.1.1 PCB layout (2layers)

Table 14.2.1 Bill of Materials List

Name	Value	Parts	Description
L1	22μH	LBR2518T220K	Inductor for DC/DC
R1	0 Ω		Select the on-chip diode (ANODE pin)
R2	0 Ω		Select the on-chip diode (CATHODE pin)
R3	DNP		Pull-up resistor for STUP_FLG
R4	1MΩ		Pull-up resistor for PGOOD
C1	10μH	Multi-Layer Ceramic Capacitor (MLCC)	Capacitor for the VIN source Suppress the fluctuation of the VIN
C2	100pF	MLCC	Capacitor for VBOOST
C3	DNP	MLCC	Capacitor for C_{STRG}
C4	DNP		Capacitor for C_{STRG}
C5	330μF	Electrolytic capacitor	Capacitor for C_{STRG}
C6	0.1μF	MLCC	Capacitor for PGOOD
C7	DNP	MLCC	Capacitor for C_{STRG}
C8	DNP	MLCC	Capacitor for C_{STRG}
D1	DNP	(RB751V40T1G)	Diode for External rectifier
IC1		AP4470	

*DNP : Do Not Populate (Even if it is not implemented, there is no problem with basic operation)

Notes:

*28. R1 and R2 are not required in the actual application because those resistances are to switch using the on-chip diode or the external diode in the schematic in this section.
If an on-chip diode (HSW) for rectifier circuit is used, please mount R1=R2=0Ω without D1.

*29. Using low leakage current capacitor is strongly recommended for C3, C4, C5, C7 and C8.

15. Packages

15.1. Outline Dimensions

20-pin HWQFN (3.0mm×3.0mm×0.75mm 0.5mm pitch) (Unit: mm)

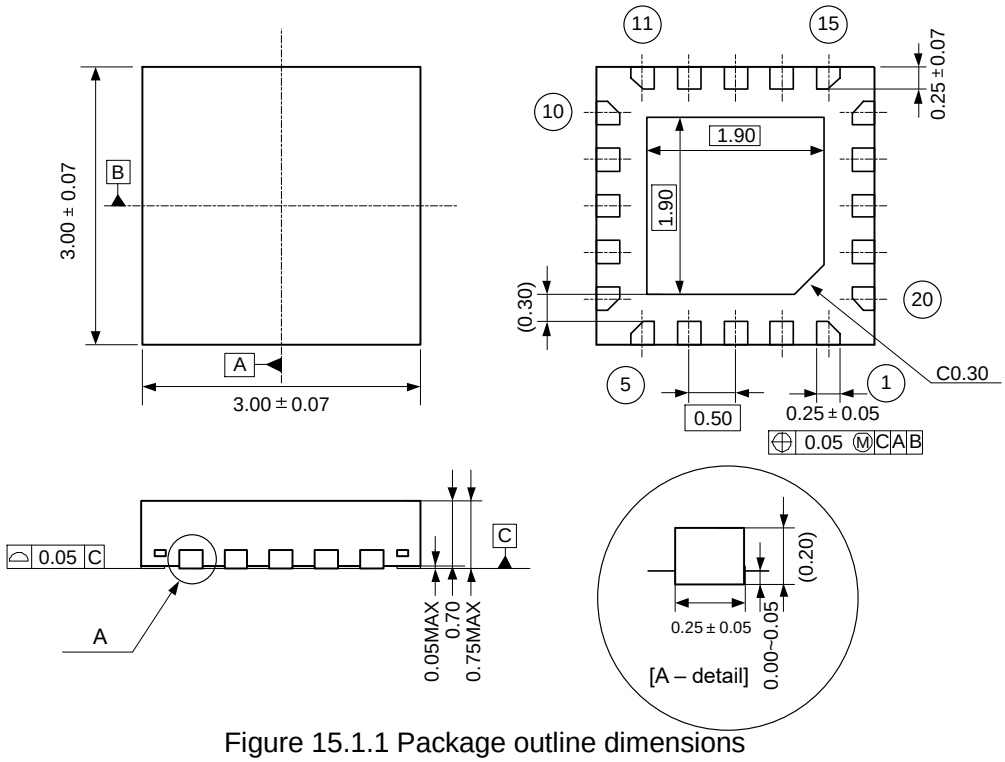
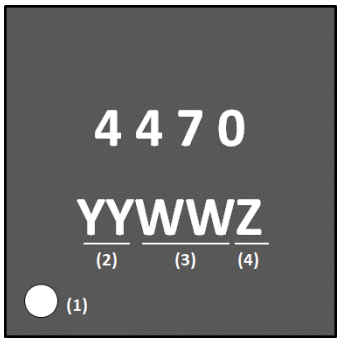


Figure 15.1.1 Package outline dimensions

15.2. Marking

Style	:	HWQFN
Number of pins	:	20 pins
Product number	:	4470
Date code	:	YYWWZ(5digits)
1 Pin Indication	:	Circle (●)
YY	:	Year code(2020->20)
WW	:	Week code
Z	:	Management code



(1) 1 Pin Indication
(2) Year code (last 2 digits)
(3) Week code
(4) Management code

16. Ordering Guide

- AP4470 20-pin HWQFN (3.0mm×3.0mm×0.75mm 0.5mm pitch)
- APD4470 AP4470 Evaluation Board

17. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
20/3/17	00	First Edition		

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