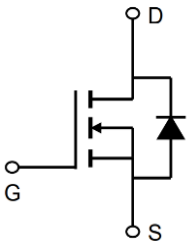
AP40N10D

100V N-Channel Enhancement Mode MOSFET

Description

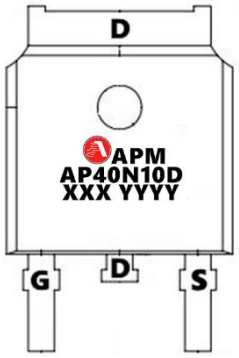
The AP40N10D uses advanced **APM-SGTII** technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



General Features

V_{DS} = 100V I_D =40A

$R_{DS(ON)}$ < 25mΩ @ V_{GS}=10V **(Type：18mΩ)**

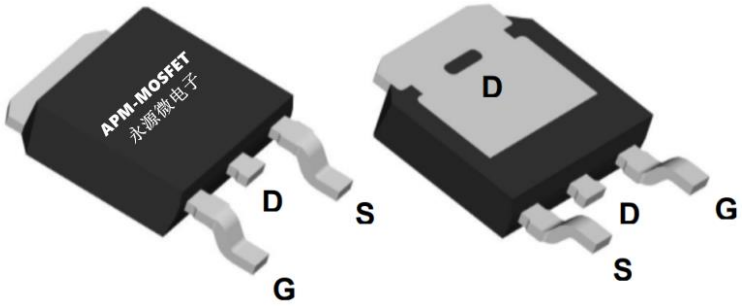


Application

DC/DC Converter

LED Backlighting

Power Management Switches



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP40N10D	TO-252-3L	AP40N10D XXX YYYY	2500

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	100	V
VGS	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ 10V	40	A
I_D@T_C=100℃	Continuous Drain Current, V_{GS} @ 10V	18	A
IDM	Pulsed Drain Current	100	A
EAS	Single Pulse Avalanche Energy	160	mJ
IAS	Avalanche Current	53.4	A
P_D@T_C=25℃	Total Power Dissipation[4]	27	W
TSTG	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃
$R_{\theta}JA$	Thermal Resistance Junction-Ambient	4.65	℃/W
$R_{\theta}JC$	Thermal Resistance Junction-Case	62	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
BVDSS	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	100	108	-	V
IDSS	Drain-Source Leakage Current	V_{DS} = 80V, V_{GS} = 0V	-	-	1	μA
IGSS	Gate to Body Leakage Current	V_{DS} = 0V, V_{GS} = ±20V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	1.2	1.8	2.6	V
RDS(on)	Static Drain-Source On-Resistance	V_{GS} = 10V, I_D = 15A	-	18	25	mΩ
		V_{GS} = 4.5V, I_D = 10A	-	28	38	mΩ
g_{fs}	Forward Threshold Voltage	V_{DS}= 10V, I_D= 20A	-	22	-	S
R_g	Gate Resistance	V_{DS} = V_{GS}=0V, f = 1.0MHz	-	1.62	-	Ω
Ciss	Input Capacitance	V_{DS} = 50V, V_{GS} = 0V, f = 1.0MHz	-	822	-	pF
Coss	Output Capacitance		-	310	-	pF
Crss	Reverse Transfer Capacitance		-	23.5	-	pF
Q_g	Total Gate Charge	V_{DS}= 50V, I_D = 20A, V_{GS} = 10V	-	22.7	-	nC
Q_{gs}	Gate-Source Charge		-	6.2	-	
Q_{gd}	Gate-Drain("Miller") Charge		-	5.3	-	
td(on)	Turn-On Delay Time	V_{DS} = 50V, I_D = 20A, R_G = 3Ω, V_{GS}=10V	-	15	-	ns
t_r	Turn-On Rise Time		-	3.2	-	
td(off)	Turn-Off Delay Time		-	30	-	
t_f	Turn-Off Fall Time		-	7.6	-	
I_S	Continuous Source Current		-	-	25	A
VSD	Diode Forward Voltage	I_S=20A . V_{GS} = 0V	-	0.88	1.0	V
t_{rr}	Reverse Recovery Time	I_{SD}=20A, dI_{SD}/dt=100A/μs	-	45	-	ns
Q_{rr}	Reverse Recovery Charge		-	59	-	nC

Notes:

1、The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%

3、The EAS data shows Max. rating . The test condition is V_{DD}=50V, V_{GS}=10V, L=0.5mH, I_{AS}=8A

4、The power dissipation is limited by 150°C junction temperature

5、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

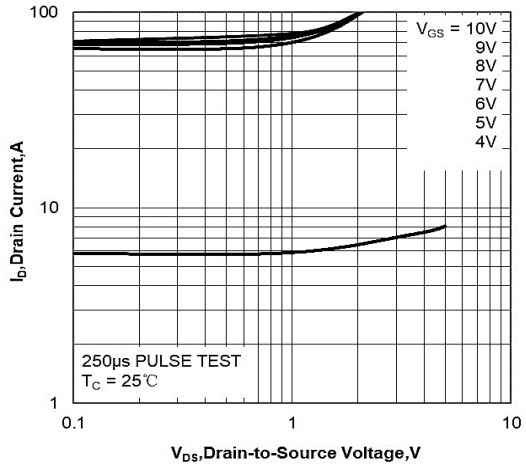


Figure 1. Output Characteristics

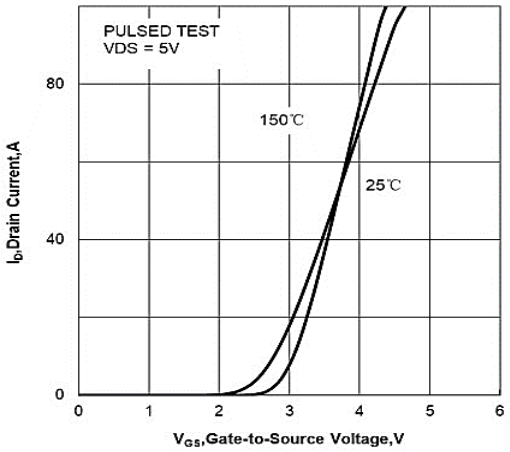


Figure 2. Transfer Characteristics

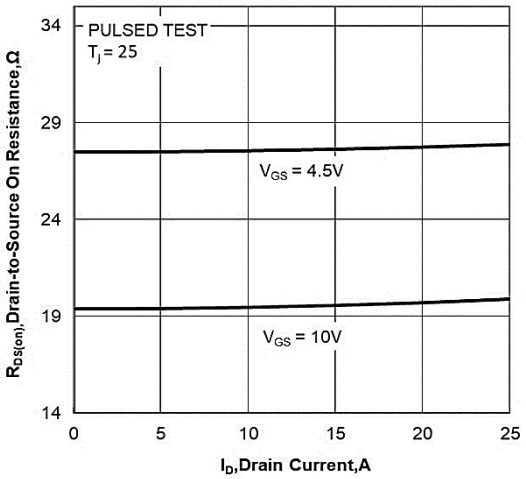


Figure 3. Drain-to-Source On Resistance vs Drain Current

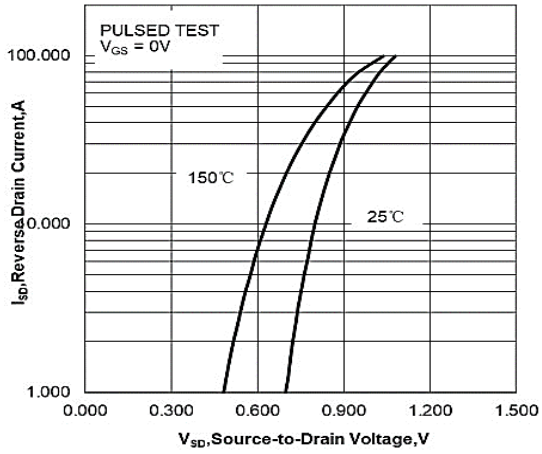


Figure 4. Body Diode Forward Voltage vs Source Current and Temperature

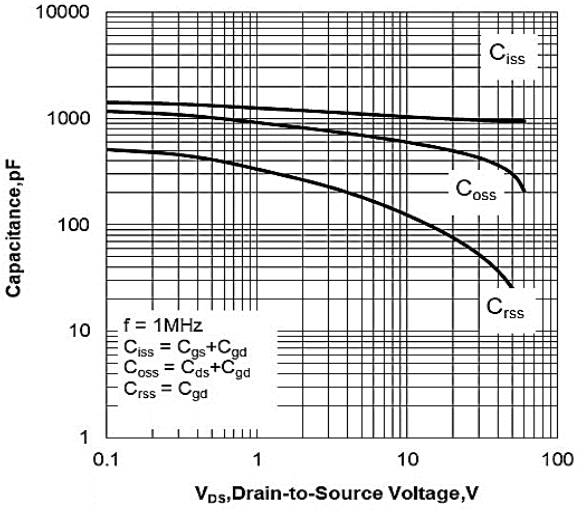


Figure 5. Capacitance Characteristics

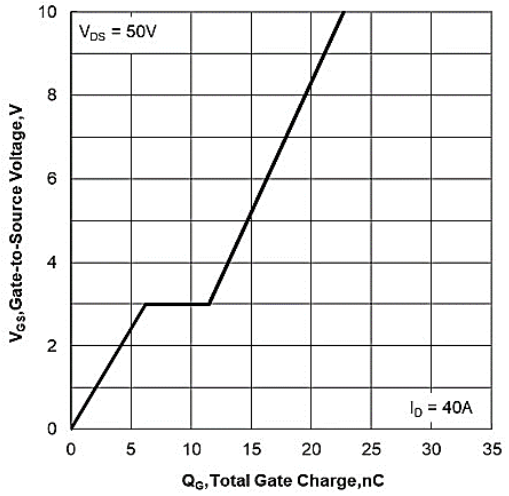


Figure 6. Gate Charge Characteristics

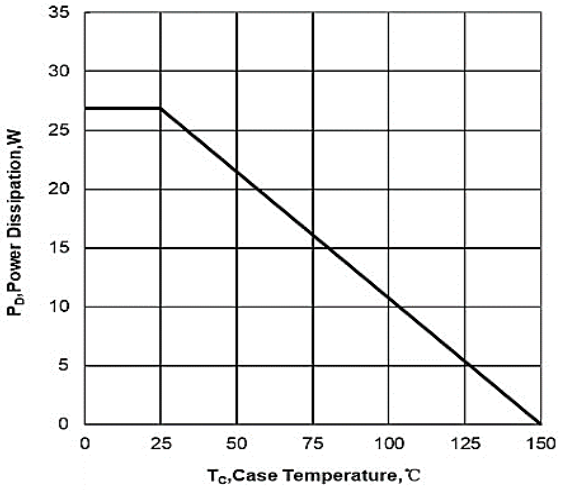


Figure 9. Maximum Continuous Drain Current vs Case Temperature

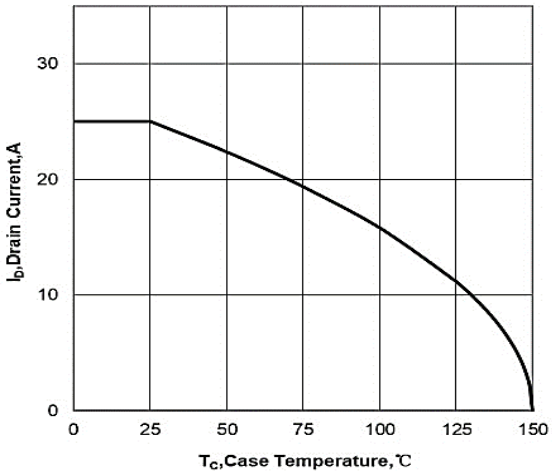


Figure 10. Maximum Power Dissipation vs Case Temperature

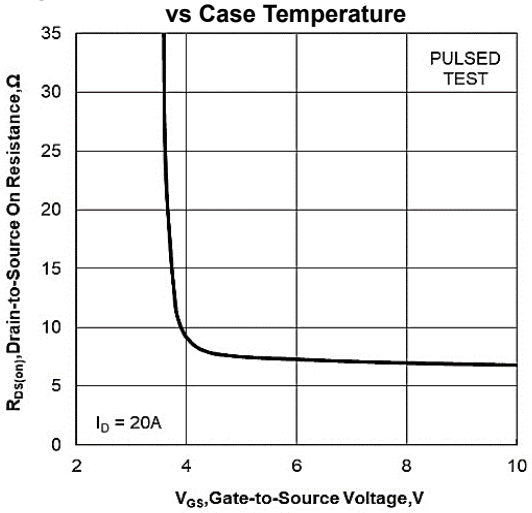


Figure11. Drain-to-Source On Resistance vs Gate Voltage and Drain Current

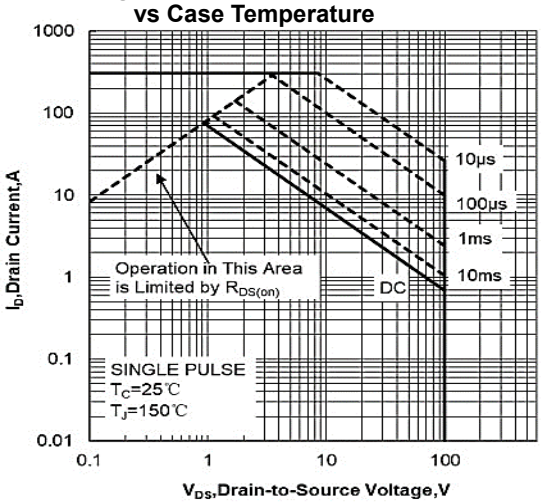


Figure 12. Maximum Safe Operating Area

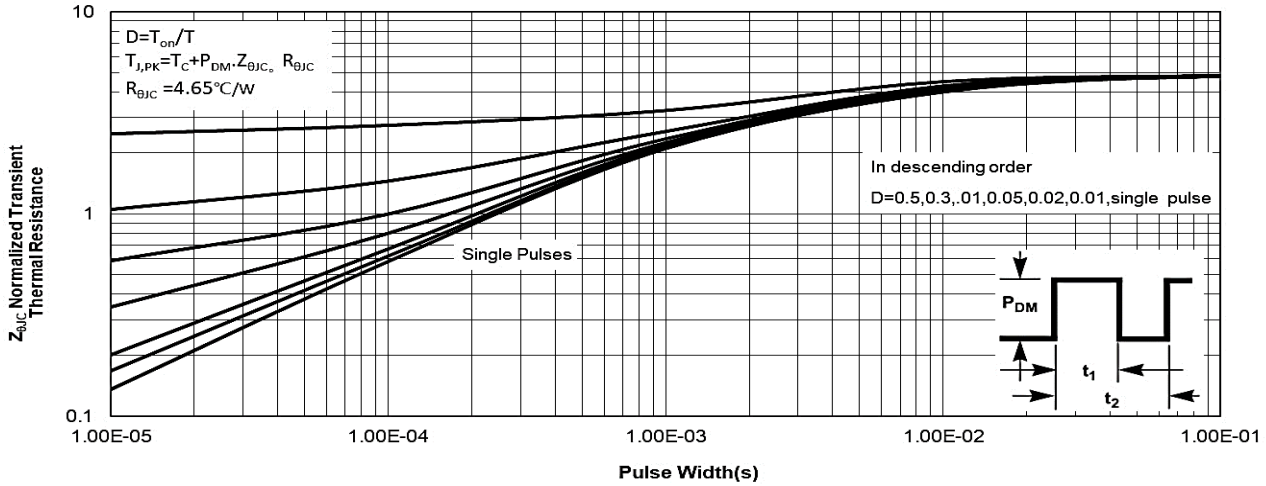
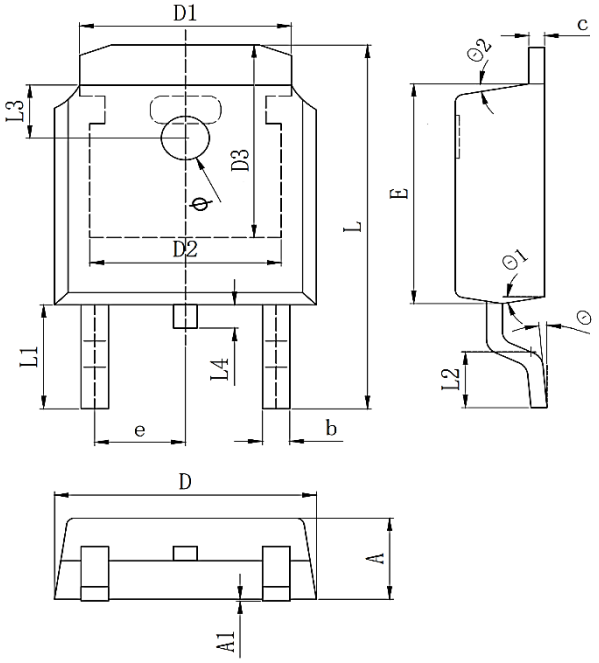


Figure 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Package Mechanical Data-TO-252-3L



Symbol	Dim in mm		
	Min	Typ	Max
A	2.1	2.3	2.5
A1	0	0.064	0.128
b	0.64	0.75	0.86
c	0.45	0.52	0.6
D	6.4	6.6	6.8
D1	5.33REF		
D2	4.83REF		
D3	5.25REF		
E	5.9	6.1	6.3
e	2.286TYP		
L	9.8	10.1	10.4
L1	2.888REF		
L2	1.4	1.5	1.7
L3	1.65REF		
L4	0.6	0.8	1
ϕ	1.1	1.2	1.3
θ	0°		10°
θ1	5°		10°
θ2	5°		10°

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Edition	Date	Change
REV1.0	2023/05/01	Initial release