



**Advanced Power
Electronics Corp.**

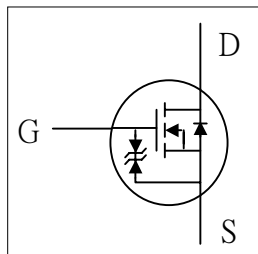
AP4024GEMT-HF

Halogen-Free Product

N-CHANNEL ENHANCEMENT MODE

POWER MOSFET

- ▼ Simple Drive Requirement
- ▼ SO-8 Compatible with Heatsink
- ▼ Low On-resistance
- ▼ RoHS Compliant & Halogen-Free

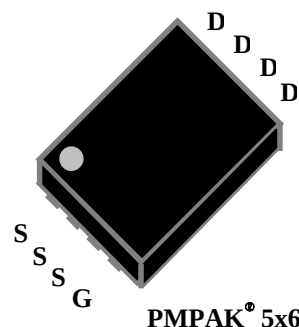


BV_{DSS}	30V
$R_{DS(ON)}$	4.5m Ω
I_D^4	60A

Description

AP4024 series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The PMPAK[®] 5x6 package is special for DC-DC converters application and the foot print is compatible with SO-8 with backside heat sink and lower profile.



Absolute Maximum Ratings@T_J=25°C(unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^\circ C$	Drain Current (Chip), $V_{GS} @ 10V^4$	60	A
$I_D@T_A=25^\circ C$	Drain Current, $V_{GS} @ 10V^3$	26.1	A
$I_D@T_A=70^\circ C$	Drain Current, $V_{GS} @ 10V^3$	20.9	A
I_{DM}	Pulsed Drain Current ¹	160	A
$P_D@T_C=25^\circ C$	Total Power Dissipation	36.7	W
$P_D@T_A=25^\circ C$	Total Power Dissipation ³	5	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-c	Maximum Thermal Resistance, Junction-case	3.4	$^\circ C/W$
Rthj-a	Maximum Thermal Resistance, Junction-ambient ³	25	$^\circ C/W$



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Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	30	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =20A	-	3.5	4.5	mΩ
		V _{GS} =4.5V, I _D =20A	-	5	8.5	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1.2	1.6	2.5	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =20A	-	70	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =24V, V _{GS} =0V	-	-	10	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V, V _{DS} =0V	-	-	±30	uA
Q _g	Total Gate Charge	I _D =20A	-	15	24	nC
Q _{gs}	Gate-Source Charge	V _{DS} =15V	-	4	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =4.5V	-	8	-	nC
t _{d(on)}	Turn-on Delay Time	V _{DS} =15V	-	14	-	ns
t _r	Rise Time	I _D =1A	-	10	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =6Ω	-	33	-	ns
t _f	Fall Time	V _{GS} =10V	-	18	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	1500	2400	pF
C _{oss}	Output Capacitance	V _{DS} =15V	-	320	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	210	-	pF
R _g	Gate Resistance	f=1.0MHz	-	1.2	2.4	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =20A, V _{GS} =0V	-	-	1.2	V
t _{rr}	Reverse Recovery Time	I _S =20A, V _{GS} =0V,	-	20	-	ns
Q _{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	5	-	nC

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Surface mounted on 1 in² copper pad of FR4 board, t ≤10sec; 60°C/W at steady state.
- 4.Package limitation current is 60A .

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

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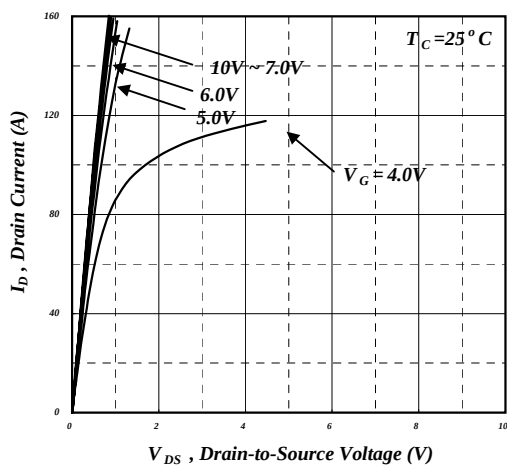


Fig 1. Typical Output Characteristics

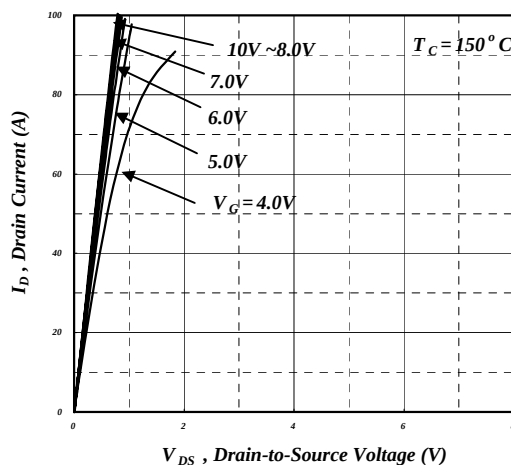


Fig 2. Typical Output Characteristics

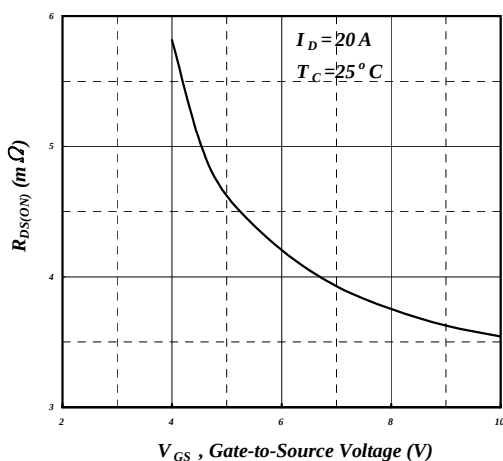


Fig 3. On-Resistance v.s. Gate Voltage

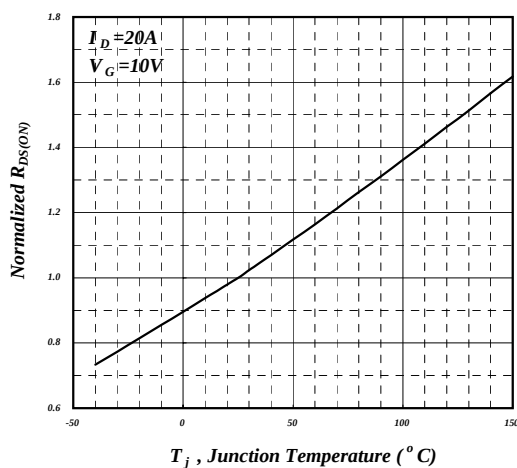


Fig 4. Normalized On-Resistance v.s. Junction Temperature

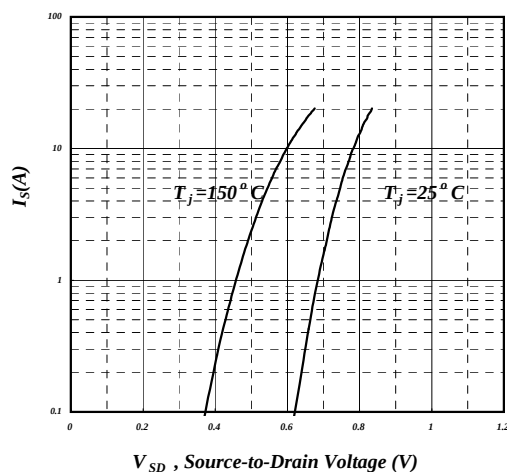


Fig 5. Forward Characteristic of Reverse Diode

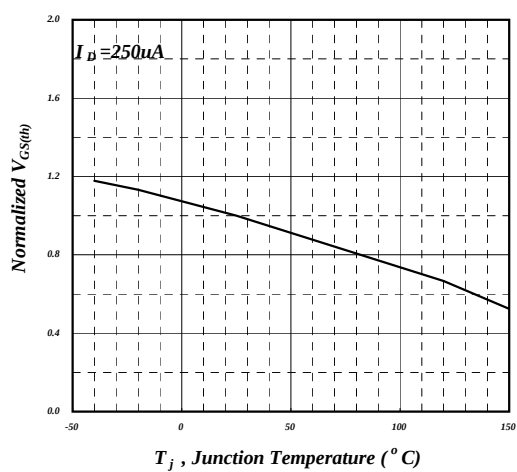


Fig 6. Gate Threshold Voltage v.s. Junction Temperature



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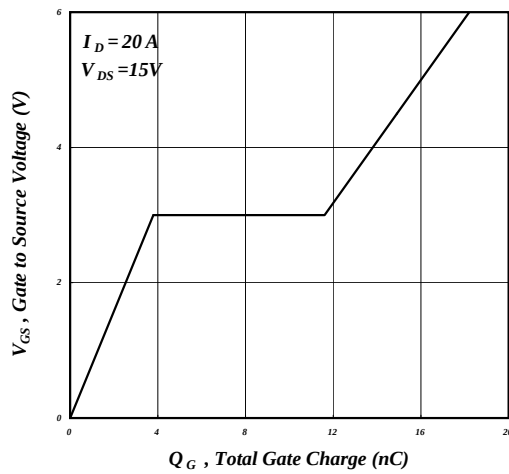


Fig 7. Gate Charge Characteristics

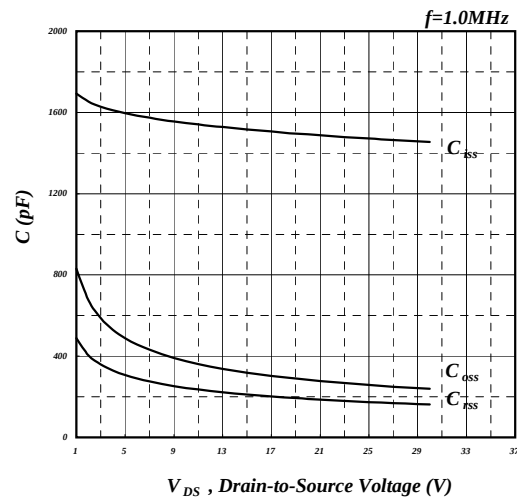


Fig 8. Typical Capacitance Characteristics

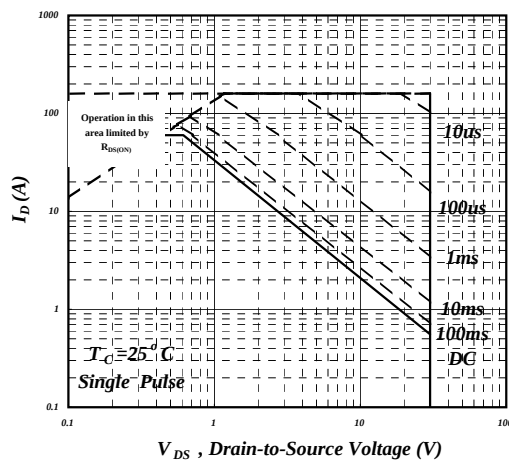


Fig 9. Maximum Safe Operating Area

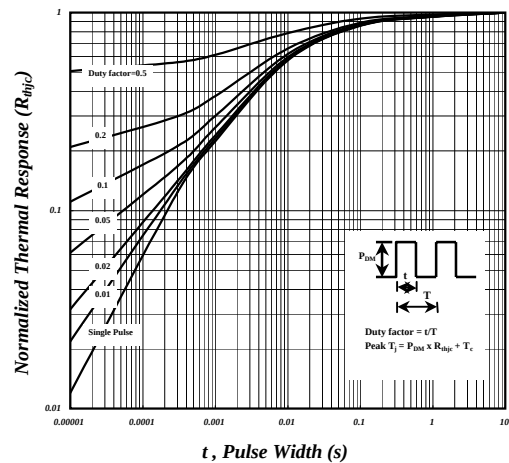


Fig 10. Effective Transient Thermal Impedance

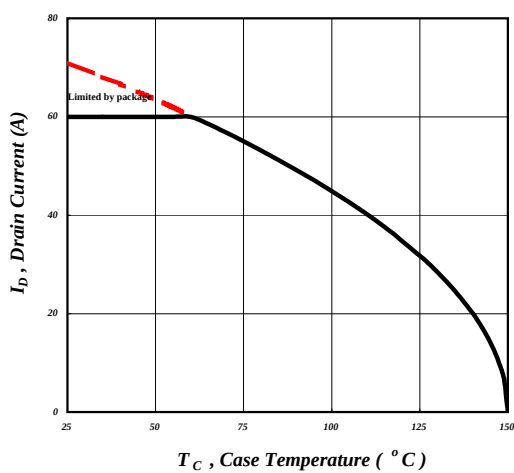


Fig 11. Drain Current v.s. Case Temperature

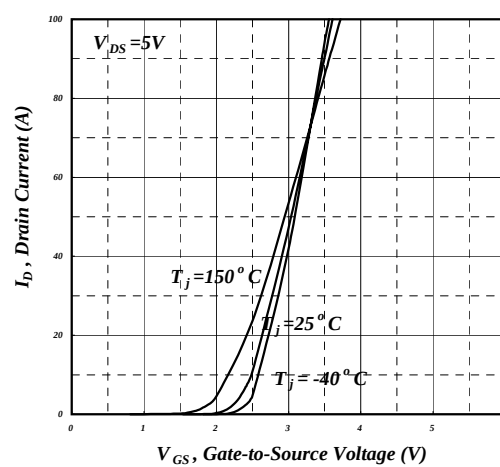


Fig 12. Transfer Characteristics

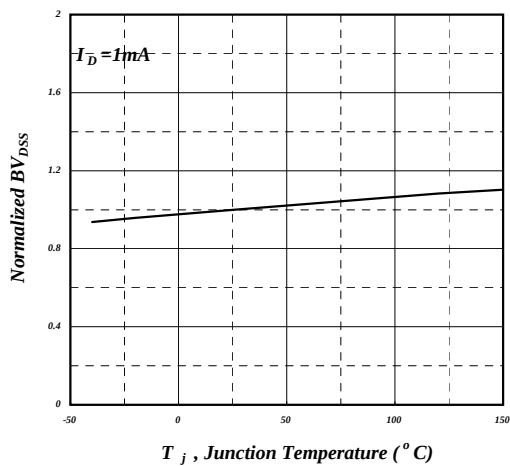


Fig 13. Normalized BV_{DSS} v.s. Junction

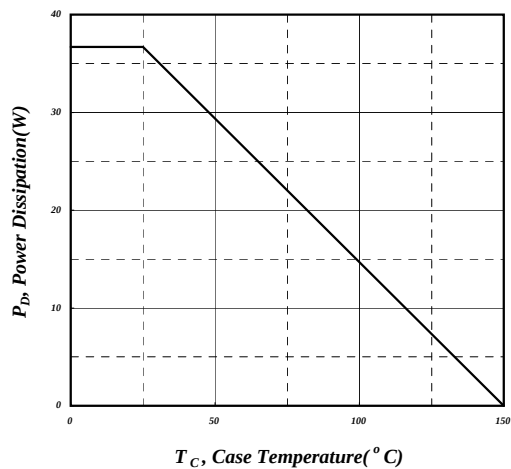


Fig 14. Total Power Dissipation

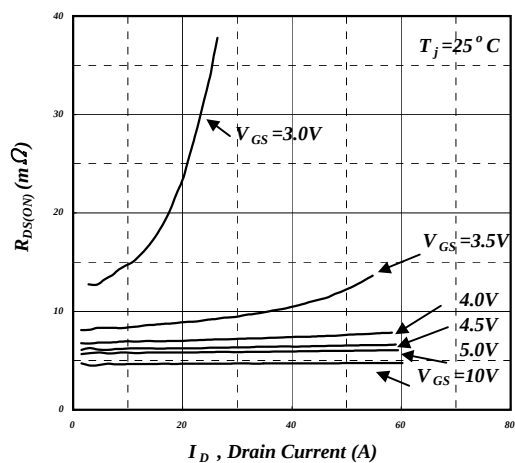


Fig 15. Typ. Drain-Source on State Resistance



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MARKING INFORMATION

