

20V NP+NP-Channel Enhancement Mode MOSFET

Description

The AP3HV02LI uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = 20V$ $I_D = 3.3A$

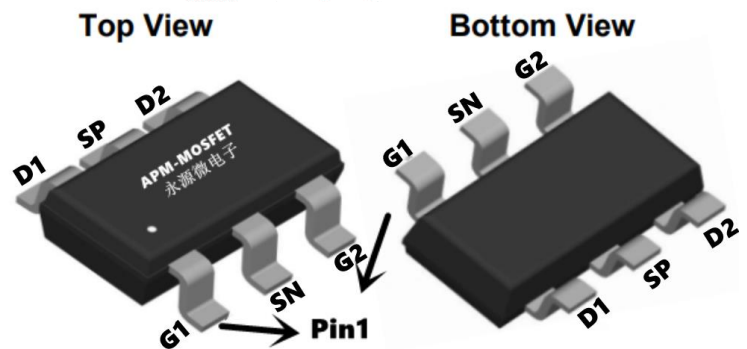
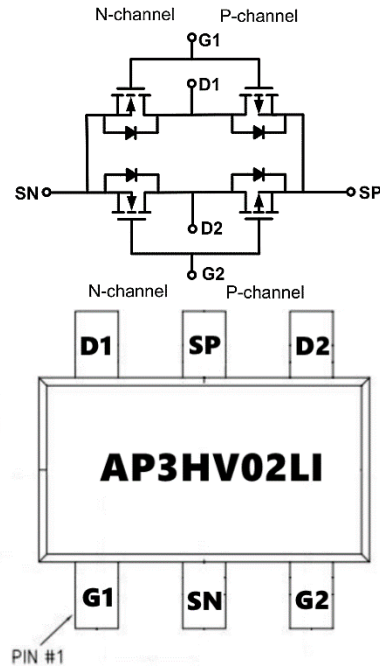
$R_{DS(ON)} < 50m\Omega$ @ $V_{GS}=4.5V$ (Type: 42m Ω)

$V_{DS} = -20V$ $I_D = -2.8A$

$R_{DS(ON)} < 120m\Omega$ @ $V_{GS}=-4.5V$ (Type: 95m Ω)

Application

BLDC



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP3HV02LI	SOT23-6L	AP3HV02LI	3000

Absolute Maximum Ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	N-Ch	P-Ch	Units
V_{DS}	Drain-Source Voltage	20	-20	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
$I_D @ T_A = 25^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V^1$	3.3	-2.8	A
$I_D @ T_A = 70^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V^1$	1.5	-1.0	A
I_{DM}	Pulsed Drain Current ²	52	-40	A
EAS	Single Pulse Avalanche Energy ³	12	18	mJ
$P_D @ T_A = 25^{\circ}C$	Total Power Dissipation ⁴	1.5	1.5	W
T_{STG}	Storage Temperature Range	-55 to 150		$^{\circ}C$
T_J	Operating Junction Temperature Range	-55 to 150		$^{\circ}C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	105		$^{\circ}C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	50		$^{\circ}C/W$

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N-Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	20	22	---	V
RDS(ON)	Static Drain-Source On-Resistance ²	V _{GS} =4.5V, I _D =3A	---	42	50	mΩ
		V _{GS} =2.5V, I _D =2A	---	55	65	
VGS(th)	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	0.4	0.6	1.2	V
IDSS	Drain-Source Leakage Current	V _{DS} =16V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =16V, V _{GS} =0V, T _J =55°C	---	---	5	
IGSS	Gate-Source Leakage Current	V _{GS} =±12V, V _{DS} =0V	---	---	±100	nA
gfs	Forward Transconductance	V _{DS} =5V, I _D =3A	---	10.5	---	S
Q _g	Total Gate Charge (4.5V)	V _{DS} =15V, V _{GS} =4.5V, I _D =3A	---	4.6	---	nC
Q _{gs}	Gate-Source Charge		---	0.7	---	
Q _{gd}	Gate-Drain Charge		---	1.5	---	
Td(on)	Turn-On Delay Time	V _{DD} =10V, V _{GS} =4.5V, R _G =3.3Ω, I _D =3A	---	1.6	---	ns
T _r	Rise Time		---	42	---	
Td(off)	Turn-Off Delay Time		---	14	---	
T _f	Fall Time		---	7	---	
Ciss	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz	---	310	---	pF
Coss	Output Capacitance		---	49	---	
Crss	Reverse Transfer Capacitance		---	35	---	
IS	Continuous Source Current ^{1,4}	V _G =V _D =0V, Force Current	---	---	3.6	A
VSD	Diode Forward Voltage ²	V _{GS} =0V, I _S =1A, T _J =25°C	---	---	1.2	V

Note :

- 1、The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
- 3、The power dissipation is limited by 150°C junction temperature
- 4、The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

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P-Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D = -250μA	-20	-	-	V
IDSS	Zero Gate Voltage Drain Current	V _{DS} = -20V, V _{GS} = 0V,	-	-	-1	μA
IGSS	Gate to Body Leakage Current	V _{DS} =0V, V _{GS} = ±12V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = -250μA	-0.4	-0.7	-1.0	V
RDS(on)	Static Drain-Source on-Resistance	V _{GS} =-4.5V, I _D =-2A	-	95	120	mΩ
		V _{GS} =-2.5V, I _D =-1A	-	135	190	
Ciss	Input Capacitance	V _{DS} = -10V, V _{GS} = 0V, f = 1.0MHz	-	185	-	pF
Coss	Output Capacitance		-	35	-	pF
Crss	Reverse Transfer Capacitance		-	25	-	pF
Q _g	Total Gate Charge	V _{DS} = -10V, I _D = -2A, V _{GS} = -4.5V	-	2.2	-	nC
Q _{gs}	Gate-Source Charge		-	0.5	-	nC
Q _{gd}	Gate-Drain(“Miller”) Charge		-	0.5	-	nC
td(on)	Turn-on Delay Time	V _{DD} = -10V, R _L =5Ω, R _{GEN} =3Ω, V _{GS} =-4.5V,	-	10	-	ns
tr	Turn-on Rise Time		-	30	-	ns
td(off)	Turn-off Delay Time		-	63	-	ns
tr	Turn-off Fall Time		-	50	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	-2.8	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-8	A
VSD	Drain to Source Diode Forward Voltage	V _{GS} = 0V, I _S = -2A	-	-	-1.2	V

Note :

- 1、 The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3、 The power dissipation is limited by 150°C junction temperature
- 4、 The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.



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N-Channel Typical Characteristics

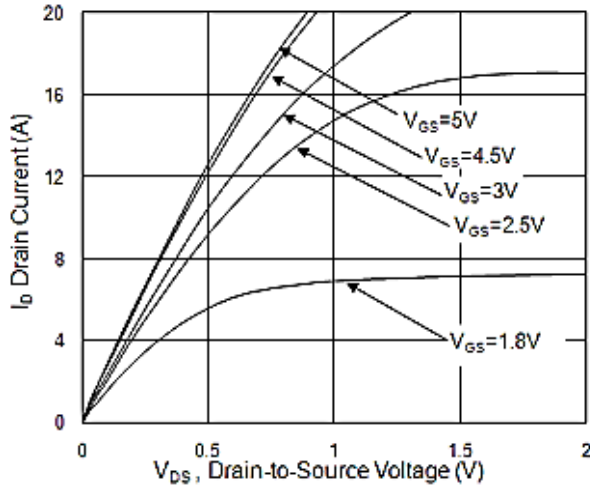


Fig.1 Typical Output Characteristics

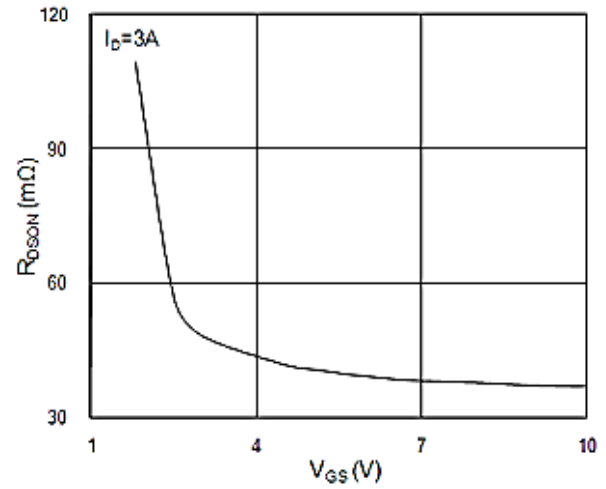
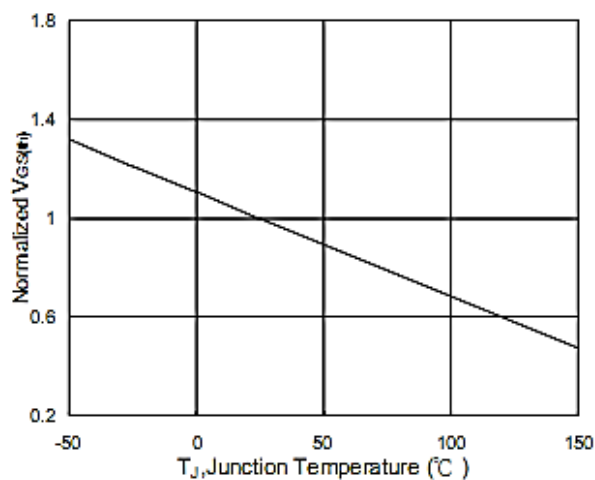
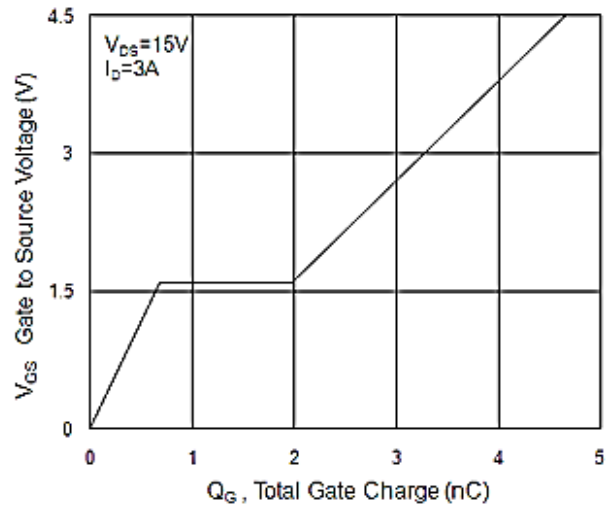
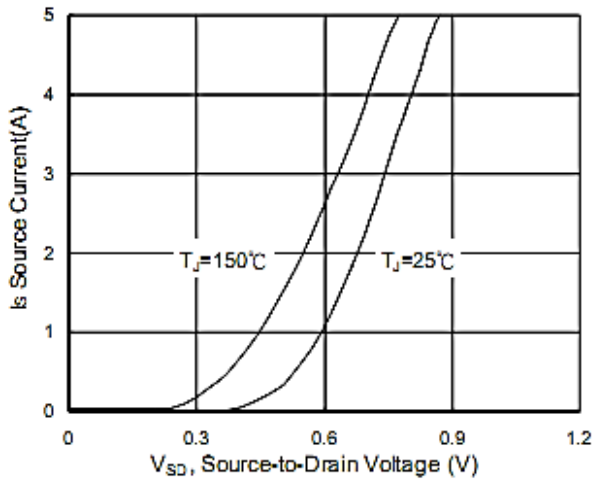
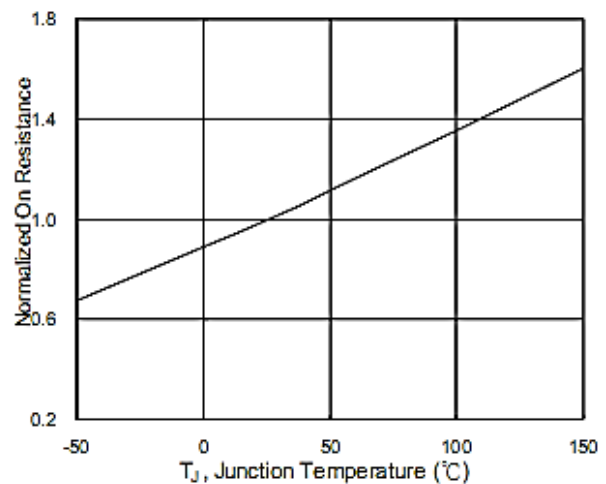
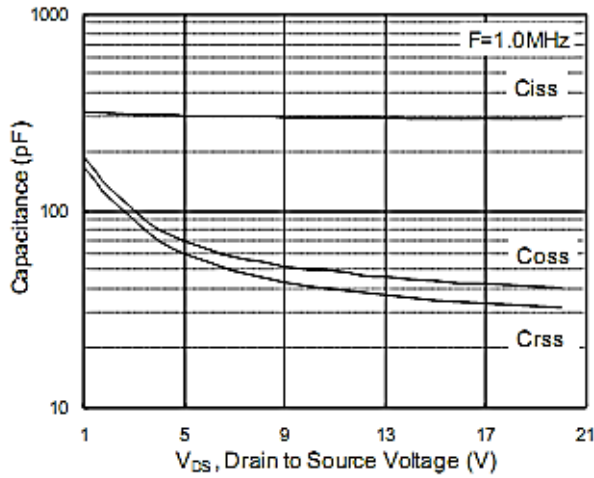
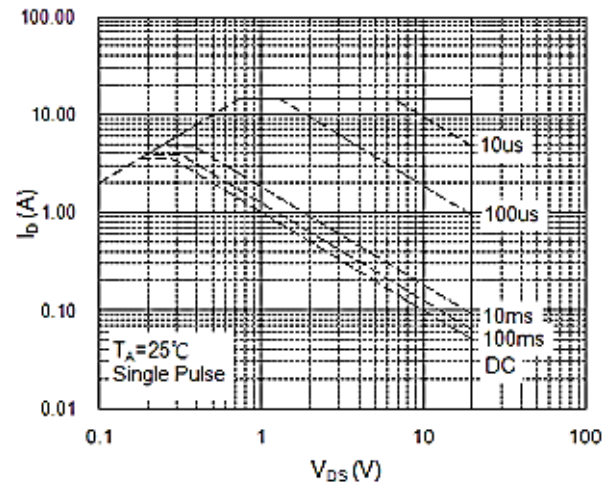
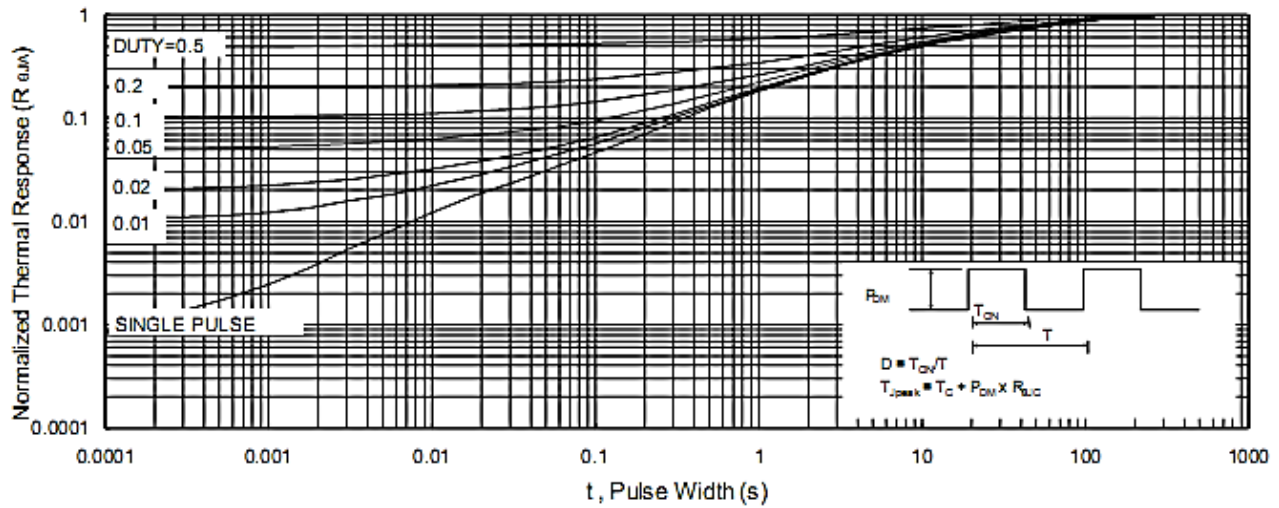
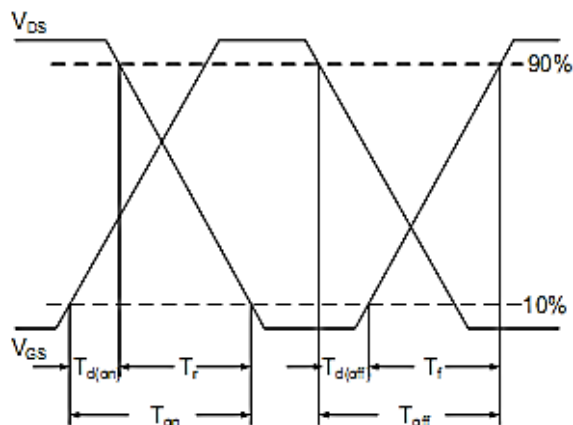
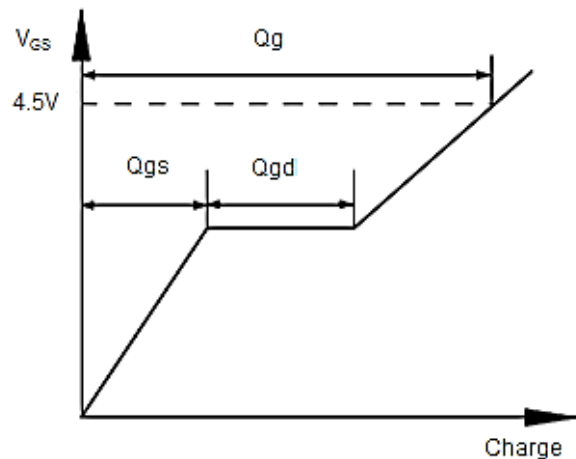


Fig.2 On-Resistance vs. G-S Voltage

Fig.5 Normalized $V_{GS(th)}$ vs. T_J Fig.6 Normalized $R_{DS(on)}$ vs. T_J

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AP3HV02LI**20V NP+NP-Channel Enhancement Mode MOSFET****Fig.7 Capacitance****Fig.8 Safe Operating Area****Fig.9 Normalized Maximum Transient Thermal Impedance****Fig.10 Switching Time Waveform****Fig.11 Gate Charge Waveform**

20V NP+NP-Channel Enhancement Mode MOSFET

P-Channel Typical Characteristics

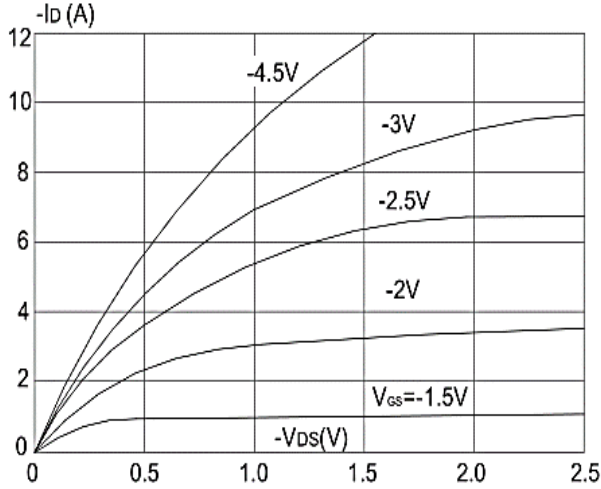


Figure1: Output Characteristics

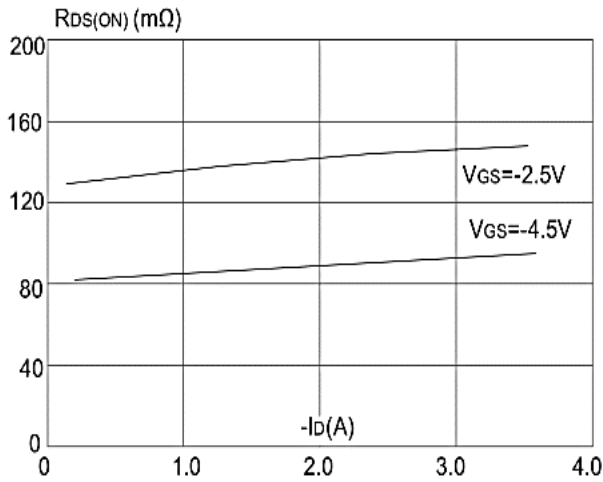


Figure 3: On-resistance vs. Drain Current

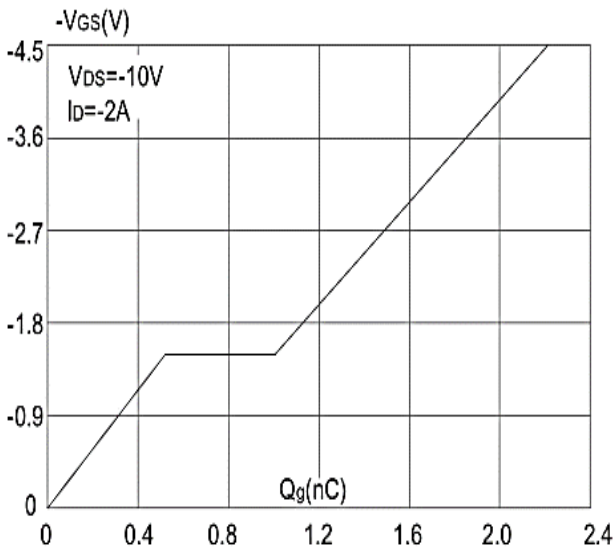


Figure 5: Gate Charge Characteristics

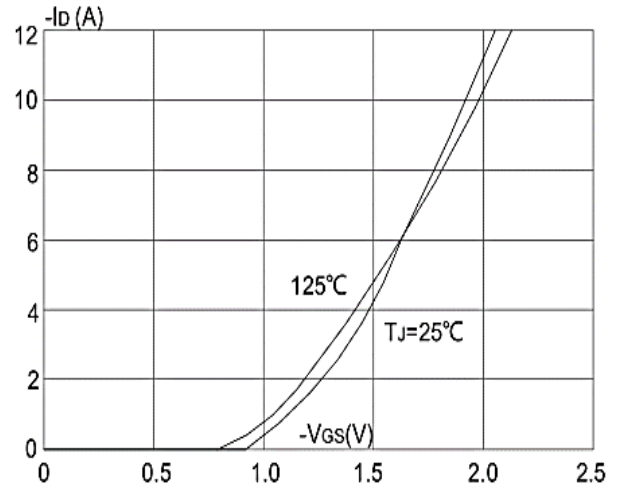


Figure 2: Typical Transfer Characteristics

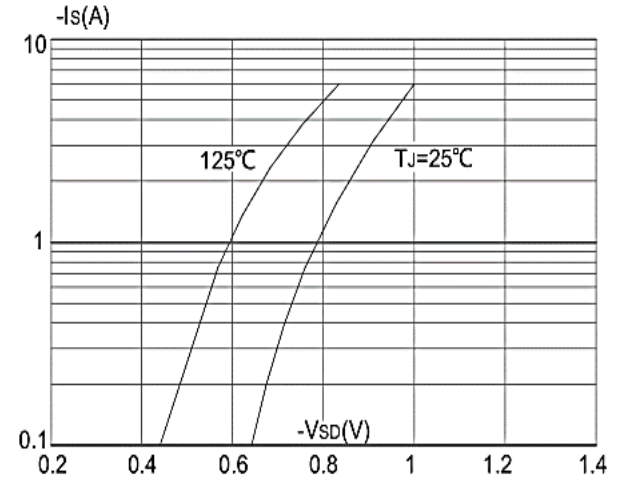


Figure 4: Body Diode Characteristics

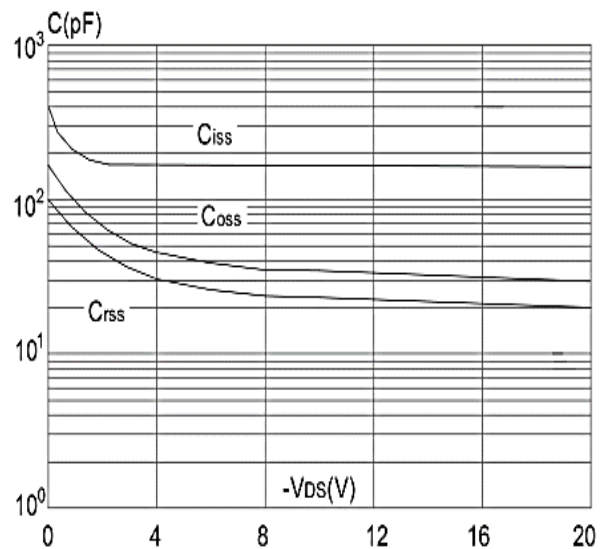


Figure 6: Capacitance Characteristics

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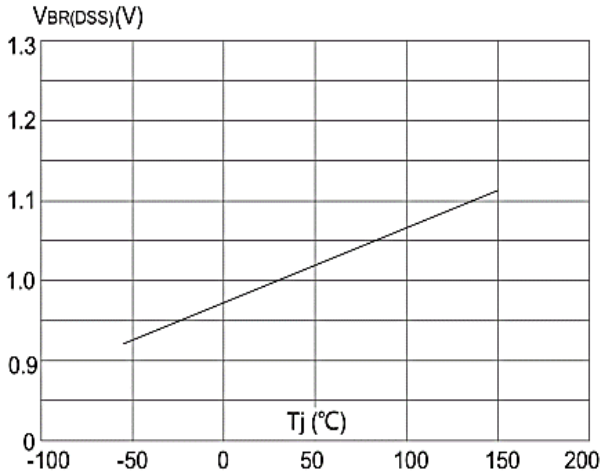


Figure 7: Normalized Breakdown Voltage vs Junction Temperature

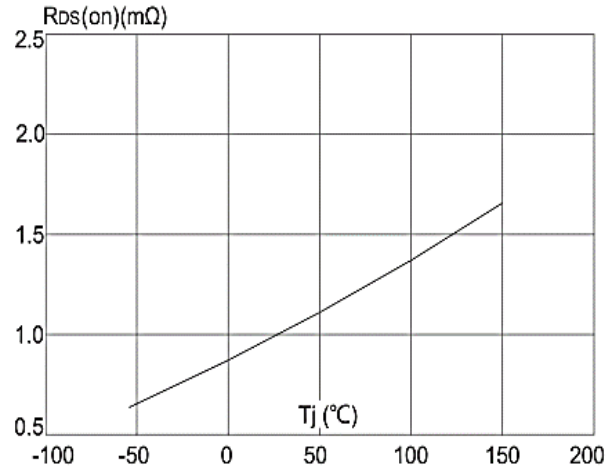


Figure 8: Normalized on Resistance vs. Junction Temperature

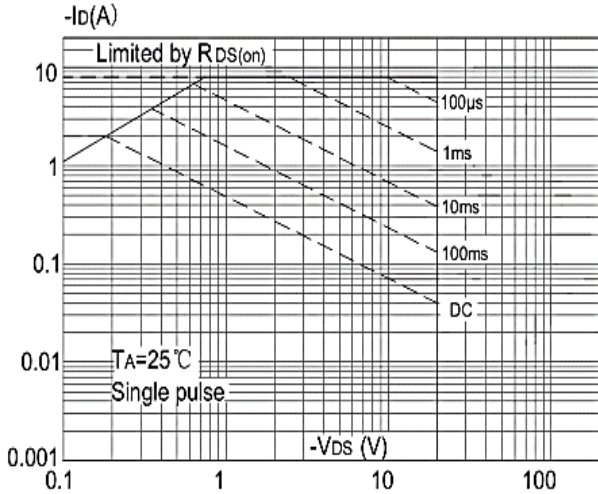


Figure 9: Maximum Safe Operating Area

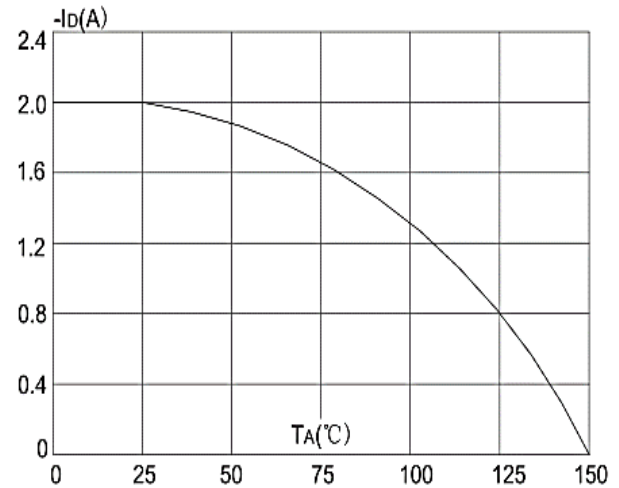


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

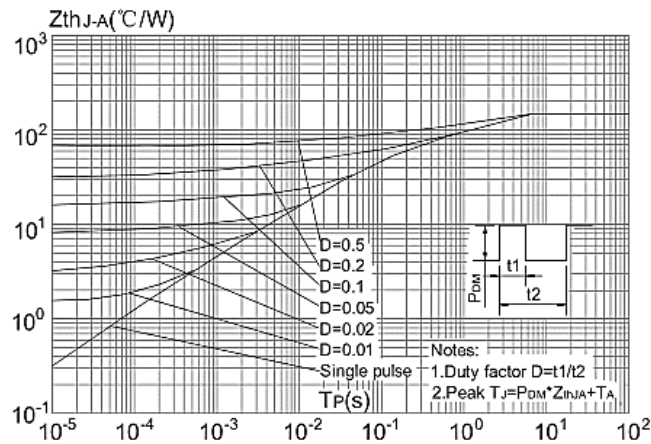
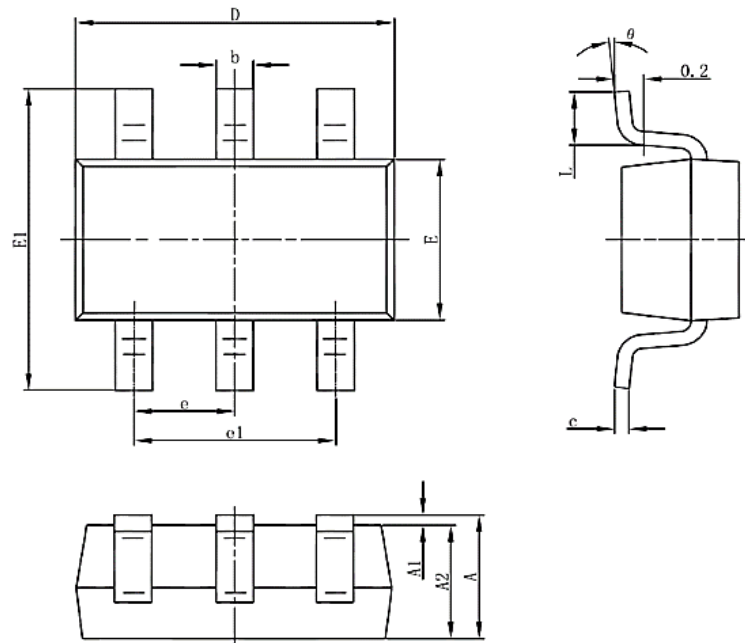


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambien

Package Mechanical Data-SOT23-6-Double



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
C	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 (BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0	8	0	8

20V N+P-Channel Enhancement Mode MOSFET**Attention**

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Edition	Date	Change
REV1.0	2021/12/21	Initial release

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