

## 30V N-Channel Enhancement Mode MOSFET

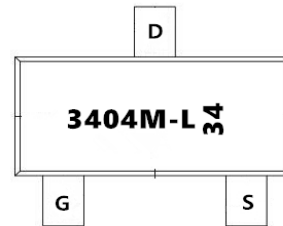
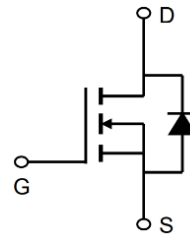
### Description

The AP3404MI-L uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

### General Features

$V_{DS} = 30V$   $I_D = 6.2A$

$R_{DS(ON)} < 24m\Omega$  @  $V_{GS}=10V$  (Type: 18m $\Omega$ )

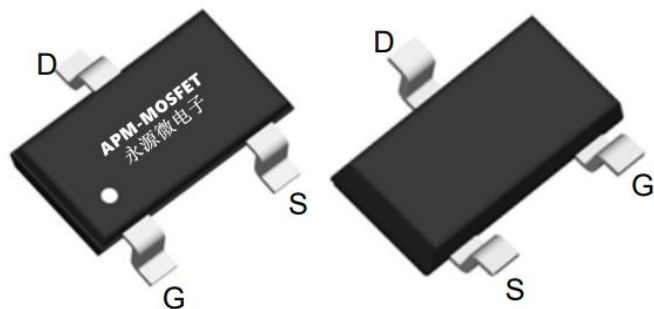


### Application

Lithium battery protection  
Wireless impact  
Mobile phone fast charging

Top View

Bottom View



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP3404MI-L	SOT23-3L	3404	3000

### Absolute Maximum Ratings ( $T_C=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	30	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_A=25^{\circ}C$	Continuous Drain Current	6.2	A
$I_D@T_A=70^{\circ}C$	Continuous Drain Current	4.1	A
IDM	Pulsed Drain Current <sup>2</sup>	20	A
$P_D@T_A=25^{\circ}C$	Total Power Dissipation <sup>3</sup>	1.25	W
TSTG	Storage Temperature Range	-55 to 150	$^{\circ}C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^{\circ}C$
$R_{\theta JA}$	Thermal Resistance Junction-ambient <sup>1</sup>	125	$^{\circ}C/W$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup> ( $t \leq 10s$ )	85	$^{\circ}C/W$

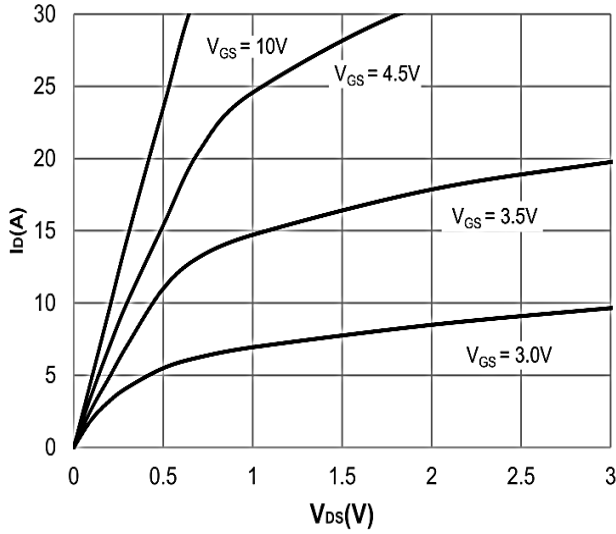
**30V N-Channel Enhancement Mode MOSFET**
**Electrical Characteristics ( $T_c=25^{\circ}\text{C}$  unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$	30	33	-	V
IDSS	Zero Gate Voltage Drain Current	$V_{DS} = 30\text{V}$ , $V_{GS} = 0\text{V}$	-	-	1.0	$\mu\text{A}$
IGSS	Gate-Body Leakage Current	$V_{DS} = 0\text{V}$ , $V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA
VGS(th)	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 250\mu\text{A}$	1.2	1.6	2.5	V
RDS(ON)	Static Drain-Source ON-Resistance	$V_{GS} = 10\text{V}$ , $I_D = 4\text{A}$	-	18	25	m $\Omega$
		$V_{GS} = 4.5\text{V}$ , $I_D = 3\text{A}$	-	27	35	m $\Omega$
Ciss	Input Capacitance	$V_{GS}=0\text{V}$ , $V_{DS}=15\text{V}$ , $f=1\text{MHz}$	-	388	-	pF
Coss	Output Capacitance		-	57	-	pF
Crss	Reverse Transfer Capacitance		-	45	-	pF
Qg	Total Gate Charge	$V_{GS}=0$ to $10\text{V}$ $V_{DS}=15\text{V}$ , $I_D=3\text{A}$	-	9	-	nC
Qgs	Gate Source Charge		-	1.5	-	nC
Qgd	Gate Drain("Miller") Charge		-	2	-	nC
td(on)	Turn-On DelayTime	$V_{GS}=10\text{V}$ , $V_{DD}=15\text{V}$ $I_D=3\text{A}$ , $R_{GEN}=3\Omega$	-	2	-	ns
tr	Turn-On Rise Time		-	6	-	ns
td(off)	Turn-Off DelayTime		-	61	-	ns
tf	Turn-Off Fall Time		-	34	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	5	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	20	A
VSD	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}$ , $I_S = 5\text{A}$	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	$I_F = 3\text{A}$ , $di/dt = 100\text{A/us}$	-	6	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	2	-	nC

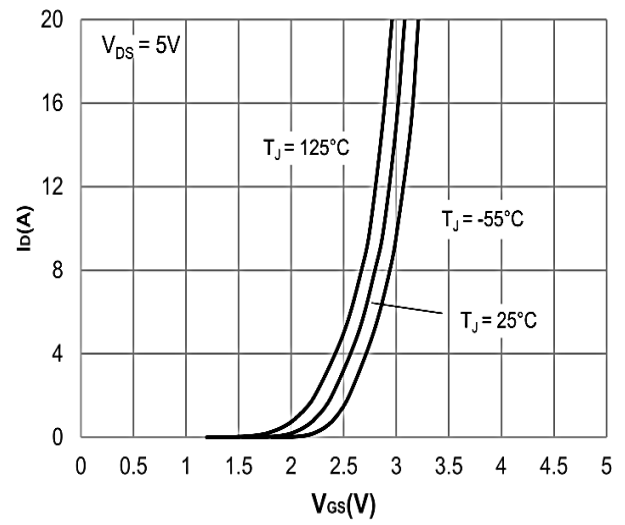
**Note :**

- 1、The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width  $\leq 300\mu\text{s}$  , duty cycle  $\leq 2\%$
- 3、The power dissipation is limited by  $150^{\circ}\text{C}$  junction temperature
- 4、The data is theoretically the same as  $I_D$  and  $I_{DM}$  , in real applications , should be limited by total power dissipation.

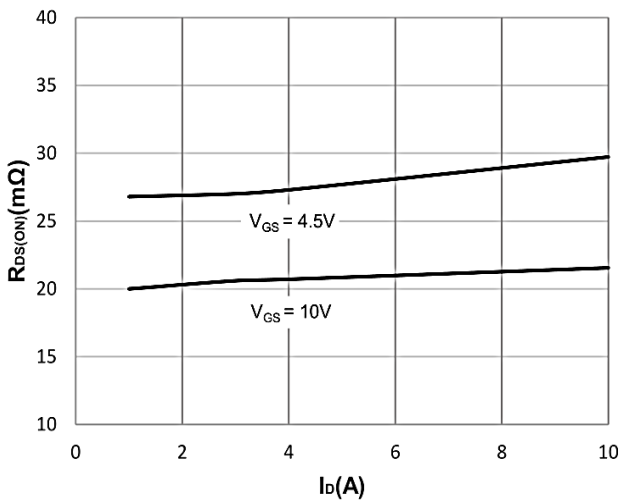
**Typical Characteristics**



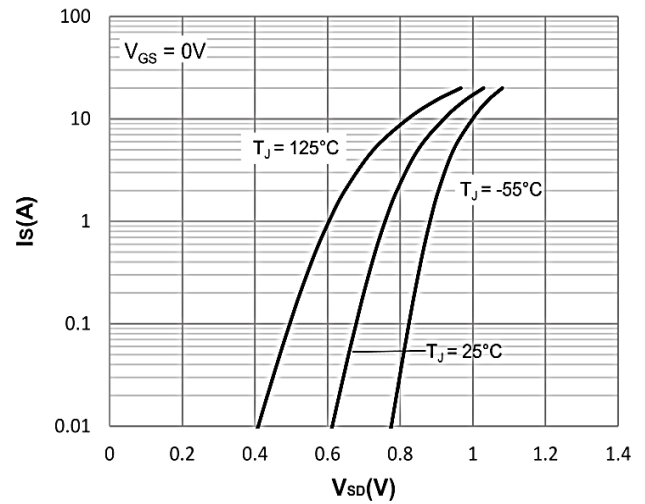
**Figure 1: Output Characteristics**



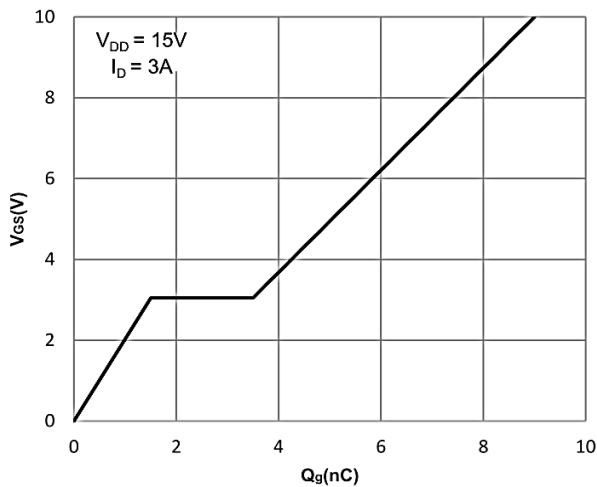
**Figure 2: Typical Transfer Characteristics**



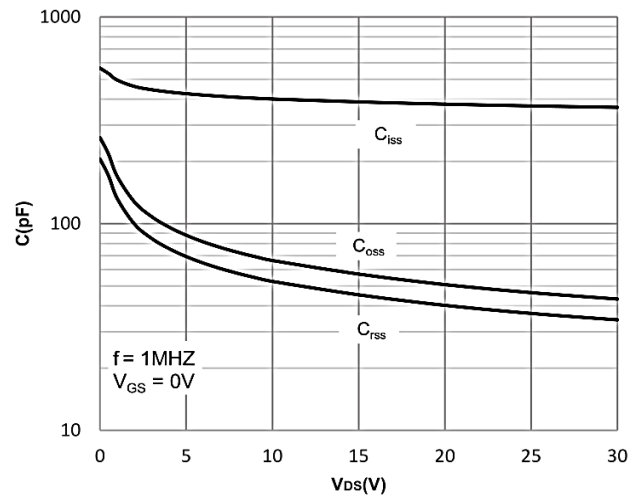
**Figure 3: On-resistance vs. Drain Current**



**Figure 4: Body Diode Characteristics**

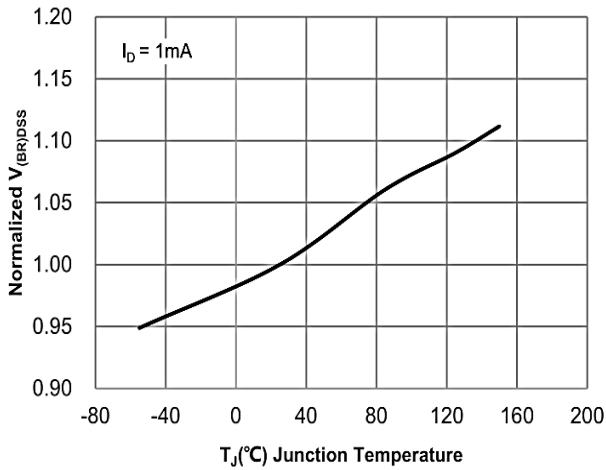


**Figure 5: Gate Charge Characteristics**

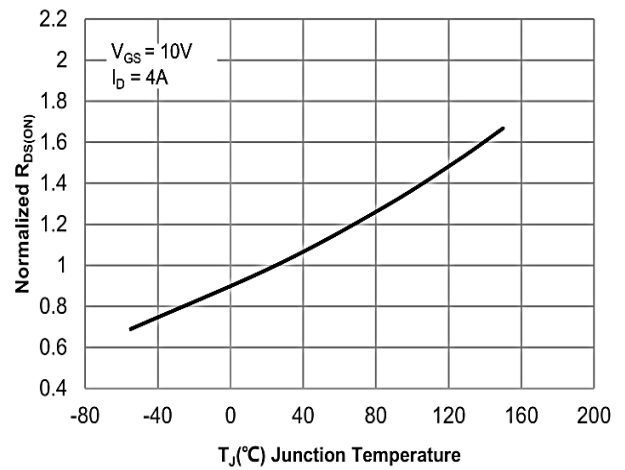


**Figure 6: Capacitance Characteristics**

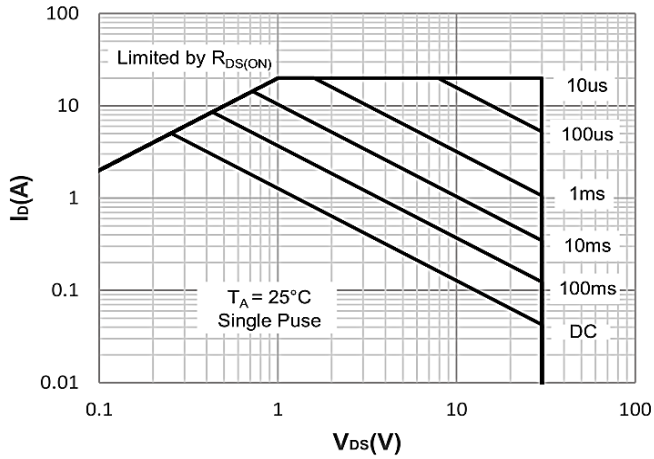
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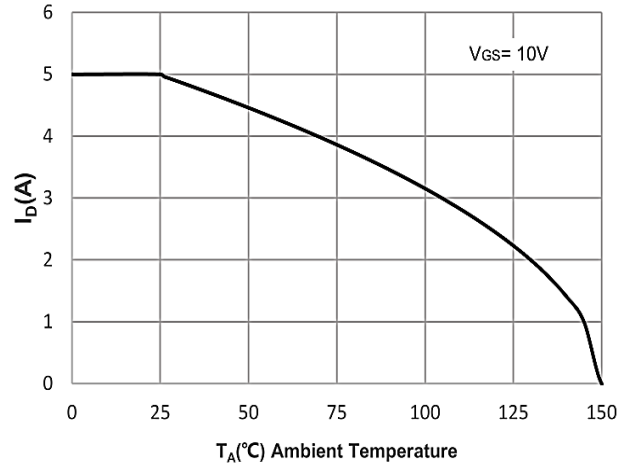
**Figure 7: Normalized Breakdown voltage vs. Junction Temperature**



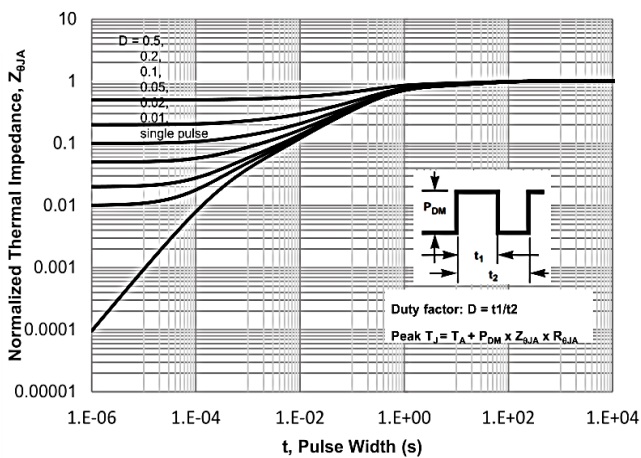
**Figure 8: Normalized on Resistance vs. Junction Temperature**



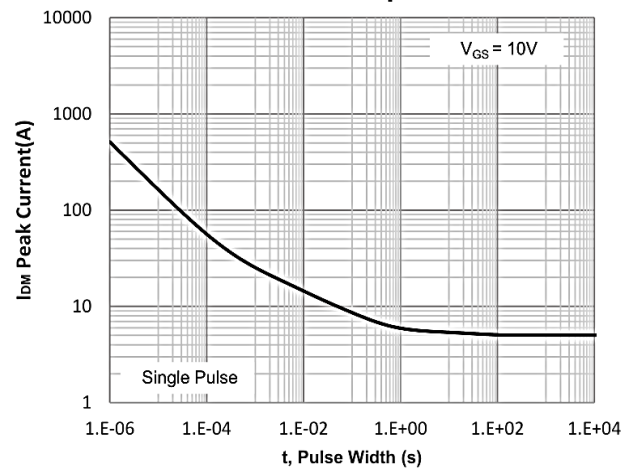
**Figure 9: Maximum Safe Operating Area**



**Figure 10: Maximum Continuous Drain Current vs. Case Temperature**



**Figure 11: Normalized Maximum Transient Thermal Impedance**



**Figure 12: Peak Current Capacity**

**30V N-Channel Enhancement Mode MOSFET****Attention**

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Edition	Date	Change
REV1.0	2023/8/31	Initial release

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