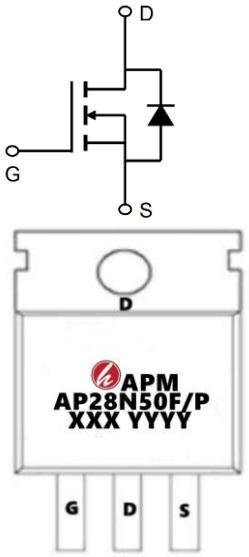
# AP28N50F/P

## 500V N-Channel Enhancement Mode MOSFET

### Description

The AP28N50F/P is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.




### General Features

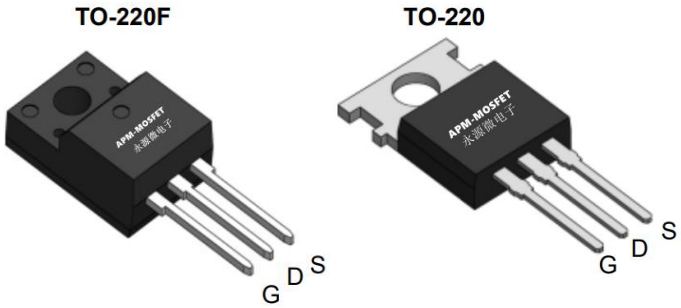
$V_{DS}$ = 500V $I_D$ =28A

$R_{DS(ON)}$ < 260mΩ @ $V_{GS}$=10V （**Type：195mΩ**）

### Application

Uninterruptible Power Supply(UPS)

Power Factor Correction (PFC)




## Package Marking and Ordering Information

| Product ID | Pack | Marking | Qty(PCS) |
|---|---|---|---|
| AP28N50F | TO-220F-3L | AP28N50F XXX YYYY | 1000 |
| AP28N50P | TO-220-3L | AP28N50P XXX YYYY | 1000 |

## Absolute Maximum Ratings ($T_C$=25℃unless otherwise noted)

| Symbol | Parameter | Value | Units |
|---|---|---|---|
| VDSS | Drain-Source Voltage | 500 | V |
| ID | Drain Current - Continuous | 28 | A |
| IDM | Drain Current - Pulsed | 80* | A |
| VGSS | Gate-Source Voltage | ± 30 | V |
| EAS | Single Pulsed Avalanche Energy (Note 2) | 957 | mJ |
| IAR | Avalanche Current (Note 1) | 20 | A |
| EAR | Repetitive Avalanche Energy (Note 1) | 101 | mJ |
| dv/dt | Peak Diode Recovery dv/dt (Note 3) | 5 | V/ns |
| $P_D$ | Power Dissipation (TC = 25°C) | 37.0 | W/°C |
| Tj ,Tstg | Operating and Storage Temperature Range | -55 to +150 | °C |
| RθJC | Thermal Resistance, Junction-to-Case | 3.69 | °C/W |
| RθJA | Thermal Resistance, Junction-to-Ambient | 44.2 | °C/W |

## 500V N-Channel Enhancement Mode MOSFET

### Electrical Characteristics ($T_J$=25℃, unless otherwise noted)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 μA | 500 | | | V |
| $\Delta BV_{DSS}$ / $\Delta T_J$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, | | 0.51 | | V/°C |
| IDSS | Zero Gate Voltage Drain Current | $V_{DS}$ = 500 V, $V_{GS}$ = 0 V | | | 1 | μA |
| | | $V_{DS}$ = 400 V, TC = 125° C | | | 10 | μA |
| IGSSF | Gate-Body Leakage Current, Forward | $V_{GS}$ = 30 V, $V_{DS}$ = 0 V | | | 100 | nA |
| IGSSR | Gate-Body Leakage Current, Reverse | $V_{GS}$ = -30 V, $V_{DS}$ = 0 V | | | -100 | nA |
| VGS(TH) | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$, $I_D$ =250 uA | 3.0 | | 5.0 | V |
| RDS(On) | Drain-Source On-state Resistance | $V_{GS}$=10 V, $I_D$ =10 A, $T_J$ = 25°C | | 195 | 260 | mΩ |
| gFS | Forward Transconductance | $V_{DS}$ = 40 V, $I_D$ = 10 A (Note 4) | | 19 | | S |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 25 V, $V_{GS}$ = 0 V, f = 1.0 MHz | | 2340 | | pF |
| $C_{oss}$ | Output Capacitance | | | 339 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 7.7 | | pF |
| td(on) | Turn On Delay Time | $V_{DD}$ = 250 V, ID = 20 A, $R_G$ = 25 Ω (Note 4, 5) | | 36 | | ns |
| $t_r$ | Rising Time | | | 50 | | ns |
| td(off) | Turn Off Delay Time | | | 95 | | ns |
| $t_f$ | Fall Time | | | 44 | | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 250 V, ID = 20 A, $V_{GS}$ = 10 V (Note 4, 5) | | 40 | | nC |
| $Q_{gs}$ | Gate-Source Charge | | | 13 | | nC |
| $Q_{gd}$ | Gate-Drain Charge | | | 12 | | nC |
| ISM | Maximum Pulsed Drain-Source Diode Forward Current | | | | 80 | A |
| $V_{SD}$ | Diode Forward Voltage | $V_{GS}$= 0 V, $I_S$ = 20 A | | | 1.4 | V |
| trr | Reverse Recovery Time | $V_{GS}$ = 0 V, $I_S$ = 20 A, $dI_F$ / dt = 100 A/μs Note 4) | | 345 | | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | | 4.6 | | μC |

**Note :**

1、The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.

2、The EAS data shows Max. rating . L=4.1Mh IAS=18A, VDD=50V, RG=25Ω, Starting TJ = 25 ºC

3、The test condition is Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%

4、The power dissipation is limited by 150℃ junction temperature

5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

## Typical Characteristics

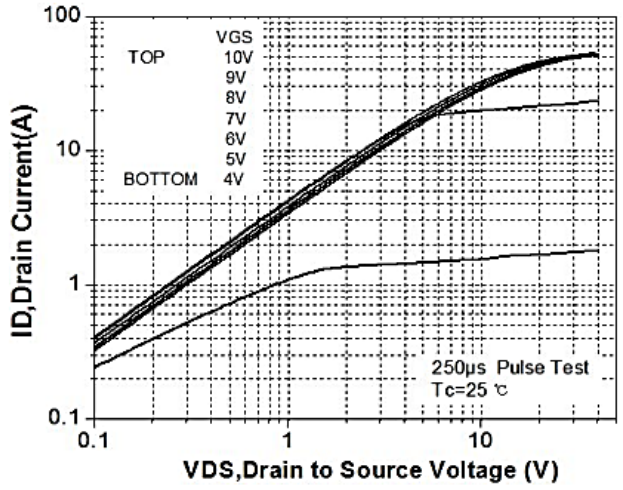



Figure 1. On-Region Characteristics

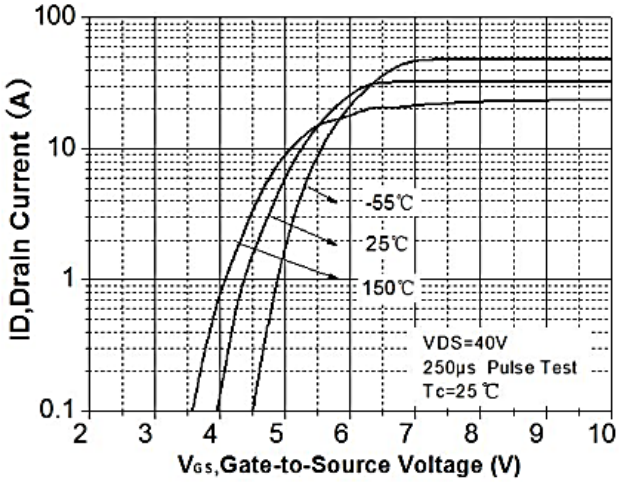



Figure 2. Transfer Characteristics

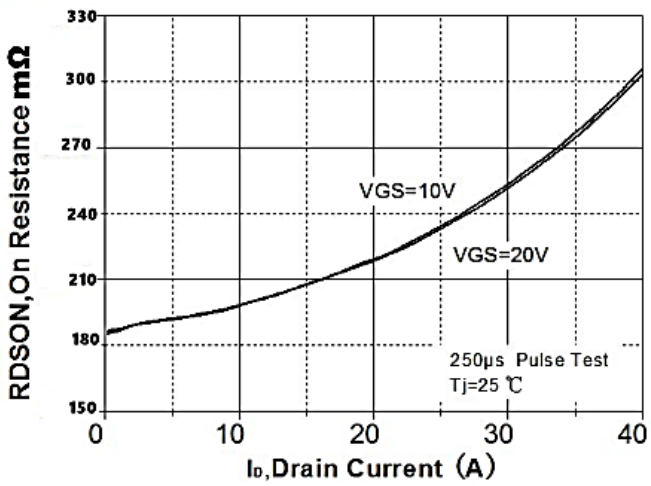



Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

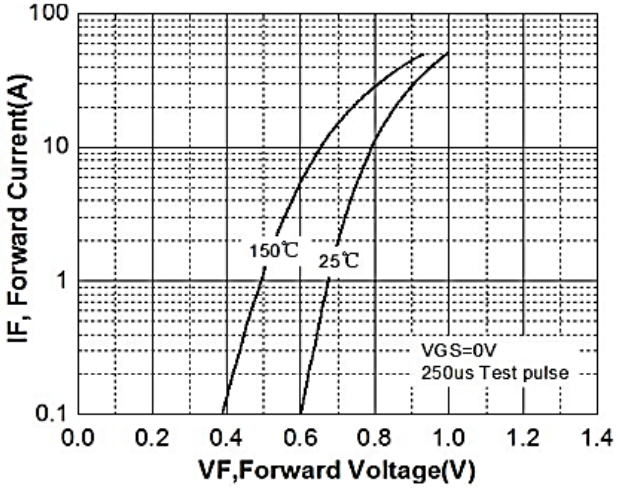



Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

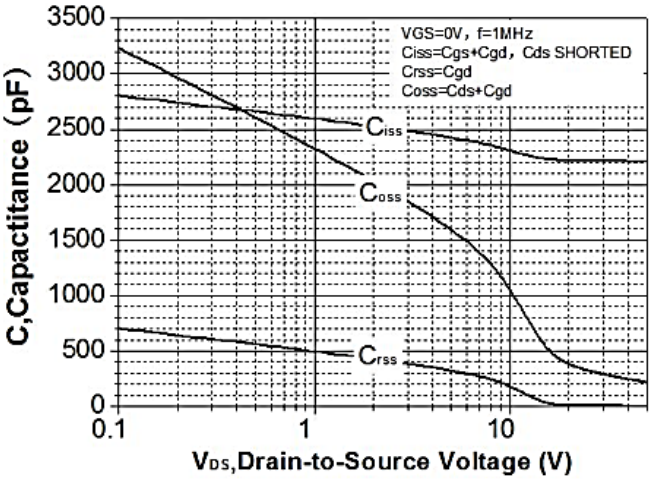



Figure 5. Capacitance Characteristics

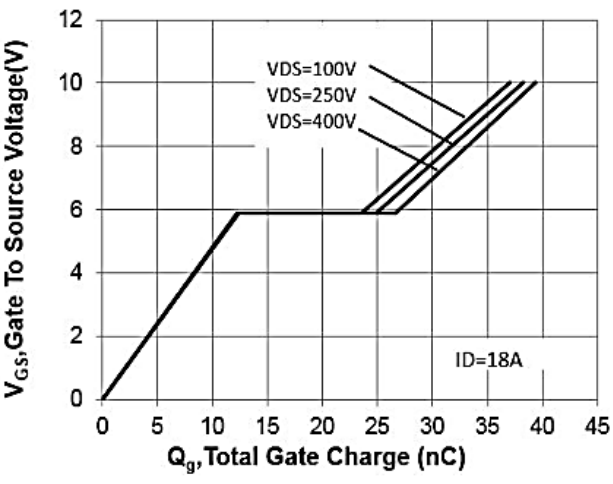



Figure 6. Gate Charge Characteristics

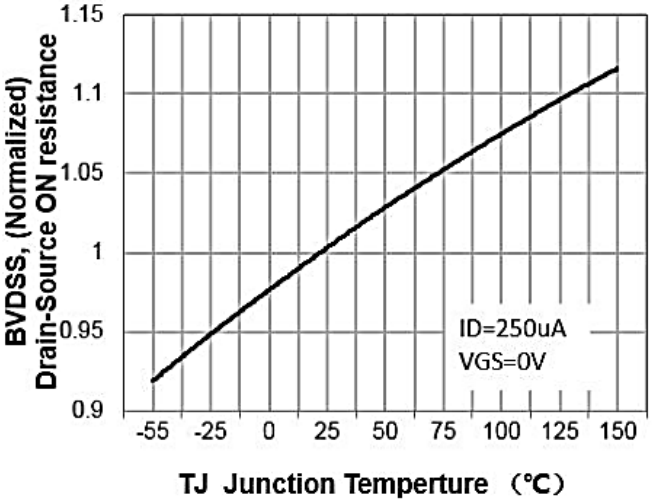



Figure 7. Breakdown Voltage Variation vs Temperature

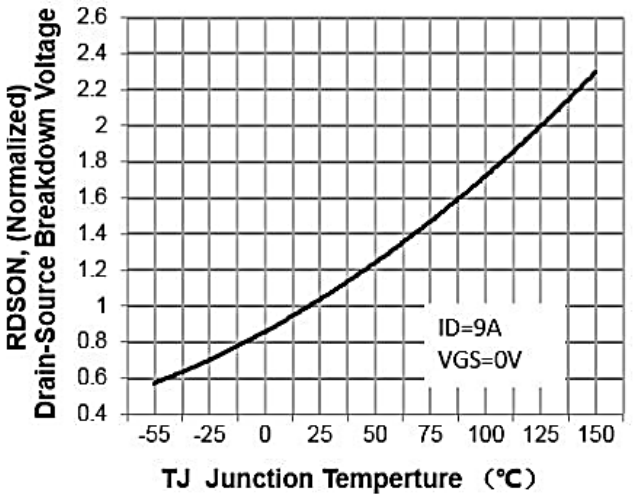



Figure 8. On-Resistance Variation vs Temperature

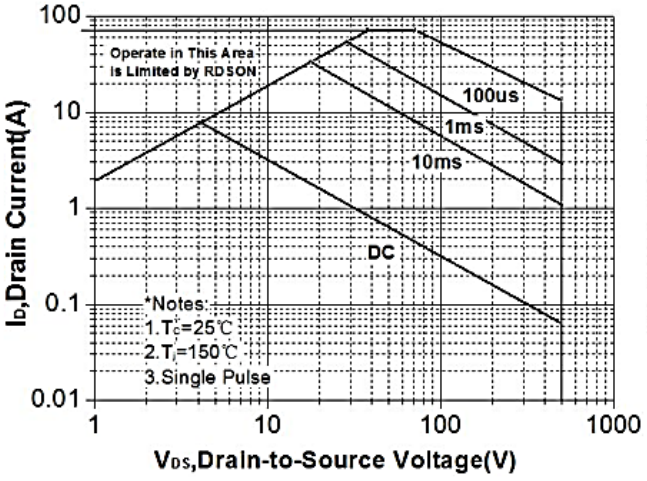



Figure 9. Maximum Safe Operating Area

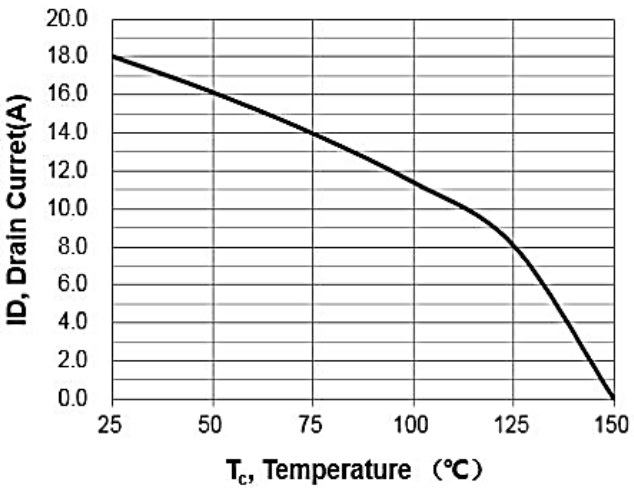



Figure 10. Maximum Drain Current vs Case Temperature

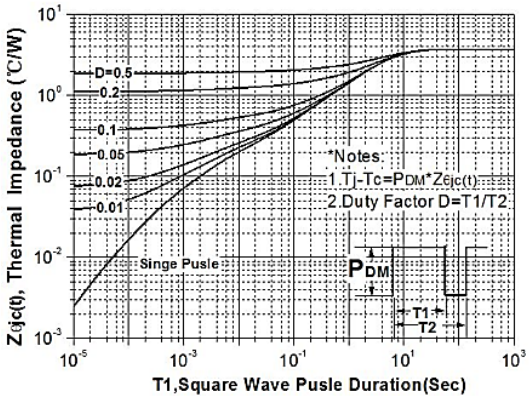



Figure 11. Transient Thermal Response Curve

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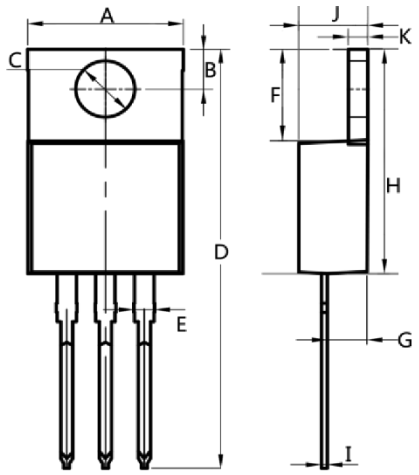


| Dim. | Min. | Max. |
|---|---|---|
| A | 10.0 | 10.4 |
| B | 2.5 | 3.0 |
| C | 3.5 | 4.0 |
| D | 28.0 | 30.0 |
| E | 1.1 | 1.5 |
| F | 6.2 | 6.6 |
| G | 2.9 | 3.3 |
| H | 15.0 | 16.0 |
| I | 0.35 | 0.45 |
| J | 4.3 | 4.7 |
| K | 1.2 | 1.4 |
| All Dimensions in millimeter | | |

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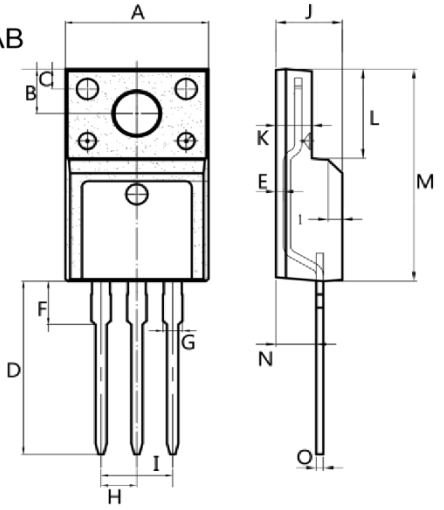


| Dim. | Min. | Max. |
|---|---|---|
| A | 9.9 | 10.3 |
| B | 2.9 | 3.5 |
| C | 1.15 | 1.45 |
| D | 12.75 | 13.25 |
| E | 0.55 | 0.75 |
| F | 3.1 | 3.5 |
| G | 1.25 | 1.45 |
| H | Typ 2.54 | |
| I | Typ 5.08 | |
| J | 4.55 | 4.75 |
| K | 2.4 | 2. 7 |
| L | 6.35 | 6.75 |
| M | 15.0 | 16.0 |
| N | 2.75 | 3.15 |
| O | 0.45 | 0.60 |
| All Dimensions in millimeter | | |

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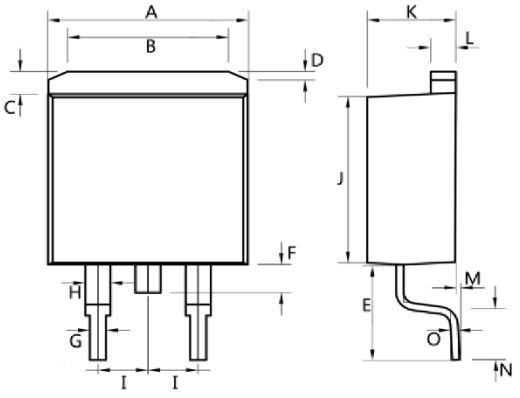


| Dim. | Min. | Max. |
|---|---|---|
| A | 10.0 | 10. 5 |
| B | 7.25 | 7.75 |
| C | 1.3 | 1.5 |
| D | 0.55 | 0.75 |
| E | 5.0 | 6.0 |
| F | 1.4 | 1.6 |
| G | 0.75 | 0.95 |
| H | 1.15 | 1.35 |
| I | Typ 2.54 | |
| J | 8.4 | 8.6 |
| K | 4.4 | 4.6 |
| L | 1.25 | 1.45 |
| M | 0.02 | 0.1 |
| N | 2.4 | 2.8 |
| O | 0.35 | 0.45 |
| All Dimensions in millimeter | | |

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## 500V N-Channel Enhancement Mode MOSFET

| Edition | Date | Change |
|---|---|---|
| Rve1.0 | 2020/1/31 | Initial release |