AP240N03NF

30V N-Channel Enhancement Mode MOSFET

Description

The AP240N03NF uses advanced **APM-SGT V** technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

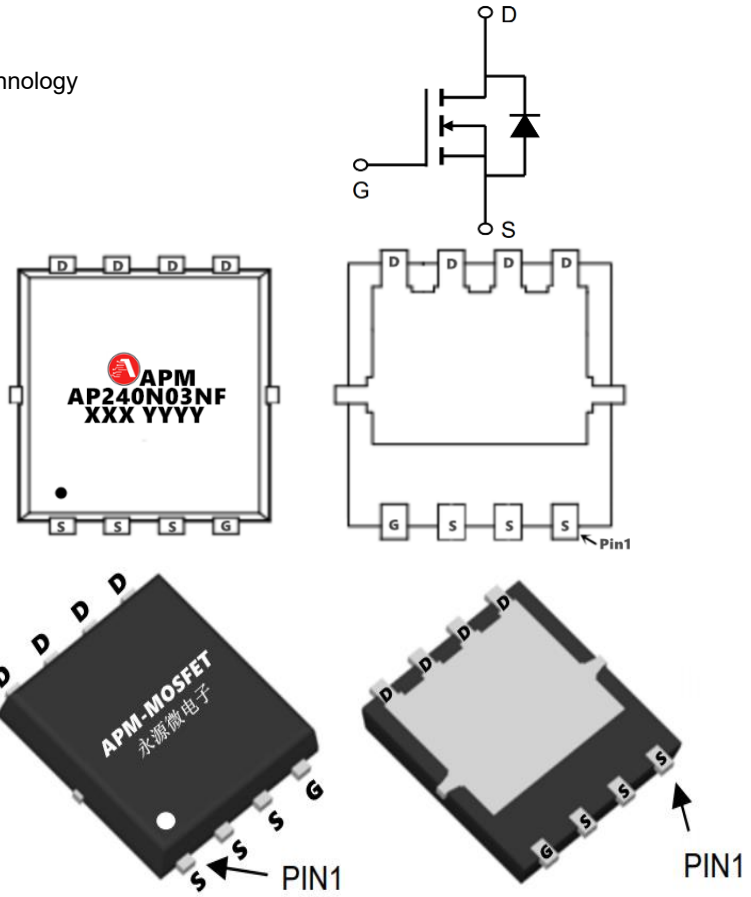
V_{DS} = 30V I_D =240A

$R_{DS(ON)}$ < 0.85mΩ @ V_{GS}=10V（**Type：0.65mΩ**）

Application

Buck

Boost



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP240N03NF	PDFN5*6-8L	AP240N03NF XXX YYYY	5000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Max.	Units
VDSS	Drain-Source Voltage	30	V
VGSS	Gate-Source Voltage	±20	V
ID@TC=25℃	Continuous Drain Current, VGS @ 10V1	240	A
ID@TC=100℃	Continuous Drain Current, VGS @ 10V1	207	A
IDM	Pulsed Drain Current	1312	A
EAS	Single Pulsed Avalanche Energy	845	mJ
IAS	Avalanche Current	125	A
PD@TC=25℃	Power Dissipation	160	W
T_J TSTG	Operating Junction Temperature Range	-55 to 150	°C
R_{θ}JA	Thermal Resistance Junction-Ambient [1]	25	°C/W
RθJC	Thermal Resistance, Junction to Case	0.78	℃/W

Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	30	-	-	V
IGSS	Gate-body Leakage Current	V_{DS} = 0V, V_{GS} = ±20V	-	-	±100	nA
IDSS	Zero Gate Voltage Drain Current T_J=25°C	V_{DS} = 30V, V_{GS} = 0V	-	-	1	μA
	Zero Gate Voltage Drain Current T_J=100°C		-	-	100	
VGS(th)	Gate-Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	1.2	1.6	2.5	V
RDS(on)	Drain-Source On-Resistance[4]	V_{GS} = 10V, I_D = 20A	-	0.65	0.85	mΩ
		V_{GS} = 4.5V, I_D =10A	-	0.90	1.2	
gfs	Forward Transconductance[4]	V_{DS} = 10V, I_D = 20A	-	110	-	S
Ciss	Input Capacitance	V_{DS} = 15V, V_{GS} =0V, f =1MHz	-	6790	-	pF
Coss	Output Capacitance		-	2450	-	
Crss	Reverse Transfer Capacitance		-	220	-	
R_g	Gate Resistance	f = 1MHz	-	2.2	-	Ω
Q_g	Total Gate Charge	V_{GS} = 10V, V_{DS} = 15V, I_D= 20A	-	109.3	-	nC
Qgs	Gate-Source Charge		-	20.8	-	
Qgd	Gate-Drain Charge		-	15.2	-	
td(on)	Turn-On Delay Time	V_{GS} =10V, V_{DD} = 15V, R_G = 3Ω, I_D= 20A	-	12	-	ns
t_r	Rise Time		-	12.3	-	
td(off)	Turn-Off Delay Time		-	88.4	-	
t_f	Fall Time		-	42.8	-	
trr	Body Diode Reverse Recovery Time	I_F=20A, dI/dt=100A/μs	-	72	-	ns
Q_{rr}	Body Diode Reverse Recovery Charge		-	36	-	nC
VSD	Diode Forward Voltage[4]	I_S = 20A, V_{GS} = 0V	-	-	1.2	V
IS	Continuous Source Current	T_C=25°C	-	-	240	A

Note :

1、The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、The EAS data shows Max. rating . The test condition is VDD =25V,VGS =10V,L=0.1mH,IAS =125A

4、The power dissipation is limited by 150℃ junction temperature

5、The data is theoretically the same as I D and I DM , in real applications , should be limited by total power dissipation.

Typical Characteristics

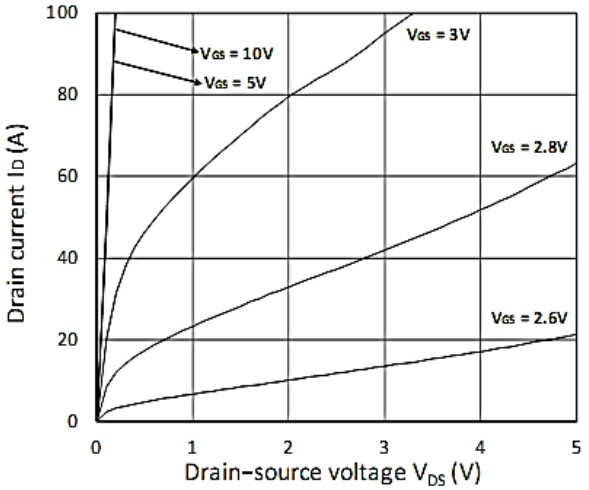


Figure 1. Output Characteristics

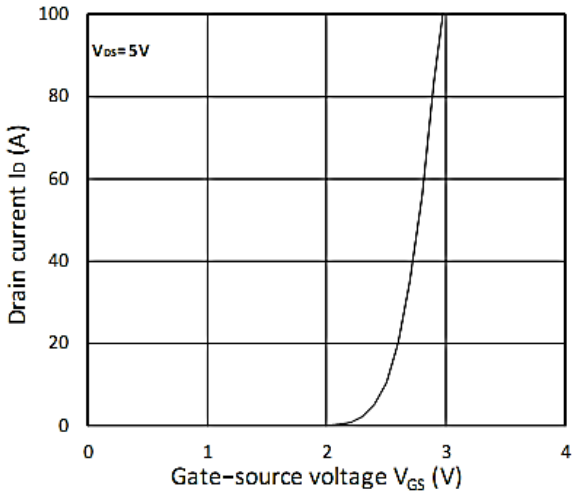


Figure 2. Transfer Characteristics

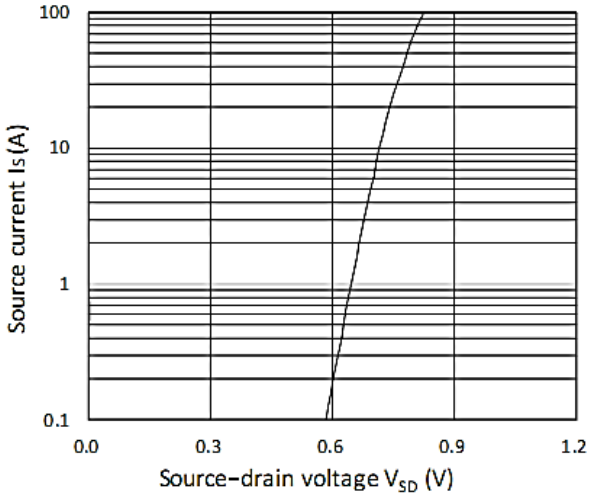


Figure 3. Forward Characteristics of Reverse

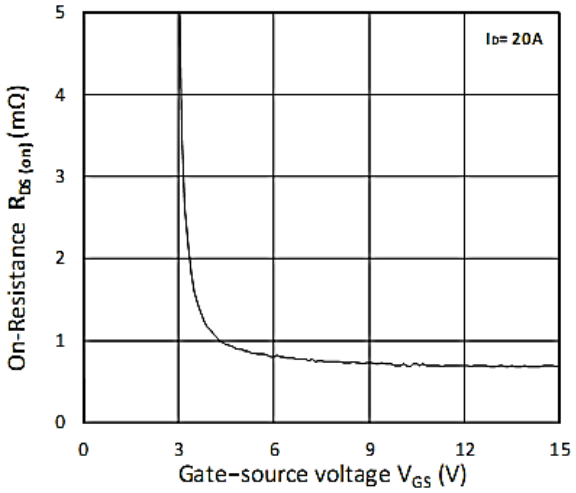


Figure 4. R DS(ON) vs. VGS

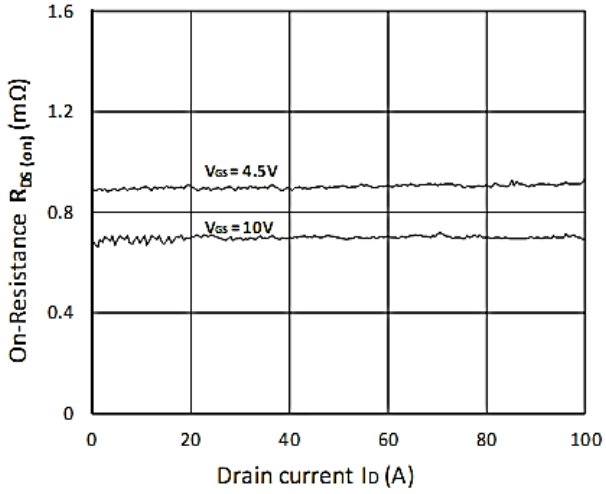


Figure 5. RDS(ON) vs. ID

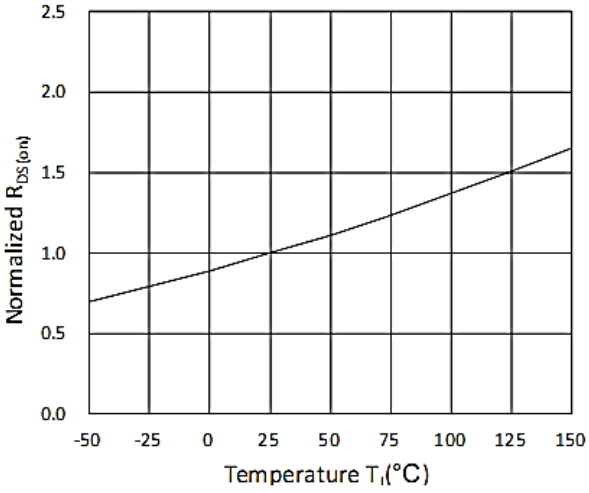


Figure 6. Normalized RDS(on) vs. Temperature

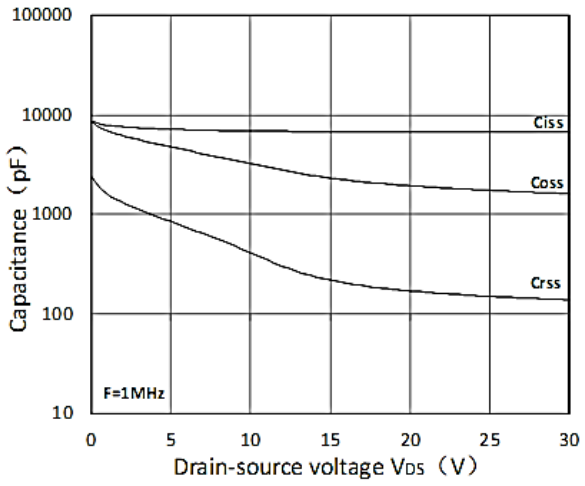


Figure 7. Capacitance Characteristics

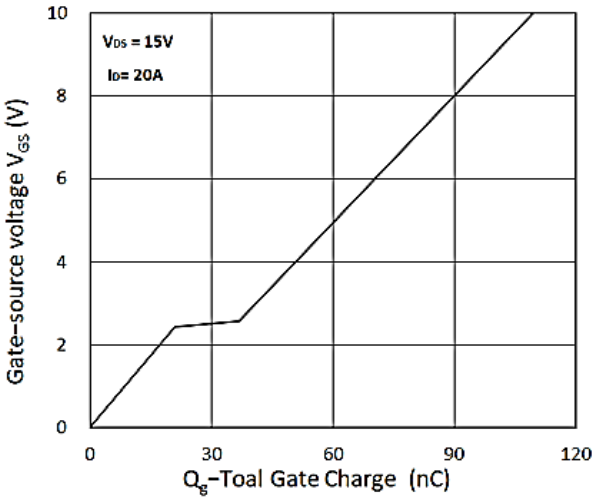


Figure 8. Gate Charge Characteristics

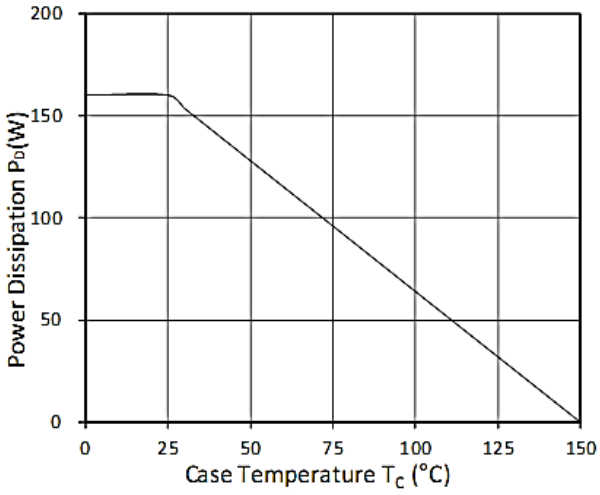


Figure 9. Power Dissipation

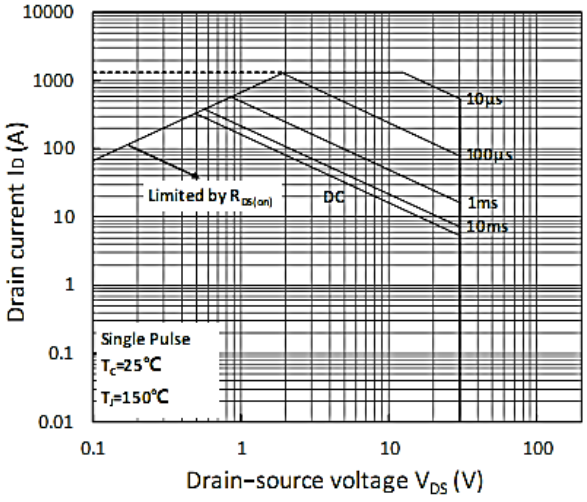


Figure10. Safe Operating Area

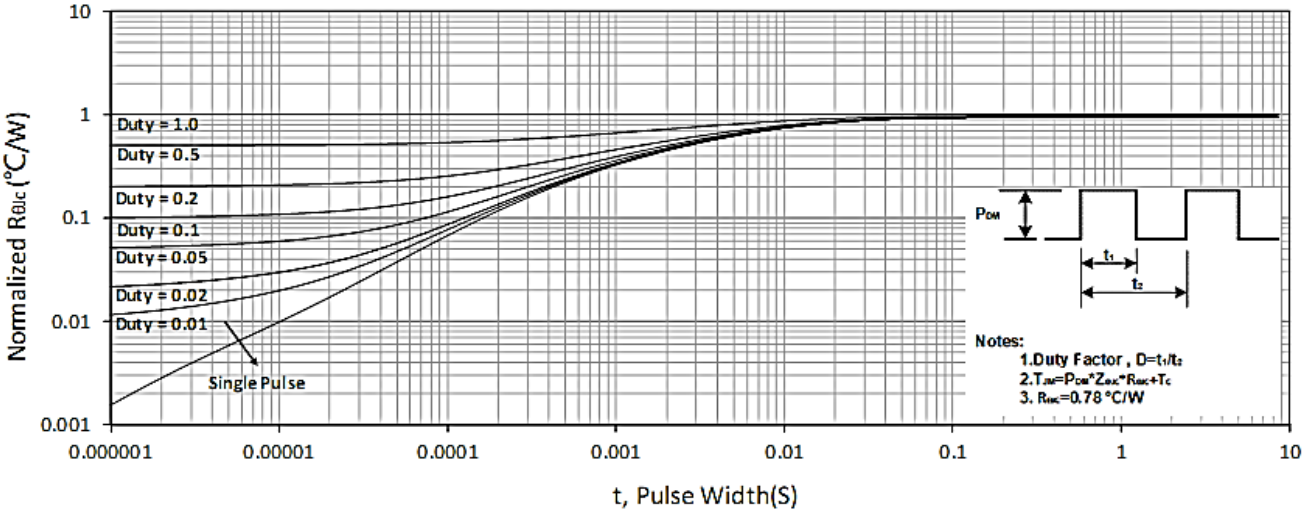
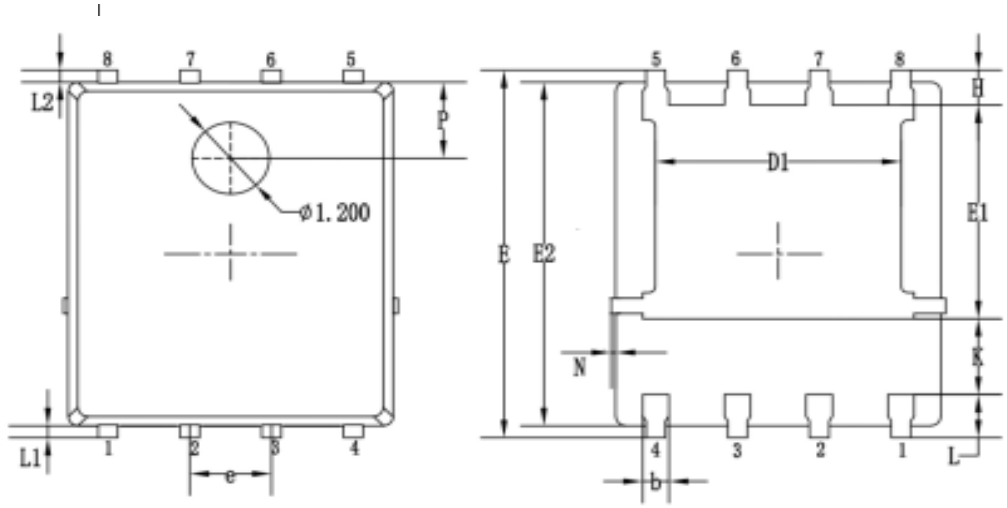
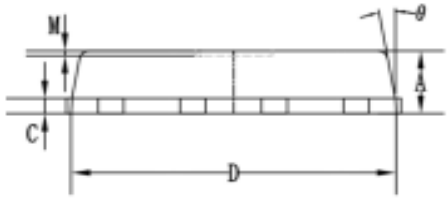


Figure 9 Normalized Maximum Transient Thermal Impedance

Package Mechanical Data-PDFN5*6-8L





Symbol	Dim in mm		
	min	typ	max
A	0.9	1.05	1.2
b	0.3	0.4	0.5
C	0.2	0.25	0.35
D	4.9	5.05	5.2
D1	3.72	3.82	4.12
E	5.9	6.1	6.3
E1	3.3	3.5	3.7
E2	5.6	5.75	5.9
e		1.27BSC	
H	0.48	0.58	0.7
K	1.14	1.27	1.4
L	0.54	0.74	0.84
L1/L2	0.1	0.2	0.3
θ	8°	10°	12°
M		0.08REF	
N	0		0.15
P		1.28REF	

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Edition	Date	Change
REV1.0	2023/3/31	Initial release