

20V N-Channel Enhancement Mode MOSFET

Description

The AP20N02DF uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = 20V$ $I_D = 20A$

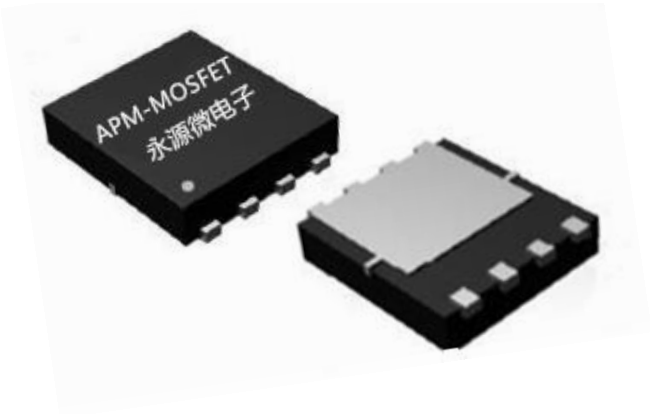
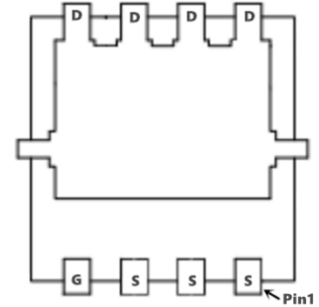
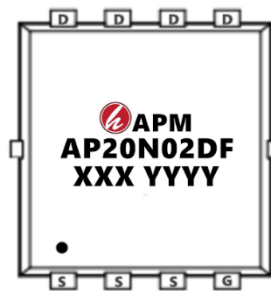
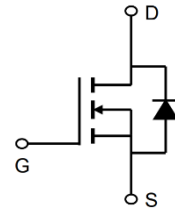
$R_{DS(ON)} < 8.0m\Omega$ @ $V_{GS}=10V$

Application

Battery protection

Load switch

Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP20N02DF	PDFN3*3-8L	AP20N02DF XXX YYYY	5000

Absolute Maximum Ratings (TC=25 °C unless otherwise noted)

Symbol	Parameter	Max.	Units
V_{DSS}	Drain-Source Voltage	20	V
V_{GSS}	Gate-Source Voltage	± 12	V
I_D	Continuous Drain Current $T_C = 25^\circ C$	20	A
I_D	Continuous Drain Current $T_C = 100^\circ C$	15	A
I_{DM}	Pulsed Drain Current ^{note1}	60	A
E_{AS}	Single Pulsed Avalanche Energy ^{note2}	36	mJ
P_D	Power Dissipation $T_C = 25^\circ C$	31	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	4.84	$^\circ C/W$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ C$

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Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	20	22	-	V
IDSS	Zero Gate Voltage Drain Current	V _{DS} =20V, V _{GS} =0V,	-	-	1.0	μA
IGSS	Gate to Body Leakage Current	V _{DS} =0V, V _{GS} =±12V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	0.4	0.7	1.1	V
RDS(on)	Static Drain-Source on-Resistance note3	V _{GS} =4.5V, I _D =25A	-	6.1	8.0	mΩ
		V _{GS} =2.5V, I _D =10A	-	8.8	13	
Ciss	Input Capacitance	V _{DS} =10V, V _{GS} =0V, f=1.0MHz	-	1458	-	pF
Coss	Output Capacitance		-	238	-	pF
Crss	Reverse Transfer Capacitance		-	212	-	pF
Qg	Total Gate Charge	V _{DS} =10V, I _D =25A, V _{GS} =4.5V	-	19	-	nC
Qgs	Gate-Source Charge		-	3	-	nC
Qgd	Gate-Drain("Miller") Charge		-	6.4	-	nC
td(on)	Turn-on Delay Time	V _{DS} =10V, I _D =10A, R _{GEN} =3Ω, V _{GS} =4.5V	-	10	-	ns
t _r	Turn-on Rise Time		-	21	-	ns
td(off)	Turn-off Delay Time		-	39	-	ns
t _f	Turn-off Fall Time		-	19	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	50	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	200	A
VSD	Drain to Source Diode Forward Voltage	V _{GS} =0V, I _S =30A	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	IF=20A, dI/dt=100A/μs	-	25	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	20	-	nC

Note :

- 1、The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width .The EAS data shows Max. rating .
- 3、The EAS condition: T_J=25°C, V_{DD}=16V, V_G=10V, R_G=0.6Ω, L=0.5mH, I_{AS}=33A
- 4、The power dissipation is limited by 175°C junction temperature
- 5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

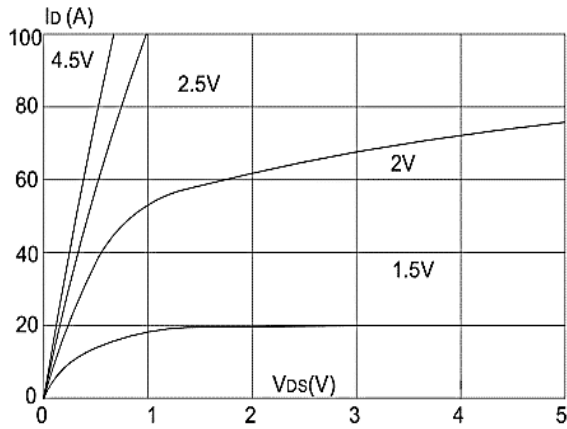


Figure1: Output Characteristics

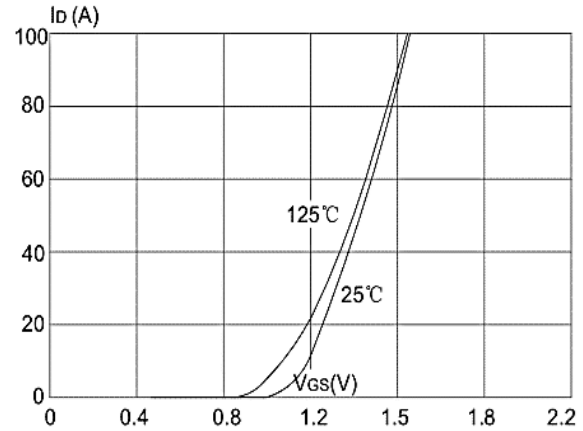


Figure 2: Typical Transfer Characteristics

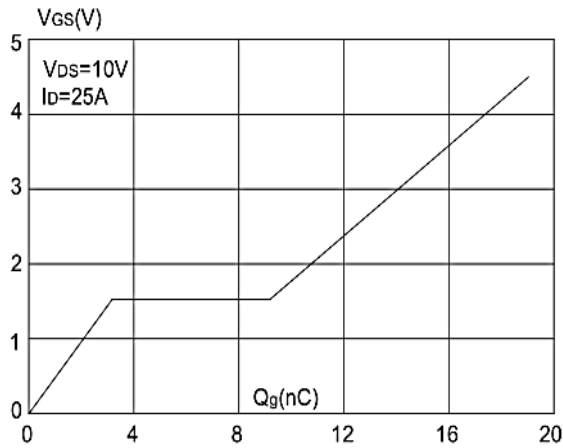


Figure 3: On-resistance vs. Drain Current

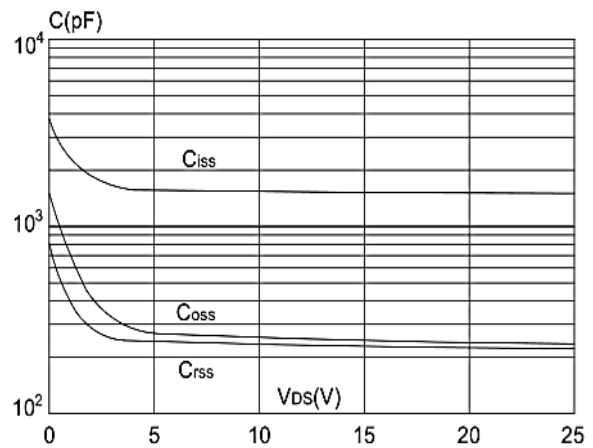


Figure 4: Body Diode Characteristics

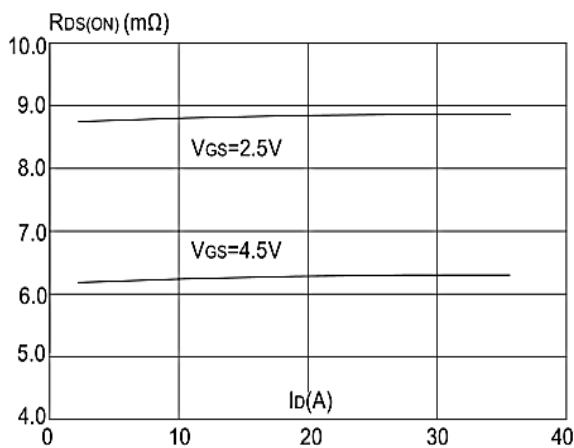


Figure 5: Gate Charge Characteristics

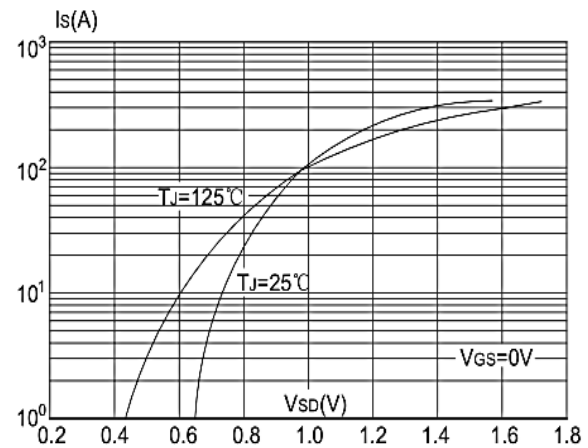


Figure 6: Capacitance Characteristics

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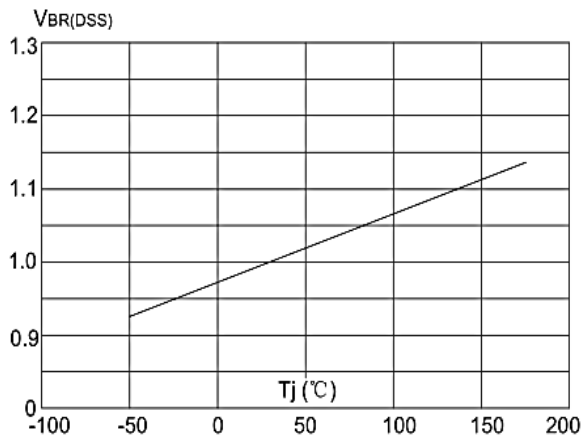


Figure 7: Normalized Breakdown Voltage vs Junction Temperature

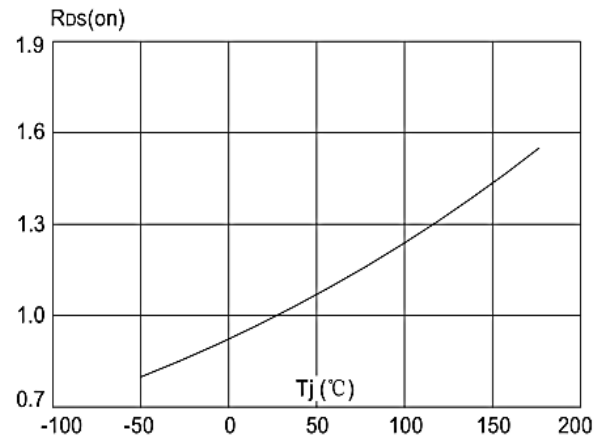


Figure 8: Normalized on Resistance vs. Junction Temperature

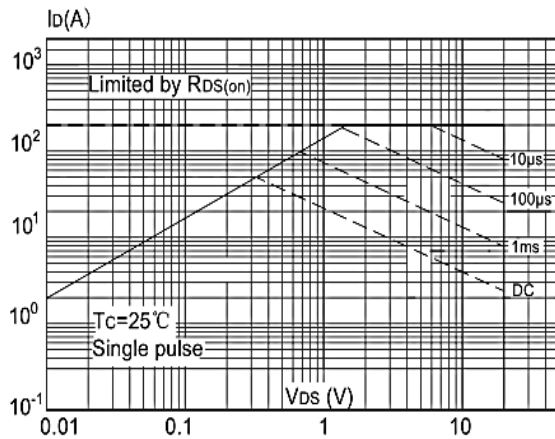


Figure 9: Maximum Safe Operating Area

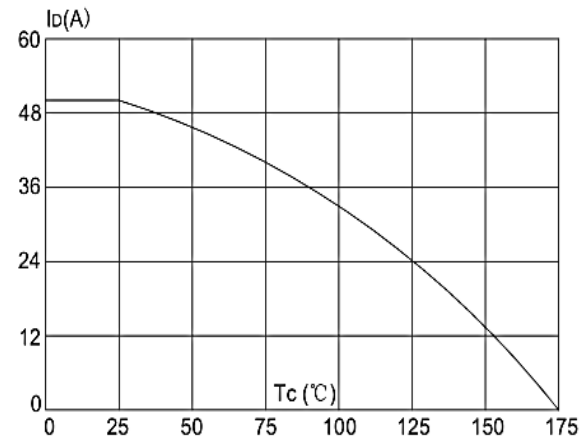


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

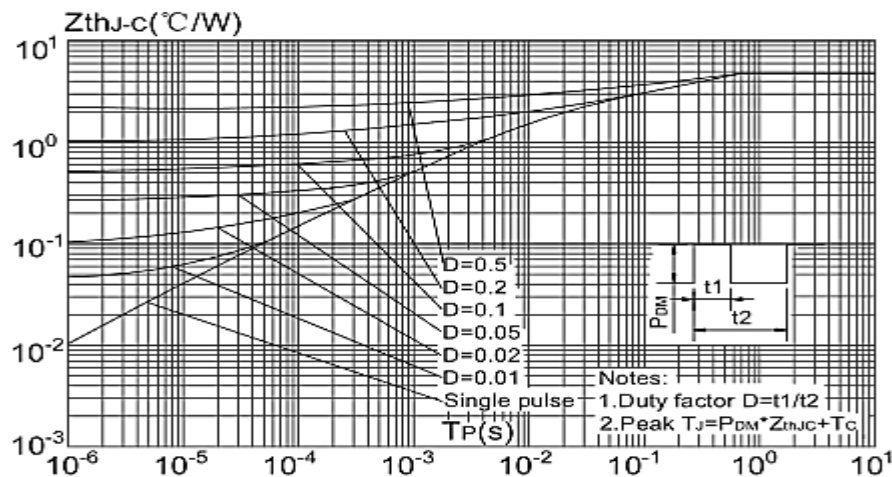
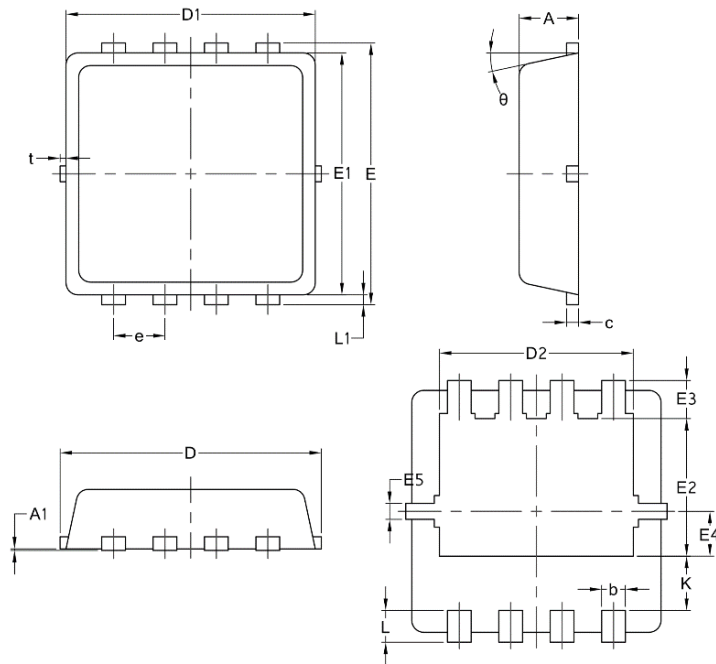


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambien

Package Mechanical Data-DFN3*3-8L-JQ Single



Symbol	Common		
	mm		
	Mim	Nom	Max
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
Φ	10	12	14

20V N-Channel Enhancement Mode MOSFET**Attention**

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Edition	Date	Change
Rve1.0	2020/9/11	Initial release

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