

20V N+P-Channel Enhancement Mode MOSFET

Description

The AP20G02DF uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = 20V$ $I_D = 25A$

$R_{DS(ON)} < 10m\Omega$ @ $V_{GS}=4.5V$ (Type: 8.0m Ω)

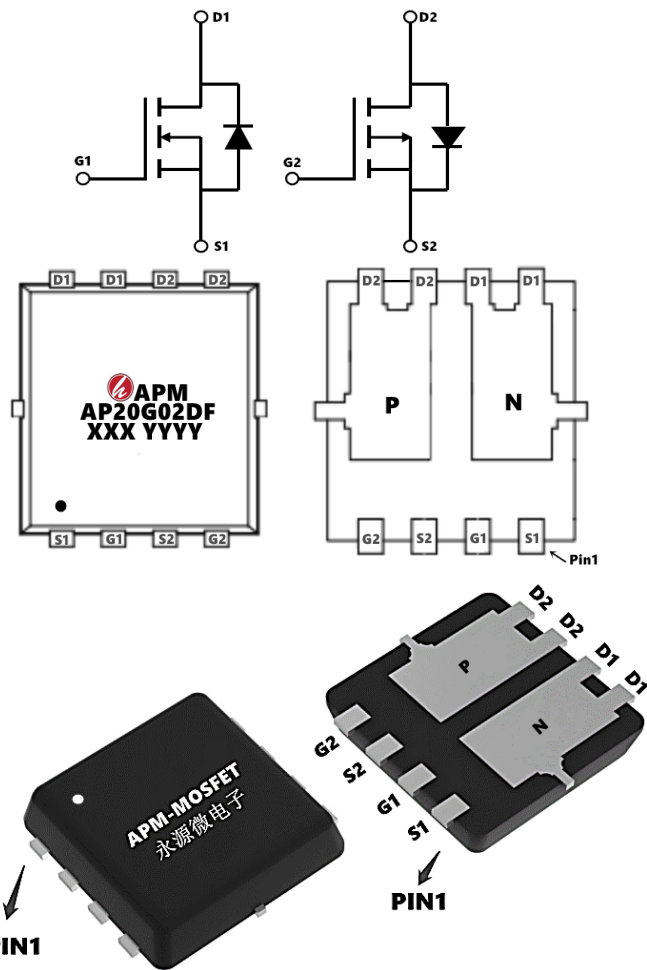
$V_{DS} = -20V$ $I_D = -20A$

$R_{DS(ON)} < 20m\Omega$ @ $V_{GS}=-4.5V$ (Type: 16m Ω)

Application

Wireless charging

Brushless motor



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP20G02DF	PDFN3*3-8L	AP20G02DF XXX YYYY	5000

Absolute Maximum Ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	N-Ch	P-Ch	Units
V_{DS}	Drain-Source Voltage	30	-30	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
$I_D@T_C=25^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V^1$	25	-20	A
$I_D@T_C=100^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V^1$	17.4	-15.5	A
I_{DM}	Pulsed Drain Current ²	78	-69.1	A
EAS	Single Pulse Avalanche Energy ³	150	135	mJ
I_{AS}	Avalanche Current	72	68	A
$P_D@T_C=25^{\circ}C$	Total Power Dissipation ⁴	46	41.3	W
T_{STG}	Storage Temperature Range	-55 to 150	-55 to 150	$^{\circ}C$
T_J	Operating Junction Temperature Range	-55 to 150	-55 to 150	$^{\circ}C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	25		$^{\circ}C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	5		$^{\circ}C/W$

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Electrical Characteristics (T_c=25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	20	23	-	V
IDSS	Zero Gate Voltage Drain Current	V _{DS} =20V, V _{GS} =0V,	-	-	1.0	μA
IGSS	Gate to Body Leakage Current	V _{DS} =0V, V _{GS} =±12V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	0.58	0.65	1.2	V
RDS(on)	Static Drain-Source on-Resistance note3	V _{GS} =4.5V, I _D =25A	-	8	10	mΩ
		V _{GS} =2.5V, I _D =10A	-	10	13	
C _{iss}	Input Capacitance	V _{DS} =10V, V _{GS} =0V, f=1.0MHz	-	1458	-	pF
C _{oss}	Output Capacitance		-	238	-	pF
C _{rss}	Reverse Transfer Capacitance		-	212	-	pF
Q _g	Total Gate Charge	V _{DS} =10V, I _D =25A, V _{GS} =4.5V	-	19	-	nC
Q _{gs}	Gate-Source Charge		-	3	-	nC
Q _{gd}	Gate-Drain("Miller") Charge		-	6.4	-	nC
td(on)	Turn-on Delay Time	V _{DS} =10V, I _D =10A, R _{GEN} =3Ω, V _{GS} =4.5V	-	10	-	ns
t _r	Turn-on Rise Time		-	21	-	ns
td(off)	Turn-off Delay Time		-	39	-	ns
t _f	Turn-off Fall Time		-	19	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	50	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	200	A
VSD	Drain to Source Diode Forward Voltage	V _{GS} =0V, I _S =30A	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	IF=20A, dI/dt=100A/μs	-	25	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	20	-	nC

Note :

- 1、The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3、The EAS data shows Max. rating . The test condition is V_{DD}=16V, V_{GS}=10V, L=0.1mH, I_{AS}=21A
- 4、The power dissipation is limited by 150°C junction temperature
- 5、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

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Electrical Characteristics ($T_c=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-20	-22	-	V
IDSS	Zero Gate Voltage Drain Current	$V_{DS}=-20V, V_{GS}=0V,$	-	-	-1	μA
IGSS	Gate to Body Leakage Current	$V_{DS}=0V, V_{GS}=\pm 12V$	-	-	± 100	nA
VGS(th)	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.58	-0.7	-1.2	V
RDS(on)	Static Drain-Source on-Resistance note2	$V_{GS}=-4.5V, I_D=-10A$	-	16.8	20	m Ω
		$V_{GS}=-2.5V, I_D=-5A$	-	21.5	25	
Ciss	Input Capacitance	$V_{DS}=-10V, V_{GS}=0V,$ $f=1.0MHz$	-	2000	-	pF
Coss	Output Capacitance		-	242	-	pF
Crss	Reverse Transfer Capacitance		-	231	-	pF
Qg	Total Gate Charge	$V_{DS}=-10V, I_D=-6A,$ $V_{GS}=-4.5V$	-	15.3	-	nC
Qgs	Gate-Source Charge		-	2.2	-	nC
Qgd	Gate-Drain("Miller") Charge		-	4.4	-	nC
td(on)	Turn-on Delay Time	$V_{DD}=-10V, I_D=-12A,$ $V_{GS}=-4.5V,$ $R_{GEN}=2.5\Omega$	-	10	-	ns
tr	Turn-on Rise Time		-	31	-	ns
td(off)	Turn-off Delay Time		-	28	-	ns
tf	Turn-off Fall Time		-	8	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	-12	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-48	A
VSD	Drain to Source Diode Forward Voltage	$V_{GS}=0V, I_S=-12A$	-	-0.8	-1.2	V

Note :

- 1、The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
- 2、The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3、The EAS data shows Max. rating . The test condition is $V_{DD}=-16V, V_{GS}=-10V, L=0.1mH, I_{AS}=-21A$
- 4、The power dissipation is limited by 150 $^{\circ}\text{C}$ junction temperature
- 5、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

N-Typical Characteristics

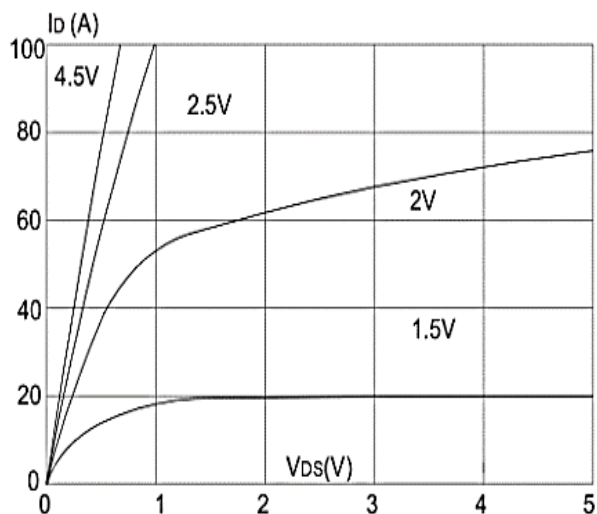


Figure1: Output Characteristics

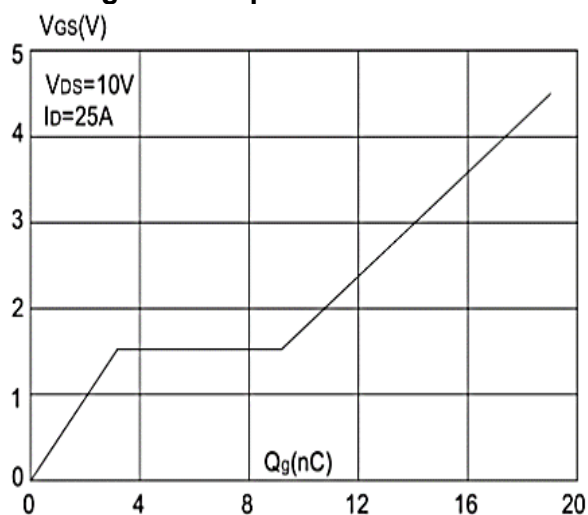


Figure 3: On-resistance vs. Drain Current

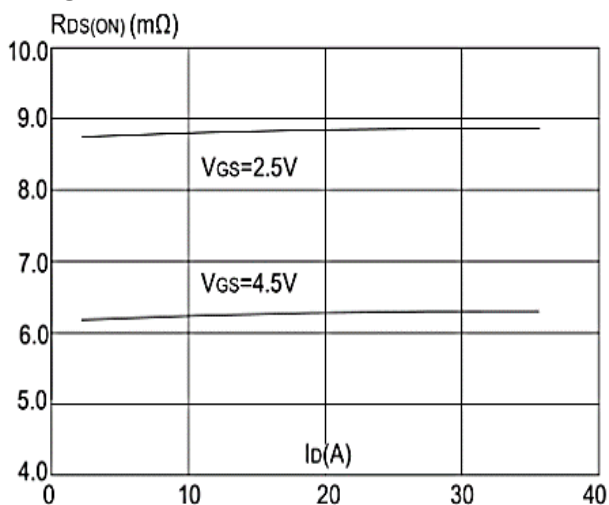


Figure 5: Gate Charge Characteristics

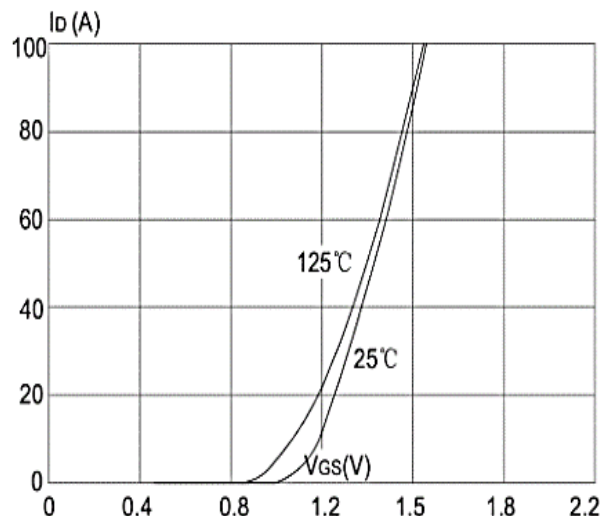


Figure 2: Typical Transfer Characteristics

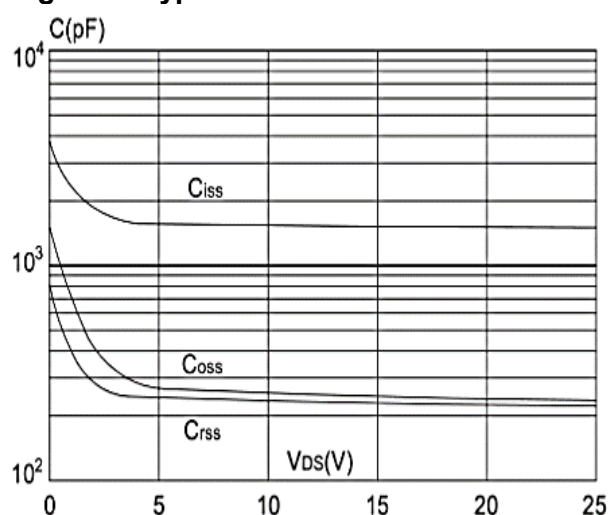


Figure 4: Body Diode Characteristics

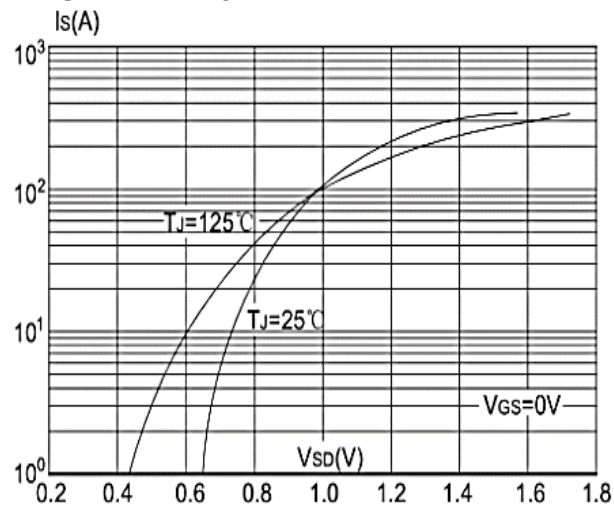


Figure 6: Capacitance Characteristics

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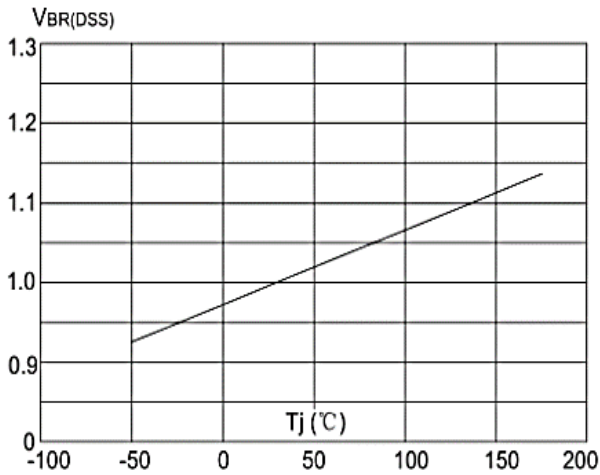


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

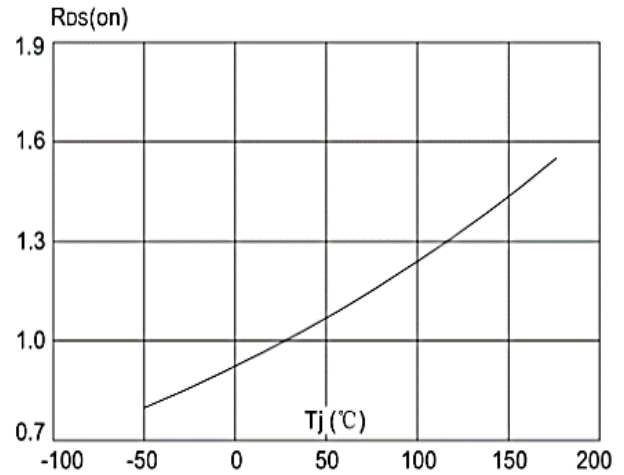


Figure 8: Normalized on Resistance vs. Junction Temperature

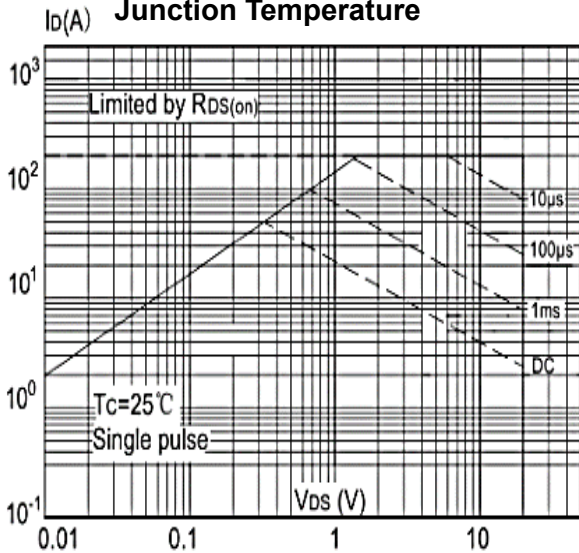


Figure 9: Maximum Safe Operating Area

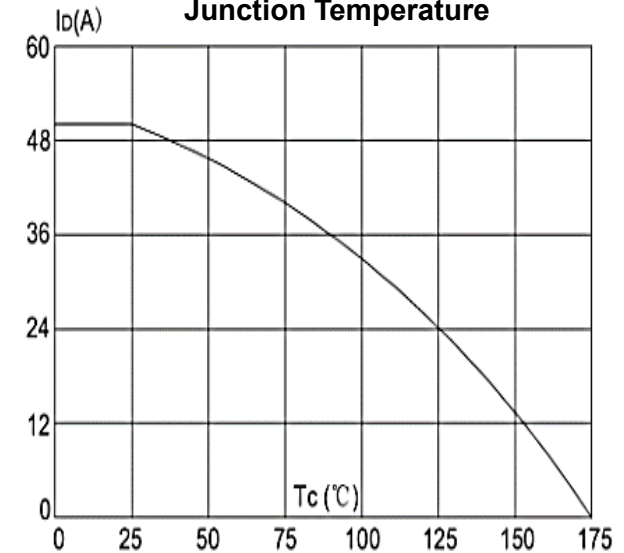


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

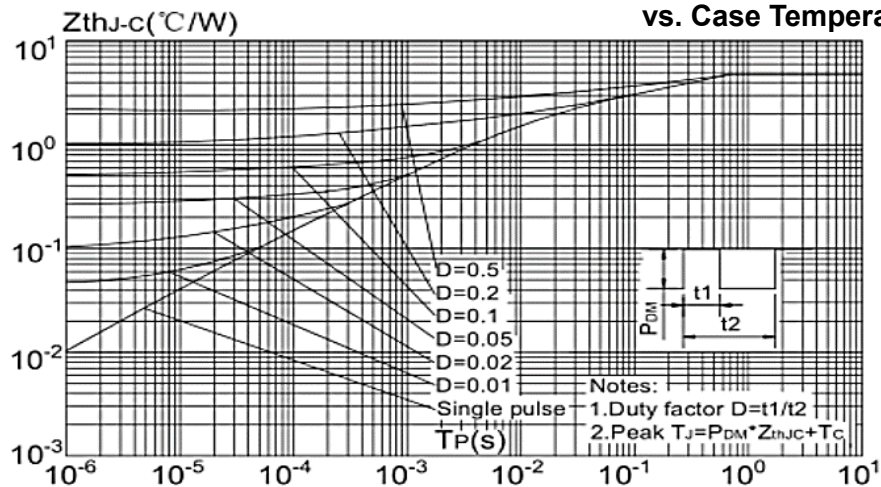


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

P-Typical Characteristics

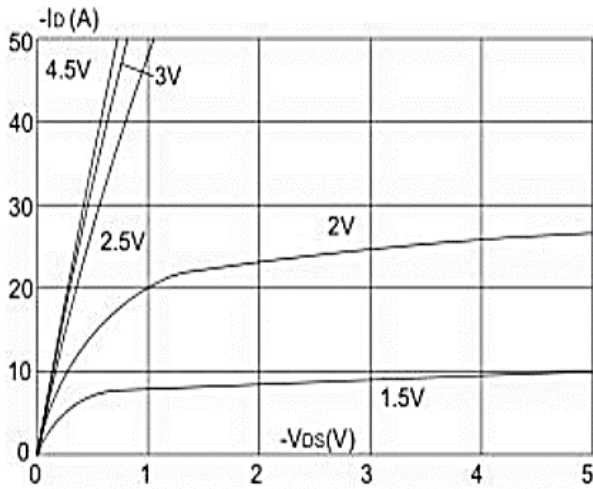


Figure1: Output Characteristics

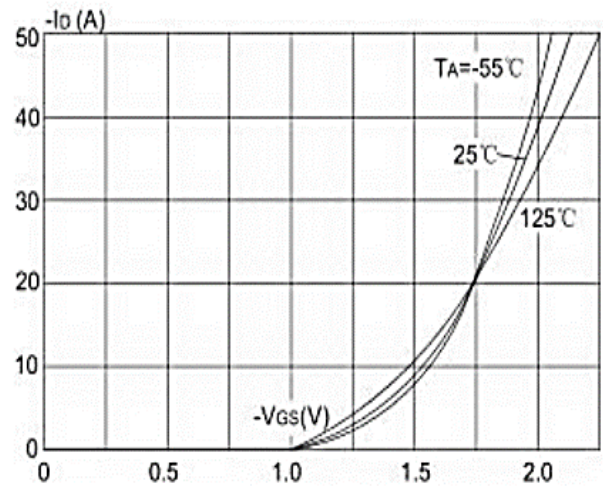


Figure 2: Typical Transfer Characteristics

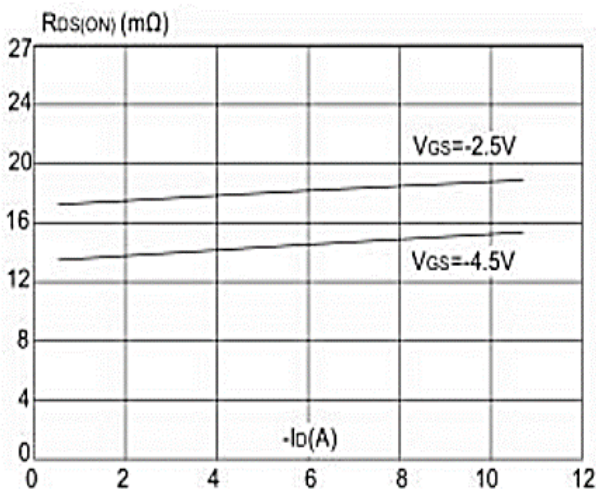


Figure 3: On-resistance vs. Drain Current

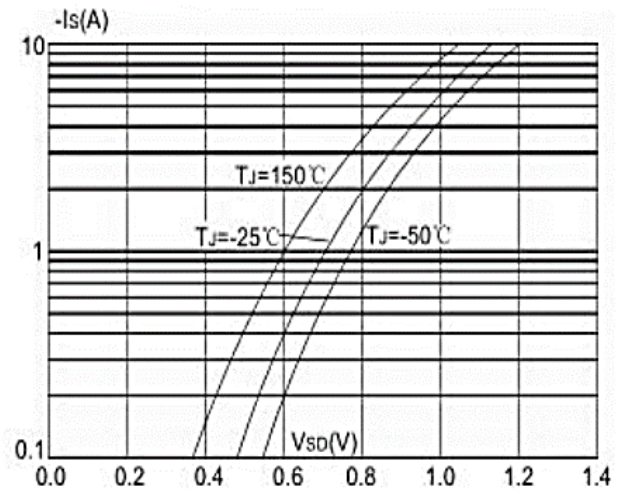


Figure 4: Body Diode Characteristics

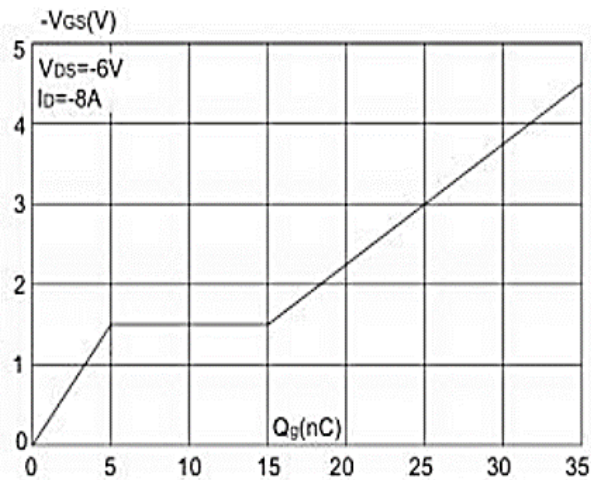


Figure 5: Gate Charge Characteristics

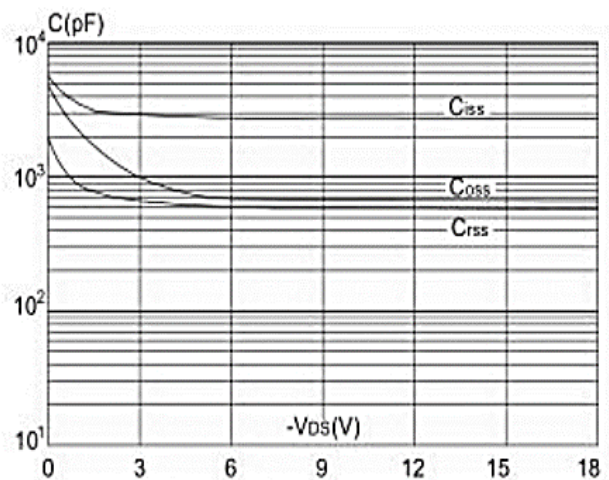


Figure 6: Capacitance Characteristics

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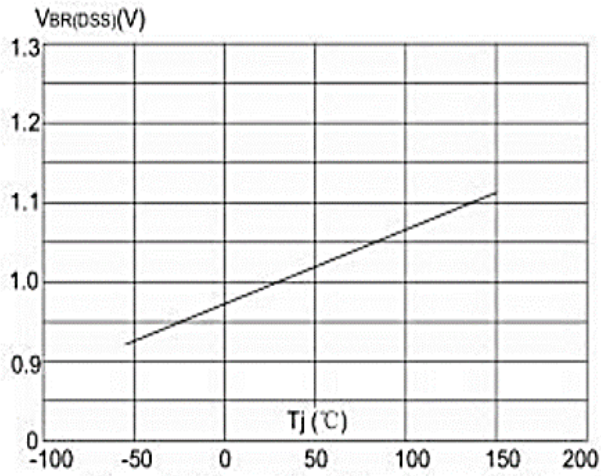


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

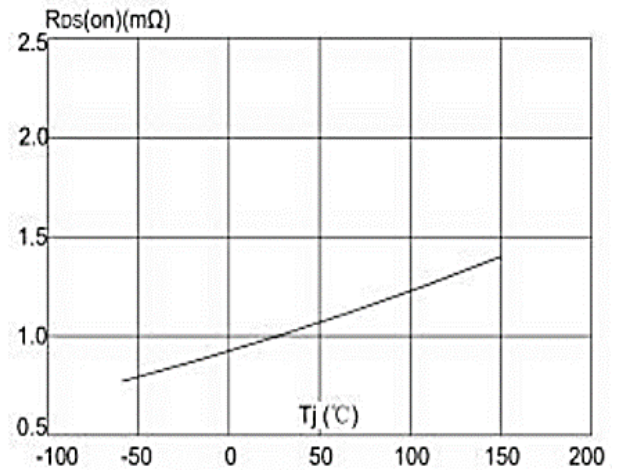


Figure 8: Normalized on Resistance vs. Junction Temperature

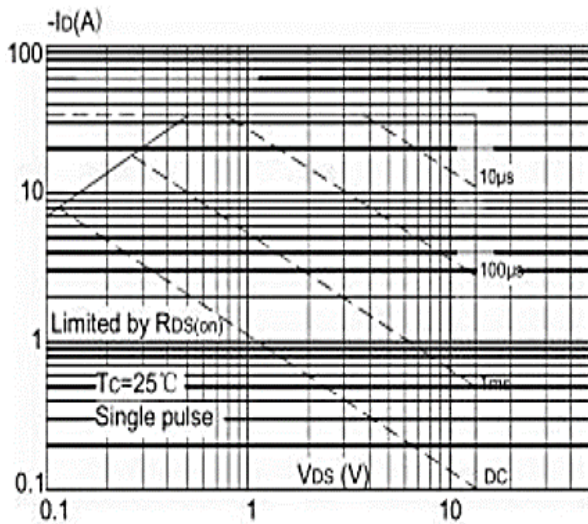


Figure 9: Maximum Safe Operating Area

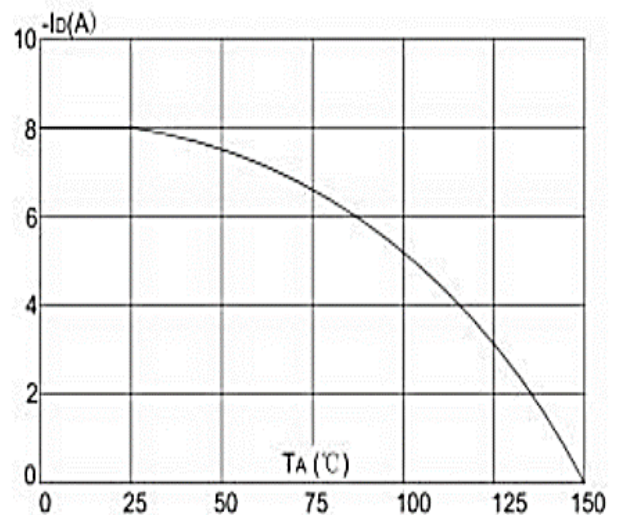


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

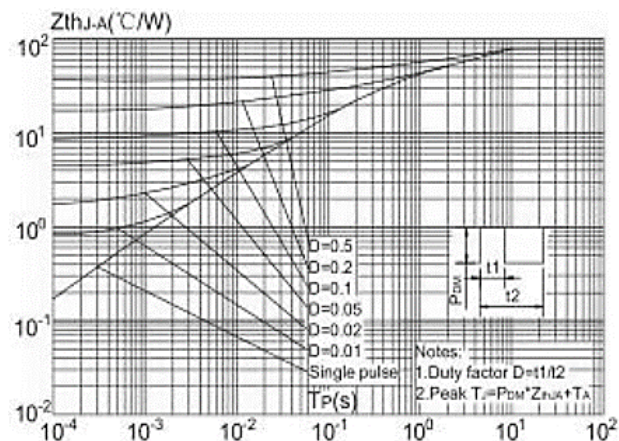
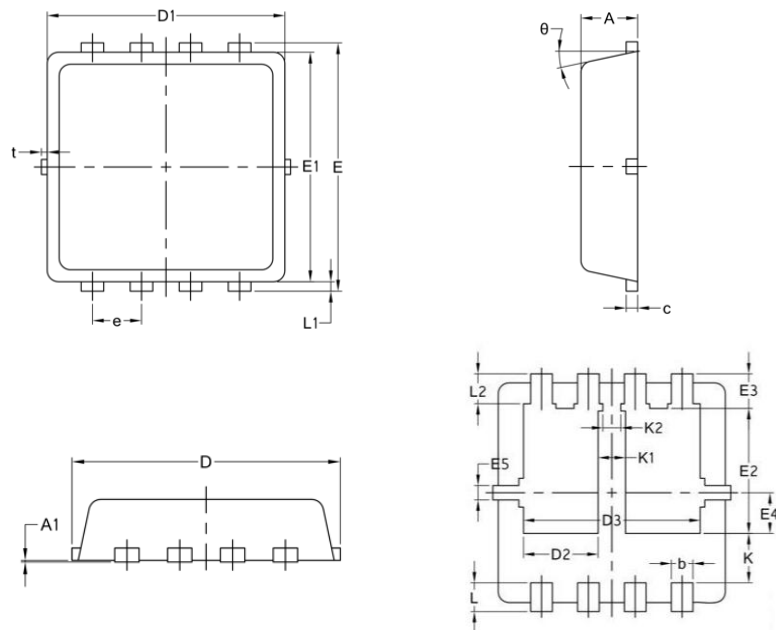


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

Package Mechanical Data-PDFN3*3-8L Double



Symbol	Common		
	Mm		
	Min	Nom	Max
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.25	0.30	0.39
c	0.14	0.152	0.20
D	3.20	3.30	3.45
D1	3.05	3.15	3.25
D2	0.84	1.04	1.24
D3	2.30	2.45	2.60
E	3.20	3.30	3.40
E1	2.95	3.05	3.15
E2	1.60	1.74	1.90
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.50	0.69	0.80
K1	0.30	0.38	0.53
K2	0.15	0.25	0.35
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
L2	0.27	0.42	0.57
t	0	0.075	0.13
Φ	10°	12°	14°

20V N+P-Channel Enhancement Mode MOSFET**Attention**

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Edition	Date	Change
REV1.0	2021/2/30	Initial release

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