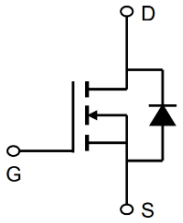
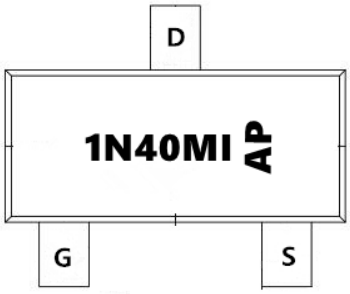
AP1N40MI

400V N-Channel Enhancement Mode MOSFET

Description

The AP1N40MI is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.





Top View

General Features

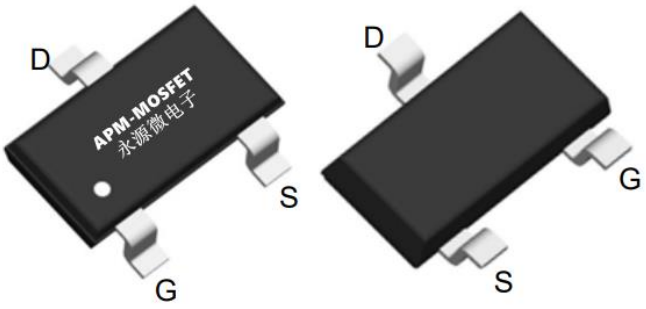
V_{DS} = 400V I_D =1A

$R_{DS(ON)}$ < 8500mΩ @ V_{GS}=10V （**Type：7200mΩ**）

Application

LED

Bottom View



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP1N40MI	SOT23-3L	1N40M-AP	3000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Value	Unit
VDSS	Drain-Source Voltage (V_{GS} = 0V)	400	V
ID	Continuous Drain Current	1	A
IDM	Pulsed Drain Current (note1)	4	A
VGS	Gate-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy (note2)	15	mJ
P_D	Power Dissipation (T_C = 25ºC)	33.2	W
TJ, Tstg	Operating Junction and Storage Temperature Range	-55~+150	ºC
RthJC	Thermal Resistance, Junction-to-Case	5	ºC/W
RthJA	Thermal Resistance, Junction-to-Ambient	125	ºC/W

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Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	400	450		V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage TemperatureCoefficient	I_D=250μA,Referenced to 25°C		0.43		V/°C
IDSS	Zero Gate Voltage Drain Current	V_{DS} =400 V, V_{GS} = 0 V			1	μA
		V_{DS} = 320V, TC = 125°C			10	μA
IGSSF	Gate-Body Leakage Current, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
IGSSR	Gate-Body Leakage Current, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
VGS(TH)	Gate Threshold voltage	V_{DS}=V_{GS}, I_D =250 uA	1.2	1.8	2.5	V
RDS(On)	Drain-Source on-state resistance	V_{GS}=10V, I_D = 0.5A, T_J=25°C		7200	8500	mΩ
C_{iss}	Input capacitance	V_{DS}= 25V, V_{GS}=0V, f=1.0MHz		83		pF
C_{oss}	Output capacitance			8.9		pF
C_{rss}	Reverse transfer capacitance			1		pF
td(on)	Turn On Delay Time	V_{DD}=320 V, ID=1A, R_G=25Ω		29		ns
t_r	Rising Time			6		ns
td(off)	Turn Off Delay Time			42		ns
t_f	Fall Time			31		ns
Q_g	Total Gate Charge	V_{DD}=320 V, ID=1A,		9.6		nC
Q_{gs}	Gate-Source Charge			3.0		nC
Q_{gd}	Gate-Drain Charge			2.5		nC
ISM	Maximum Pulsed Drain-Source Diode Forward Current				1	A
V_{SD}	Diode Forward Voltage	V_{GS}=0V, I_S =0.5A			1.4	V
trr	Reverse Recovery Time	V_{GS}=0V, I_S = 1 A, dI_F / dt = 100 A/μs		180		ns
Q_{rr}	Reverse Recovery Charge			0.28		μC

Note :

1、The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.

2、The test condition is Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%

3、The power dissipation is limited by 150℃ junction temperature

4、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

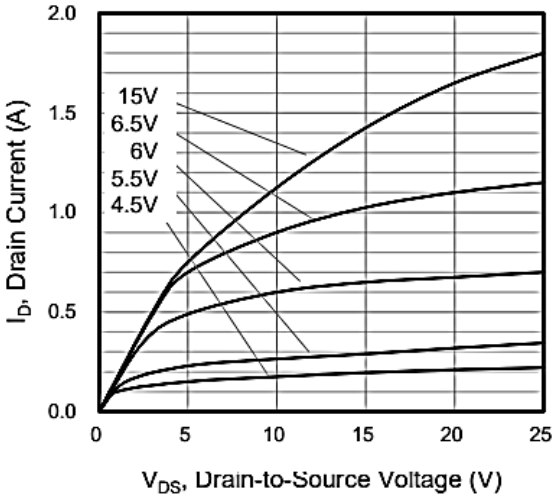


Figure 1. Output Characteristics

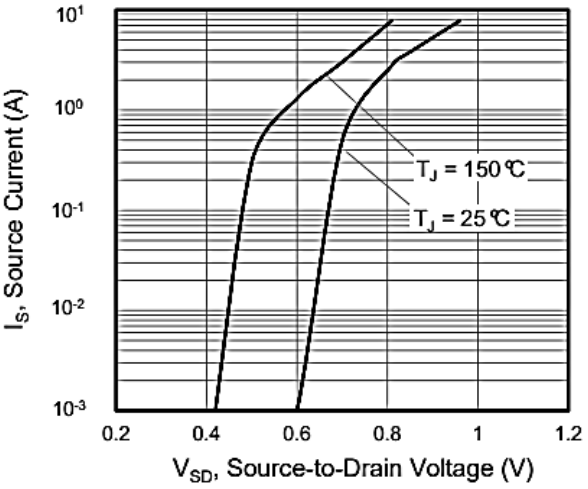


Figure 2. Body Diode Forward Voltage

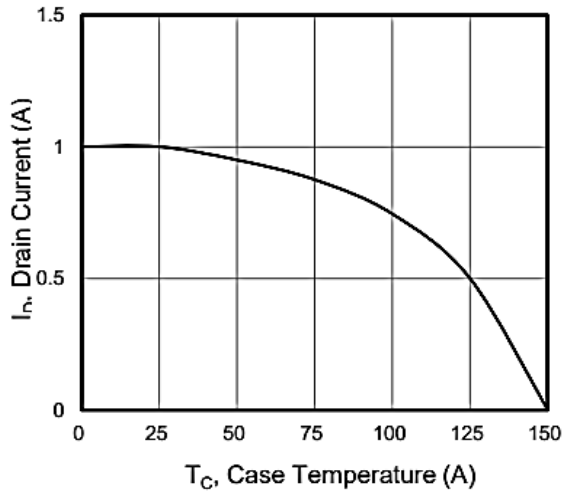


Figure3.DrainCurrentvs.Temperature

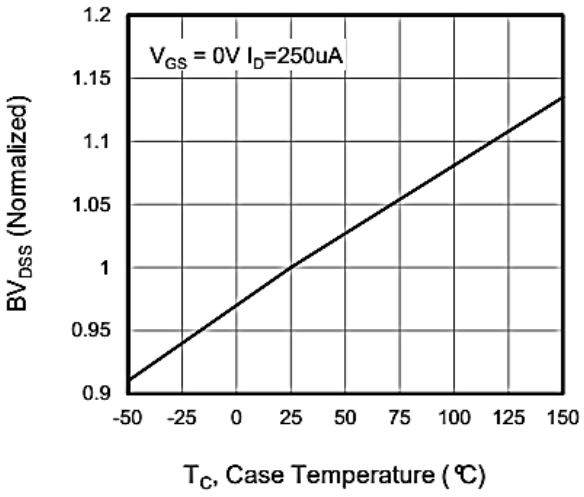


Figure4.BVDSSVariationvs.Temperature

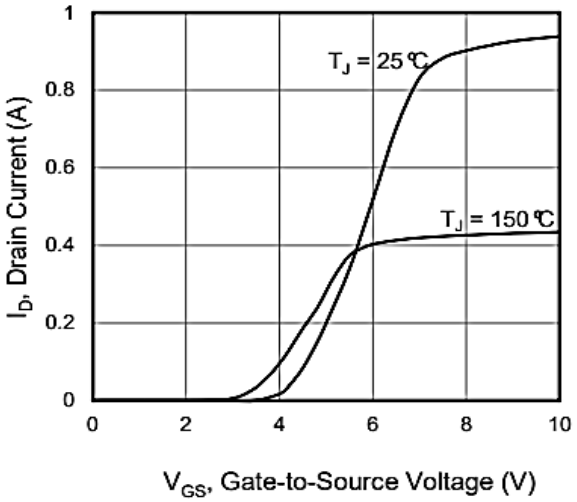


Figure 5. Transfer Characteristics

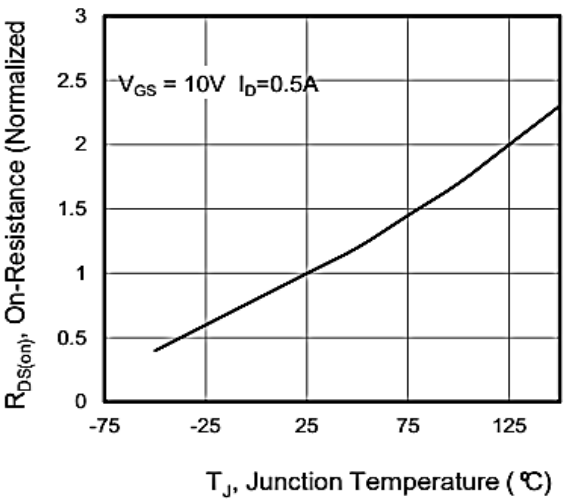


Figure 6. On-Resistance vs. Temperature

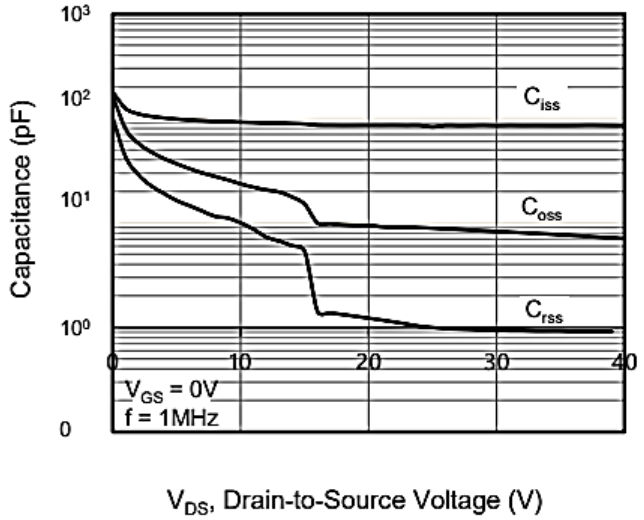


Figure 7. Capacitance

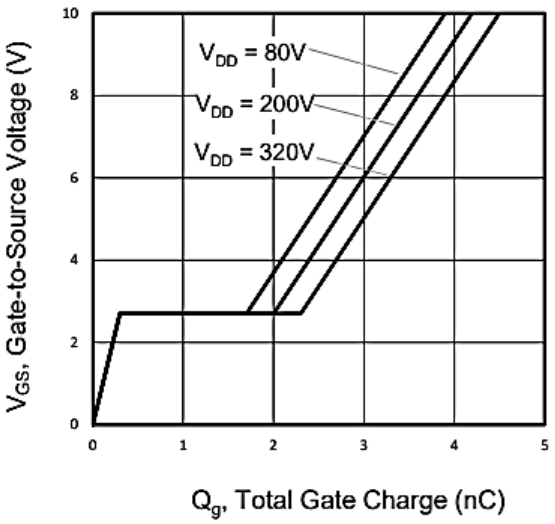


Figure 8.Gate Charge

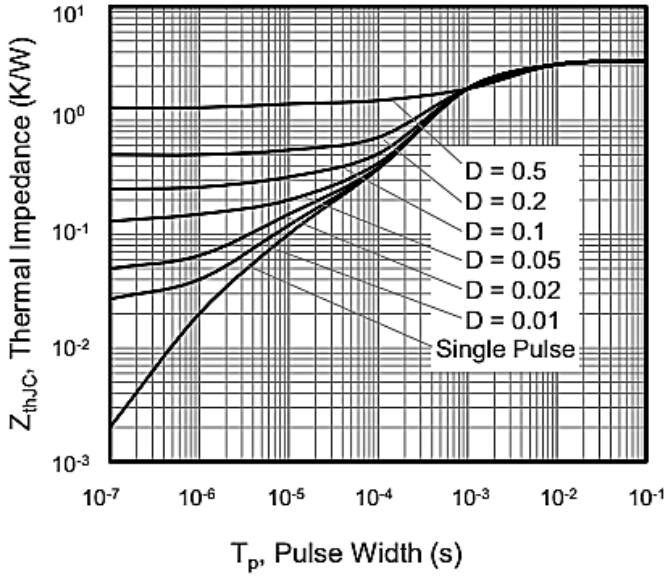
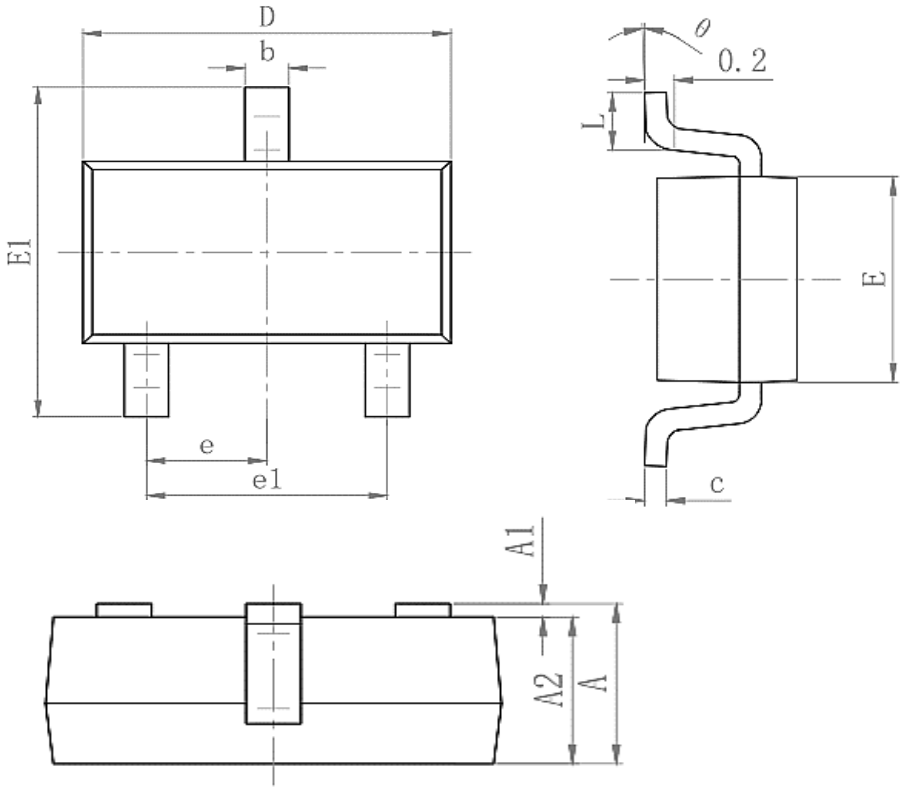


Figure 9. Transient Thermal Impedance

Package Mechanical Data-SOT23-3-XC-Single



Symbol	Dimensions In Millimeters	
	Min.	Max.
A	1.050	1.250
A1	0.000	0.100
A2	1.050	1.150
b	0.25	0.45
c	0.100	0.200
D	2.820	3.020
E	1.5	1.7
E1	2.650	2.950
e	0.950(BSC)	
e1	1.800	2.000
L	0.300	0.500
θ	0°	8°

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Edition	Date	Change
Rve1.0	2020/1/31	Initial release