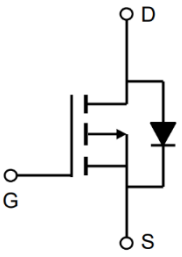
AP18P02BF

-20V P-Channel Enhancement Mode MOSFET

Description

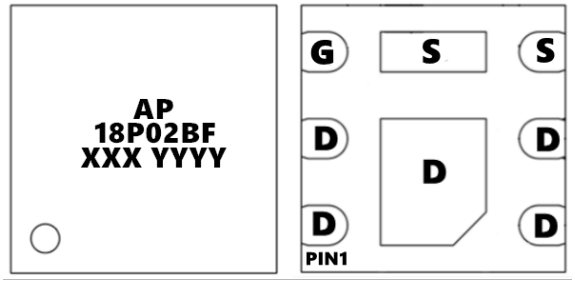
The AP18P02BF uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



General Features

V_{DS} = -20V I_D =-18A

$R_{DS(ON)}$ < 22mΩ @ V_{GS}=-4.5V **(Type：18mΩ)**

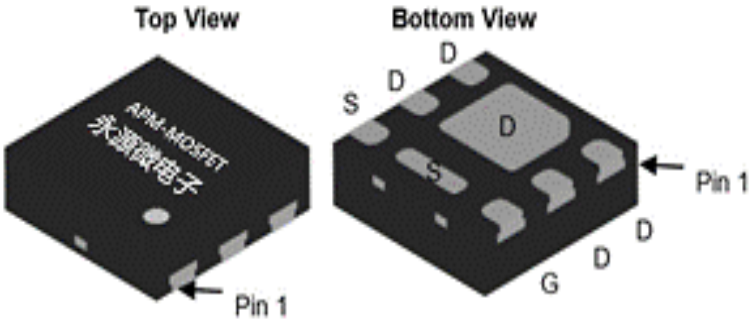


Application

Battery protection

Load switch

Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP18P02BF	QFN2X2-6L	AP18P02BF XXX YYYY	3000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-20	V
V_{GS}	Gate-Source Voltage	±12	V
I_D@T_A=25℃	Continuous Drain Current, V_{GS} @ -4.5V[1]	-18	A
I_D@T_A=70℃	Continuous Drain Current, V_{GS} @ -4.5V[1]	-10.4	A
I_{DM}	Pulsed Drain Current[2]	-54	A
P_D@T_A=25℃	Total Power Dissipation[3]	1.31	W
P_D@T_A=70℃	Total Power Dissipation[3]	0.74	W
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃
RθJA	Thermal Resistance Junction-Ambient [1]	57	℃/W
RθJC	Thermal resistance, junction-case	7.4	℃/W

Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=-250uA	-20	-23	---	V
△BVDSS/△TJ	BV_{DSS} Temperature Coefficient	Reference to 25℃ , I_D=-1mA	---	-0.014	---	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-4.5V , I_D=-5.0A	---	18	22	mΩ
		V_{GS}=-2.5V , I_D=-3.0A	---	24	30	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =-250uA	-0.5	-0.6	-1.2	V
△$V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	3.95	---	mV/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-16V , V_{GS}=0V , T_J=25℃	---	---	-1	uA
		V_{DS}=-16V , V_{GS}=0V , T_J=55℃	---	---	-5	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±12V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=-5V , I_D=-3A	---	12.8	---	S
Q_g	Total Gate Charge (-4.5V)	V_{DS}=-15V , V_{GS}=-4.5V , I_D=-3A	---	10.2	14.3	nC
Q_{gs}	Gate-Source Charge		---	1.89	2.6	
Q_{gd}	Gate-Drain Charge		---	3.1	4.3	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=-10V , V_{GS}=-4.5V , R_G=3.3 , I_D=-3A	---	5.6	11.2	ns
T_r	Rise Time		---	40.8	73	
$T_{d(off)}$	Turn-Off Delay Time		---	33.6	67	
T_f	Fall Time		---	18	36	
C_{iss}	Input Capacitance	V_{DS}=-15V , V_{GS}=0V , f=1MHz	---	857	1200	pF
C_{oss}	Output Capacitance		---	114	160	
C_{rss}	Reverse Transfer Capacitance		---	108	151	
I_S	Continuous Source Current[1,4]	V_G=V_D=0V , Force Current	---	---	-4.9	A
I_{SM}	Pulsed Source Current[2,4]		---	---	-14	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=-1A , T_J=25℃	---	---	-1	V
t_{rr}	Reverse Recovery Time	IF=-3A , di/dt=100A/μs , T_J=25℃	---	21.8	---	nS
Q_{rr}	Reverse Recovery Charge		---	6.9	---	nC

Note :
1、The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2、The data tested by pulsed , pulse width △ 300us , duty cycle △ 2%
3、The power dissipation is limited by 150℃ junction temperature
4、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

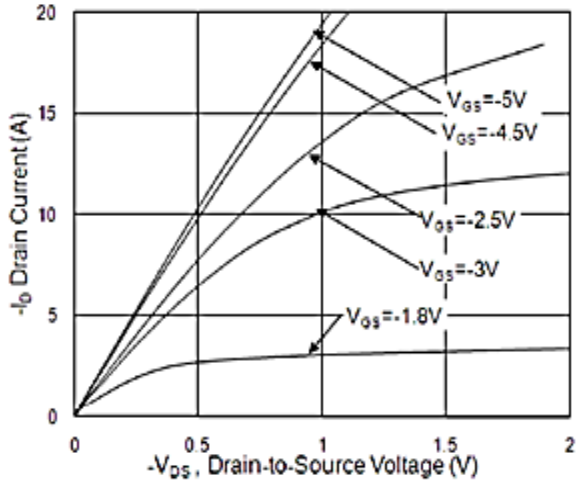


Fig.1 Typical Output Characteristics

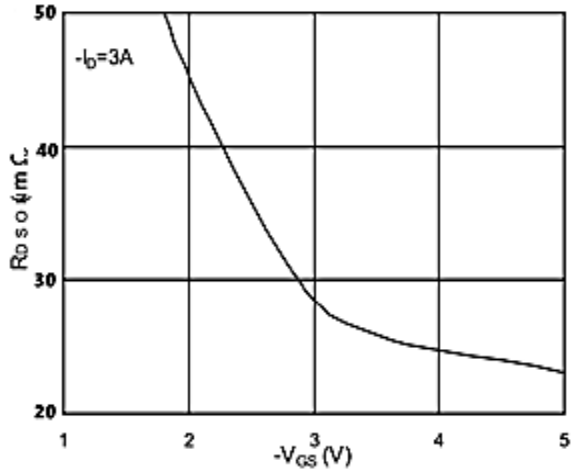


Fig.2 On-Resistance vs. G-S Voltage

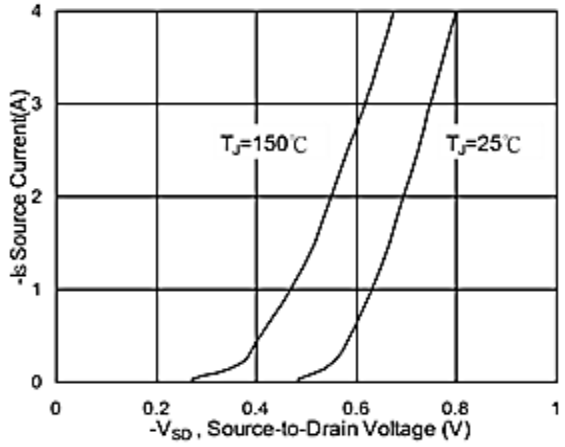


Fig.3 Forward Characteristics of Reverse

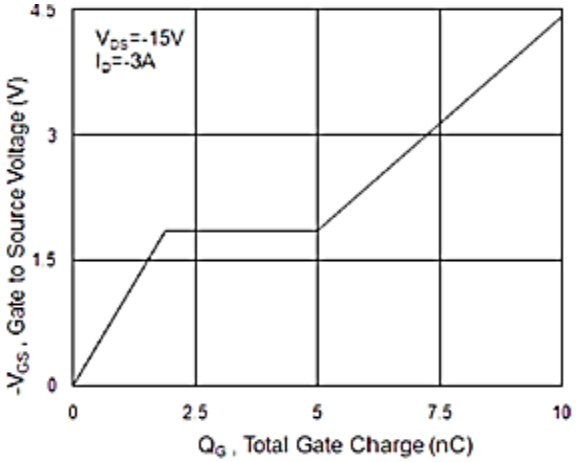


Fig.4 Gate-charge Characteristics

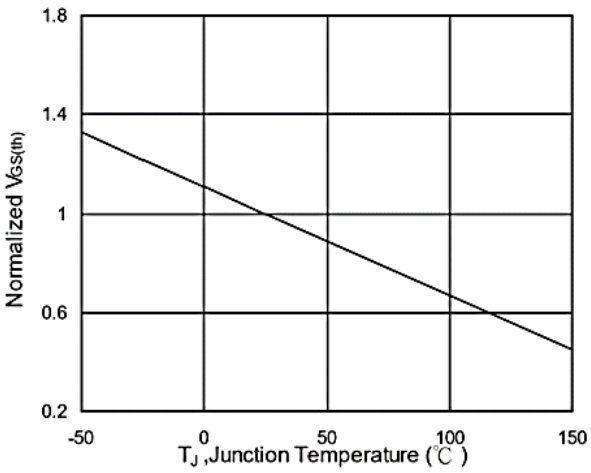


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

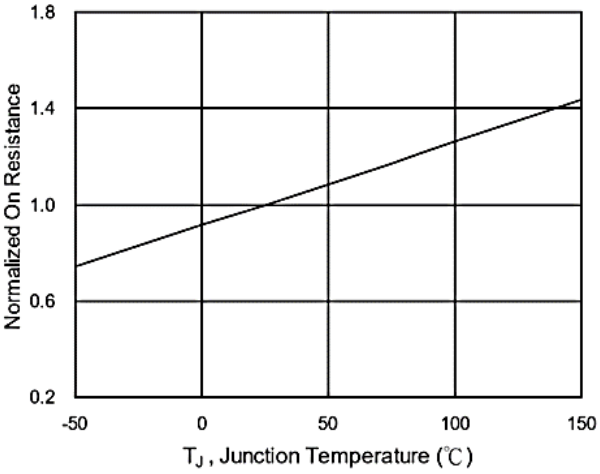


Fig.6 Normalized R_{DSON} vs. T_J

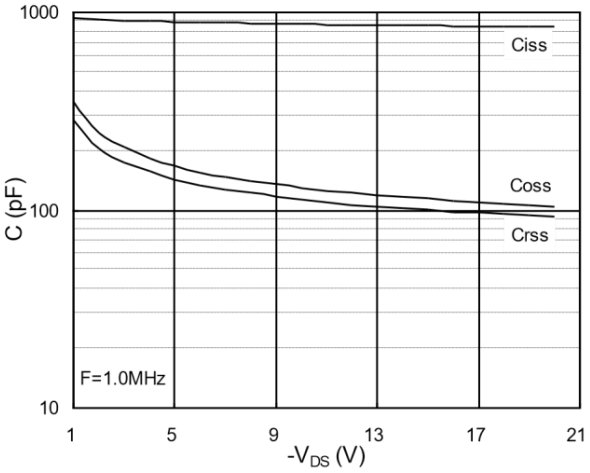


Fig.7 Capacitance

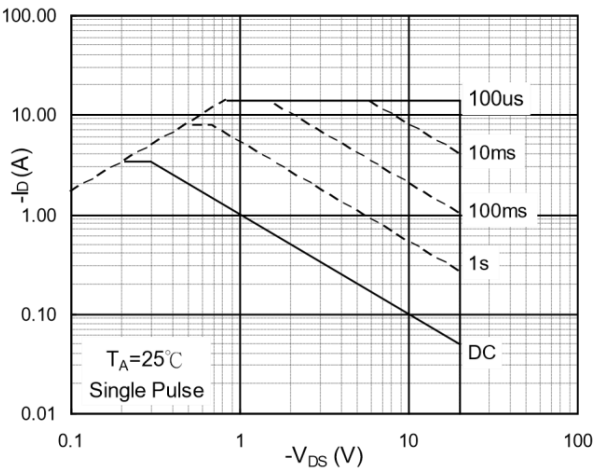


Fig.8 Safe Operating Area

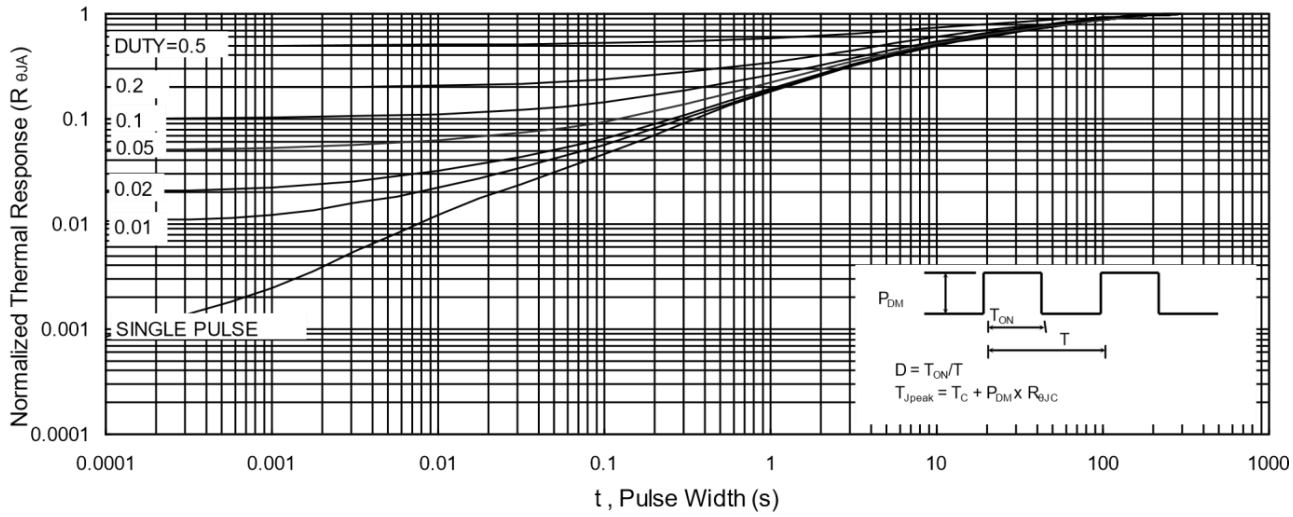


Fig.9 Normalized Maximum Transient Thermal Impedance

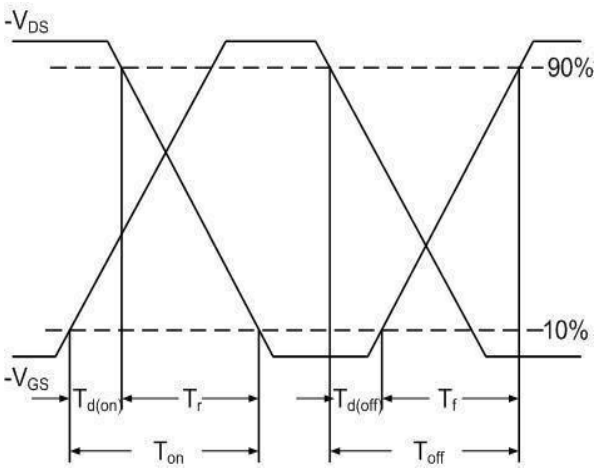


Fig.10 Switching Time Waveform

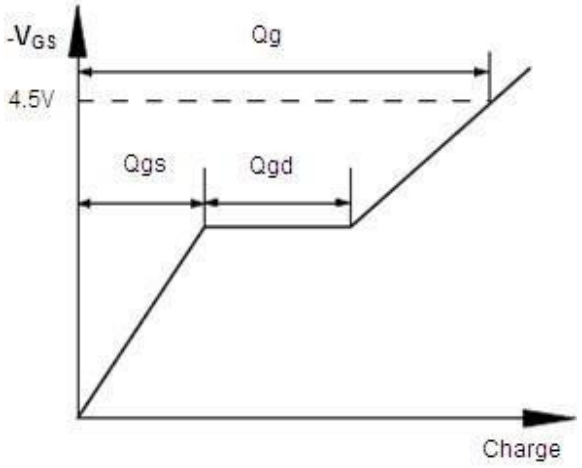
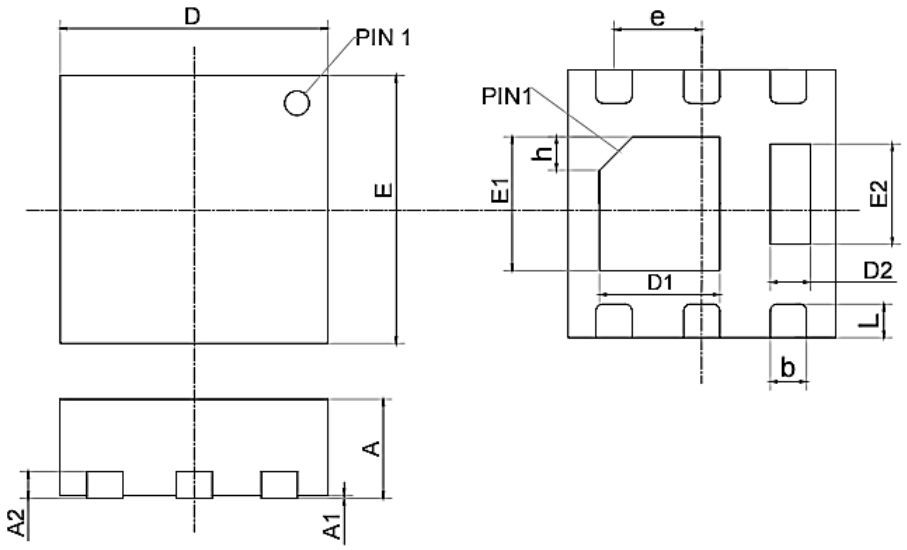


Fig.11 Gate Charge Waveform

Package Mechanical Data：QFN2*2-6L



Symbol	Dim in mm		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	--	0.02	0.05
A2	0.18	0.20	0.25
b	0.20	0.27	0.34
D	1.95	2.00	2.05
E	1.95	2.00	2.05
D1	0.80	0.90	1.00
E1	0.90	1.00	1.10
D2	0.20	0.30	0.40
E2	0.65	0.75	0.85
L	0.20	0.25	0.35
h	0.20	0.25	0.30
e	0.65 BSC		

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-20V P-Channel Enhancement Mode MOSFET

Edition	Date	Change
REV1.0	2023/4/31	Initial release