

65V N-Channel Enhancement Mode MOSFET

Description

The AP150N06D uses advanced **APM-SGT II** technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 10V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

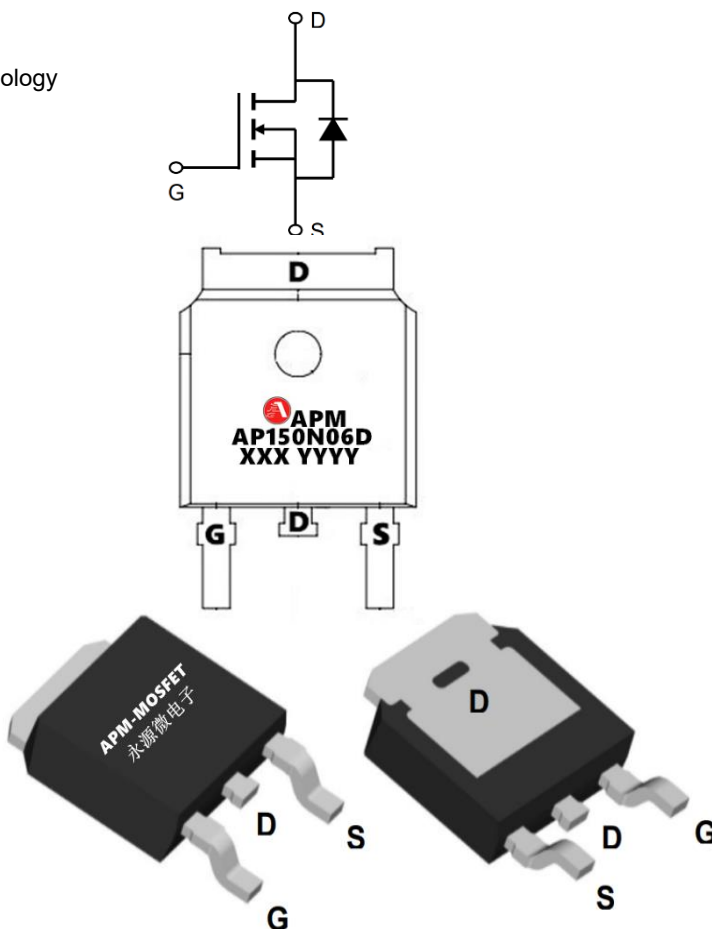
$V_{DS} = 60V$ $I_D = 150A$

$R_{DS(ON)} < 2.8m\Omega$ @ $V_{GS}=10V$ (**Type: 2.1mΩ**)

Application

Battery protection

UPS



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP150N06D	TO-252-3L	AP150N06D XXX YYYY	2500

Absolute Maximum Ratings ($T_C=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^\circ\text{C}$	Continuous Drain Current ^{1,6}	150	A
$I_D@T_C=100^\circ\text{C}$	Continuous Drain Current ^{1,6}	105	A
I_{DM}	Pulsed Drain Current ²	450	A
E_{AS}	Single Pulse Avalanche Energy ³	585	mJ
I_{AS}	Avalanche Current	55	A
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation ⁴	168	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	62.5	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	1.5	$^\circ\text{C/W}$



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Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	60	68	-	V
I _{GSS}	Gate-body Leakage Current	V _{DS} =0V, V _{GS} =±20V	-	-	±100	nA
I _{DSS} T _J =25°C	Zero Gate Voltage Drain Current	V _{DS} =60V, V _{GS} =0V	-	-	1	μA
I _{DSS} T _J =100°C	Zero Gate Voltage Drain Current		-	-	100	
V _{GS(th)}	Gate-Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	2.0	2.8	4.0	V
R _{DS(on)}	Drain-Source On-Resistance ⁴	V _{GS} =10V, I _D =20A	-	2.1	2.8	mΩ
g _{fs}	Forward Transconductance ⁴	V _{DS} =10V, I _D =20A	-	89	-	S
C _{iss}	Input Capacitance	V _{DS} =30V, V _{GS} =0V, f =1MHz	-	4080	-	pF
C _{oss}	Output Capacitance		-	1053	-	
C _{rss}	Reverse Transfer Capacitance		-	31	-	
R _G	Gate Resistance	f =1MHz	-	2.2	-	Ω
Q _g	Total Gate Charge	V _{GS} =10V, V _{DS} =30V, I _D =20A	-	68	-	nC
Q _{gs}	Gate-Source Charge		-	16	-	
Q _{gd}	Gate-Drain Charge		-	20.5	-	
t _{d(on)}	Turn-on Delay Time	V _{GS} =10V, V _{DD} =30V, R _G =3Ω, I _D =20A	-	17	-	ns
t _r	Rise Time		-	17.8	-	
t _{d(off)}	Turn-off Delay Time		-	40	-	
t _f	Fall Time		-	21	-	
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A , dI/dt=100A/μs	-	56	-	ns
Q _{rr}	Body Diode Reverse Recovery Charge		-	67.5	-	nC
V _{SD}	Diode Forward Voltage ⁴	I _S =20A, V _{GS} =0V	-	-	1.2	V
I _S	Continuous Source Current	T _C =25°C	-	-	140	A

Note :

- 1、The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width .The EAS data shows Max. rating .
- 3、The power dissipation is limited by 175°C junction temperature
- 4、EAS condition: T_J=25°C, V_{DD}=48V, V_G=10V, R_G=25Ω, L=0.1mH, I_{AS}= 55A
- 5、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

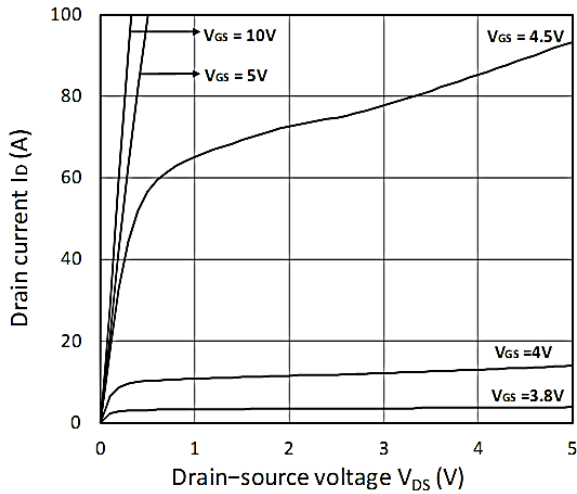


Figure 1. Output Characteristics

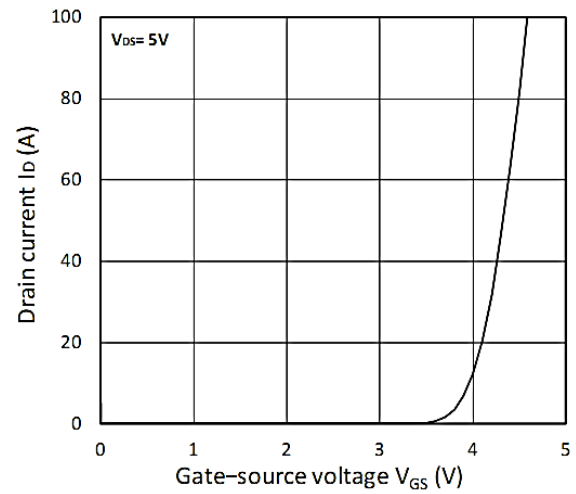


Figure 2. Transfer Characteristics

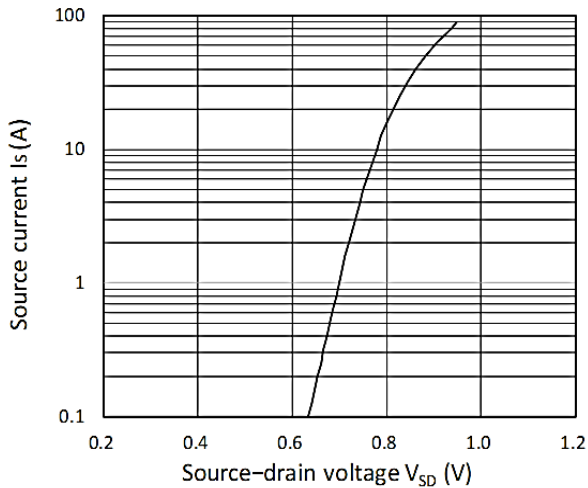


Figure 3. Forward Characteristics of Reverse

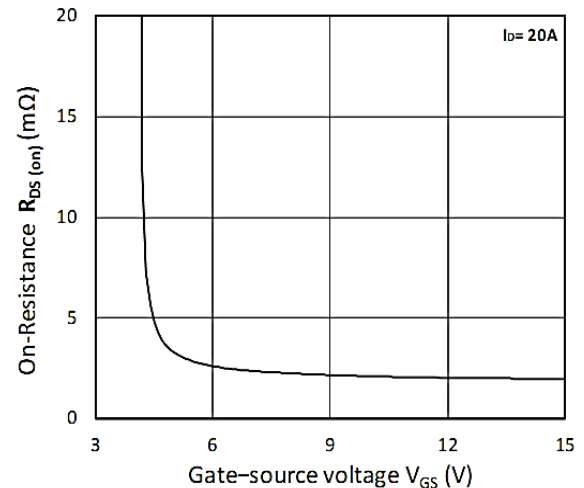


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

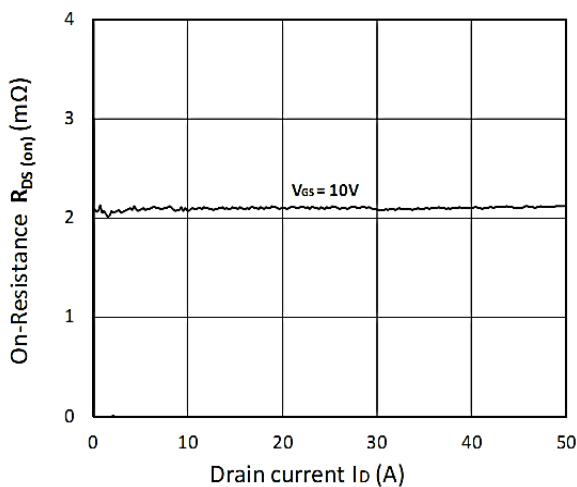


Figure 5. $R_{DS(ON)}$ vs. I_D

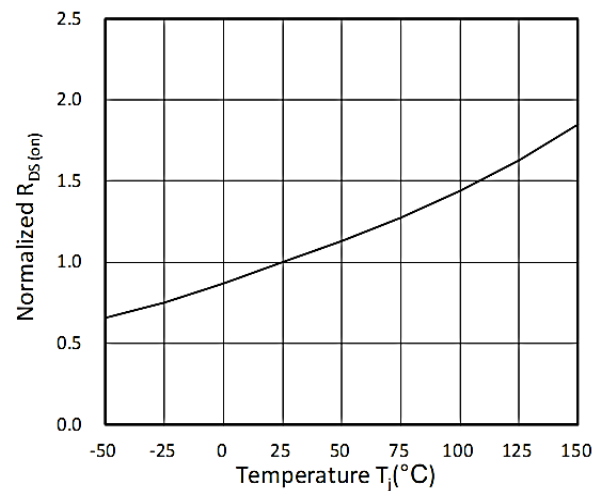


Figure 6. Normalized $R_{DS(ON)}$ vs. Temperature

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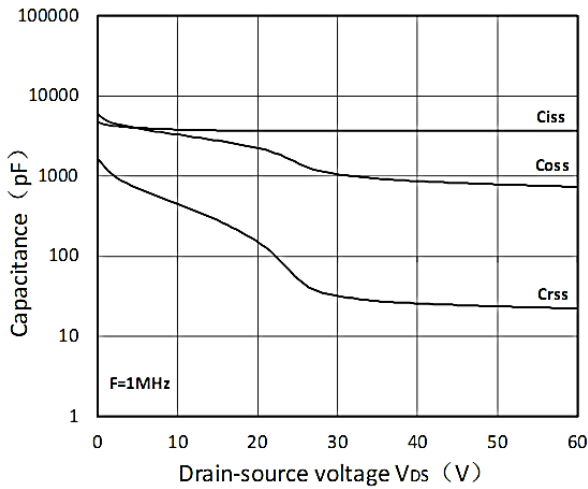


Figure 7. Capacitance Characteristics

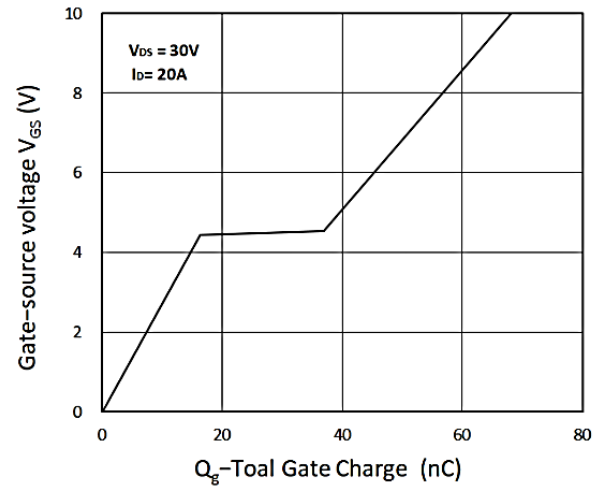


Figure 8. Gate Charge Characteristics

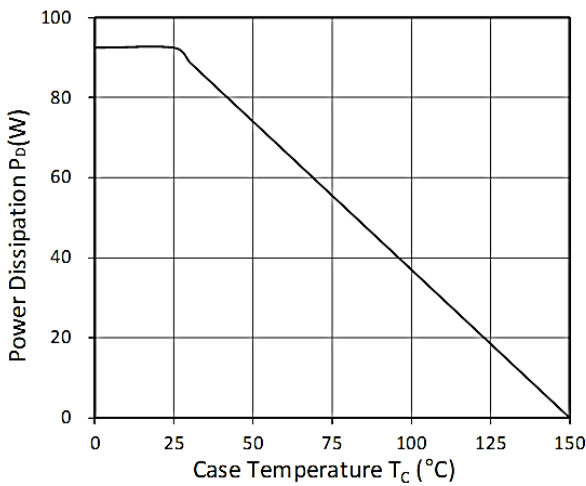


Figure 9. Power Dissipation

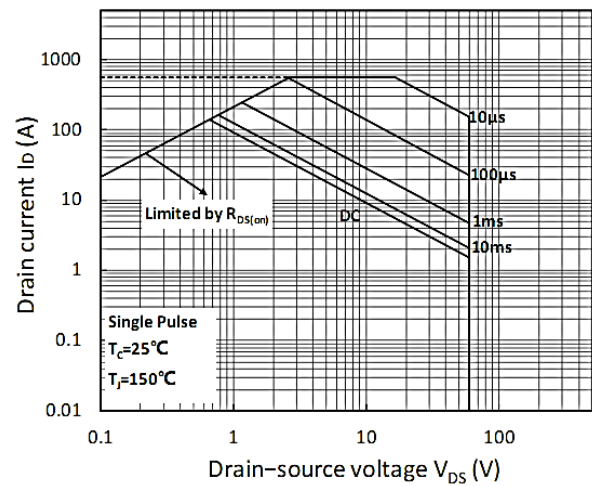


Figure10. Safe Operating Area

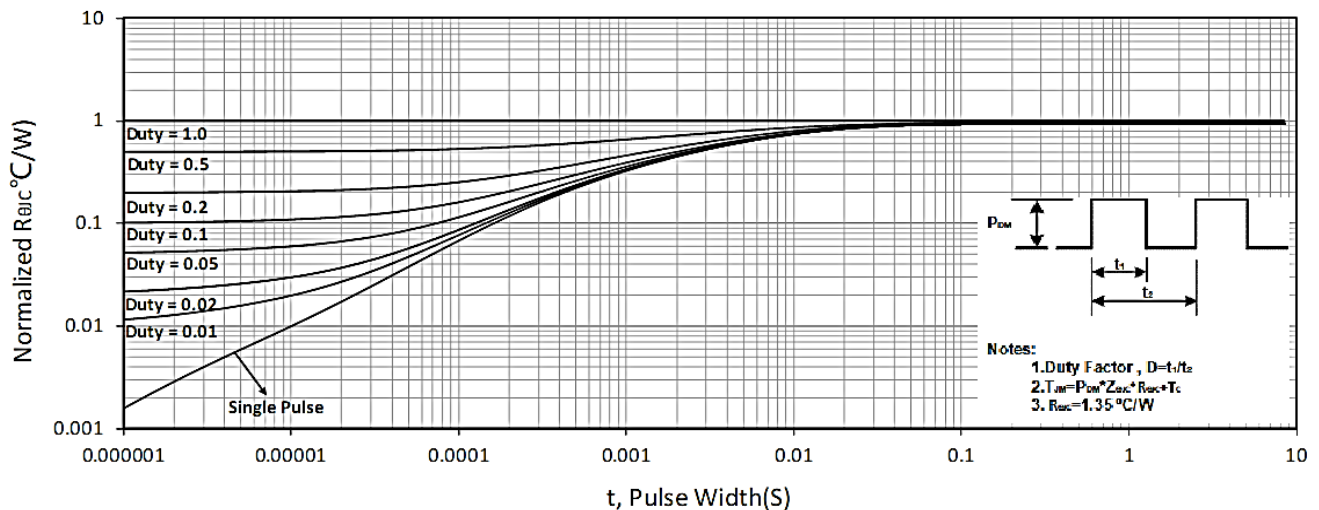
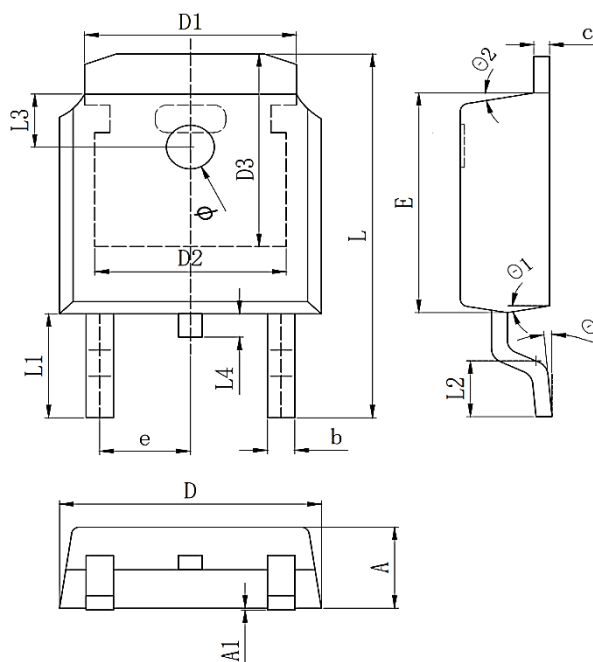


Figure 11. Normalized Maximum Transient Thermal Impedance

Package Mechanical Data-TO-252-3L



Symbol	Dim in mm		
	Min	Typ	Max
A	2.1	2.3	2.5
A1	0	0.064	0.128
b	0.64	0.75	0.86
c	0.45	0.52	0.6
D	6.4	6.6	6.8
D1	5.33REF		
D2	4.83REF		
D3	5.25REF		
E	5.9	6.1	6.3
e	2.286TYP		
L	9.8	10.1	10.4
L1	2.888REF		
L2	1.4	1.5	1.7
L3	1.65REF		
L4	0.6	0.8	1
φ	1.1	1.2	1.3
θ	0°		10°
θ1	5°		10°
θ2	5°		10°

65V N-Channel Enhancement Mode MOSFET**Attention**

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Edition	Date	Change
REV1.0	2024/3/20	Initial release

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