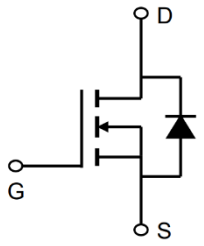
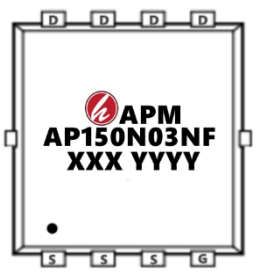
AP150N03NF

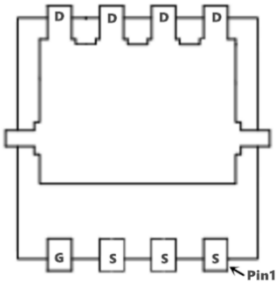
30V N-Channel Enhancement Mode MOSFET

Description

The AP150N03NF uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.







General Features

V_{DS} = 30V I_D =150A

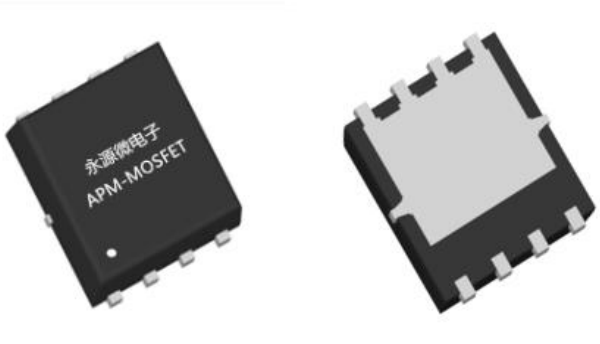
$R_{DS(ON)}$ < 2mΩ @ V_{GS}=10V （Type:1.4mΩ）

Application

Battery protection

Load switch

Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP150N03NF	PDFN5*6-8L	AP150N03NF XXX YYYY	5000

Absolute Maximum Ratings (TC=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	30	V
VGS	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ 10V[1,6]	150	A
I_D@T_C=100℃	Continuous Drain Current, V_{GS} @ 10V[1,6]	78	A
IDM	Pulsed Drain Current[2]	500	A
EAS	Single Pulse Avalanche Energy[3]	240	mJ
IAS	Avalanche Current	55	A
P_D@T_C=25℃	Total Power Dissipation[4]	48	W
P_D@T_A=25℃	Total Power Dissipation[4]	2.6	W
TSTG	Storage Temperature Range	-55 to 175	℃
T_J	Operating Junction Temperature Range	-55 to 175	℃
$R_{\theta}JA$	Thermal Resistance Junction-Ambient [1]	62	℃/W
$R_{\theta}JA$	Thermal Resistance Junction-Ambient [1] (t ≤10s)	25	℃/W
$R_{\theta}JC$	Thermal Resistance Junction-Case[1]	2.6	℃/W

Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	30	33	---	V
△BVDSS/△TJ	BVDSS Temperature Coefficient	Reference to 25℃ , I_D=1mA	---	0.0213	---	V/℃
RDS(ON)	Static Drain-Source On-Resistance	V_{GS}=10V , I_D=30A	---	1.4	2.0	mΩ
		V_{GS}=4.5V , I_D=20A	---	2.3	3.2	
VGS(th)	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =250uA	1.2	1.6	2.5	V
△$V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-5.73	---	mV/℃
IDSS	Drain-Source Leakage Current	V_{DS}=24V , V_{GS}=0V , T_J=25℃	---	---	1	uA
		V_{DS}=24V , V_{GS}=0V , T_J=55℃	---	---	5	
IGSS	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	---	---	±100	nA
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	1.4	---	Ω
Q_g	Total Gate Charge (4.5V)	V_{DS}=15V , V_{GS}=4.5V , I_D=30A	---	70	---	nC
Q_{gs}	Gate-Source Charge		---	12	---	
Q_{gd}	Gate-Drain Charge		---	17	---	
Td(on)	Turn-On Delay Time	V_{DD}=15V , V_{GS}=10V , R_G=3Ω I_D=30A	---	10	---	ns
T_r	Rise Time		---	6.5	---	
Td(off)	Turn-Off Delay Time		---	75	---	
T_f	Fall Time		---	18	---	
C_{iss}	Input Capacitance	V_{DS}=15V , V_{GS}=0V , f=1MHz	---	4930	---	Pf
Coss	Output Capacitance		---	682	---	
Crss	Reverse Transfer Capacitance		---	566	---	
I_S	Continuous Source Current[1,5]	V_G=V_D=0V , Force Current	---	---	120	A
ISM	Pulsed Source Current[2,5]		---	---	480	A
VSD	Diode Forward Voltage[2]	V_{GS}=0V , I_S=30A , T_J=25℃	---	---	1.2	V
Qrr	Body Diode Reverse Recovery Charge	IF =20A,dI/dt=100A/μs	---	30	---	ns
trr	Body Diode Reverse Recovery Time		---	15	---	nC

Note :

1、The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.
2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3、The EAS data shows Max. rating . The test condition is VDD=24V,VGS =10V,L=0.1mH,IAS =55A
4、The power dissipation is limited by 150℃ junction temperature
5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation

Typical Characteristics

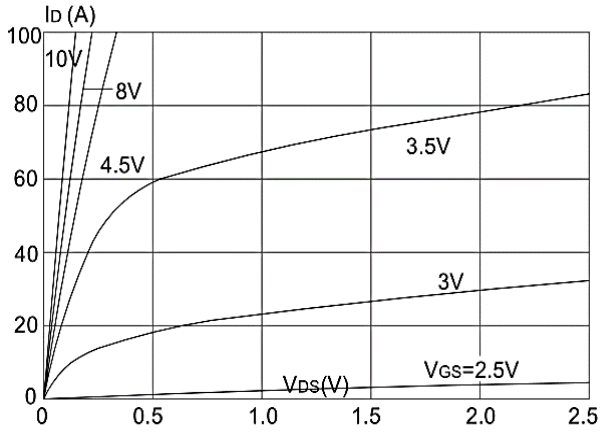


Figure1: Output Characteristics

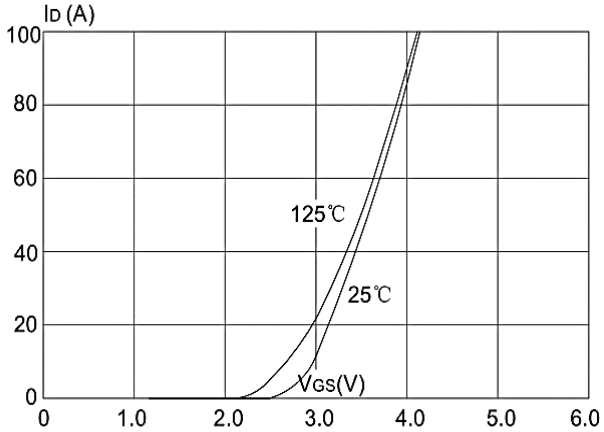


Figure 2: Typical Transfer Characteristics

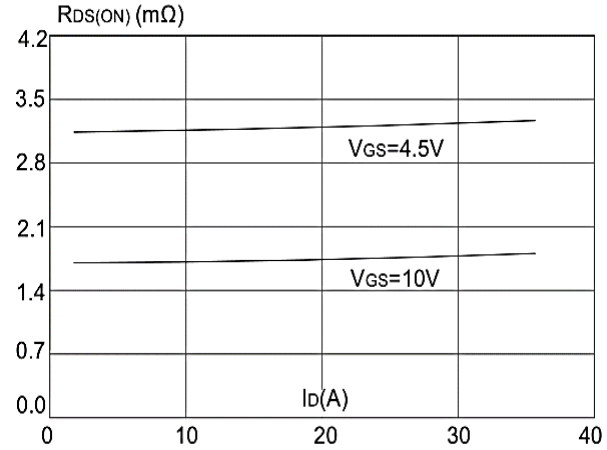


Figure 3:On-resistance vs. Drain Current

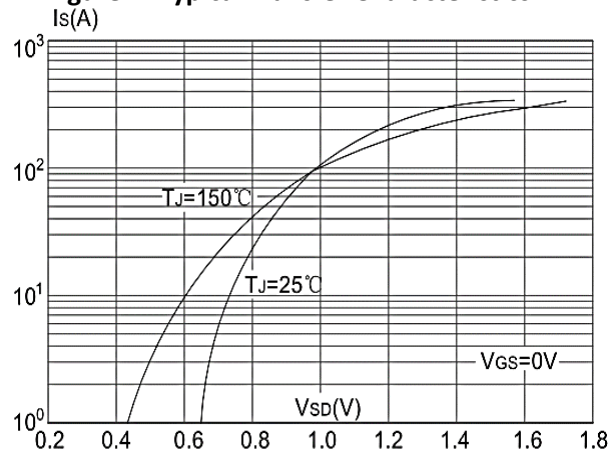


Figure 4: Body Diode Characteristics

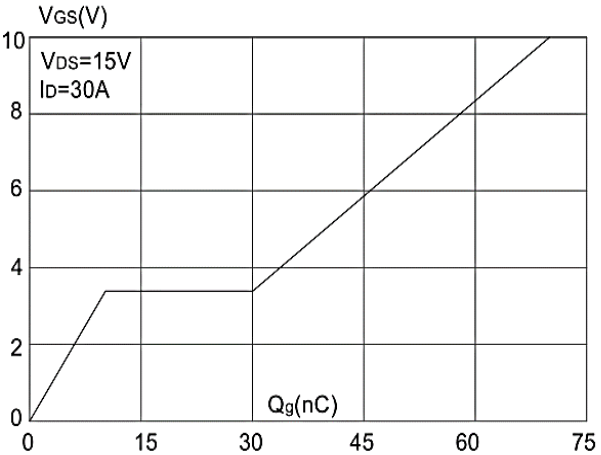


Figure 5: Gate Charge Characteristics

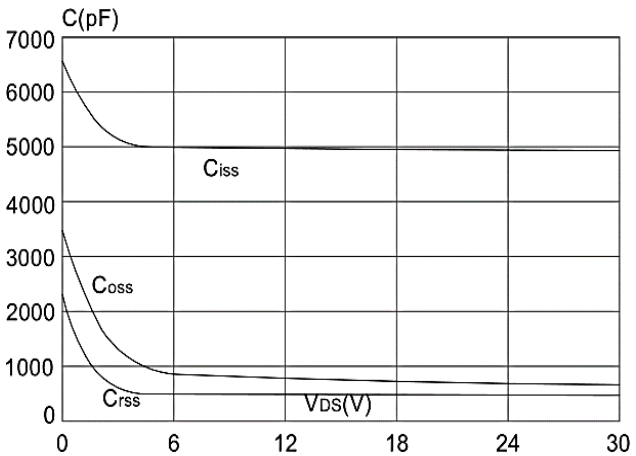


Figure 6: Capacitance Characteristics

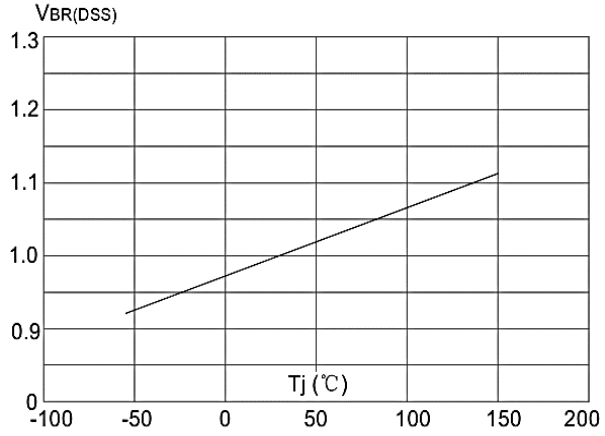


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

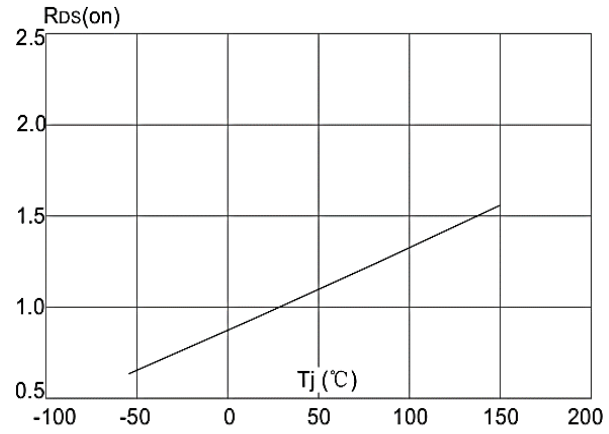


Figure 8: Normalized on Resistance vs Junction Temperature

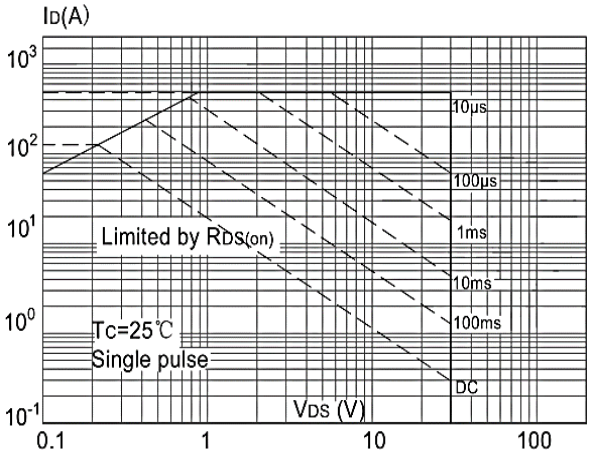


Figure 9: Maximum Safe Operating Area vs. Case Temperature

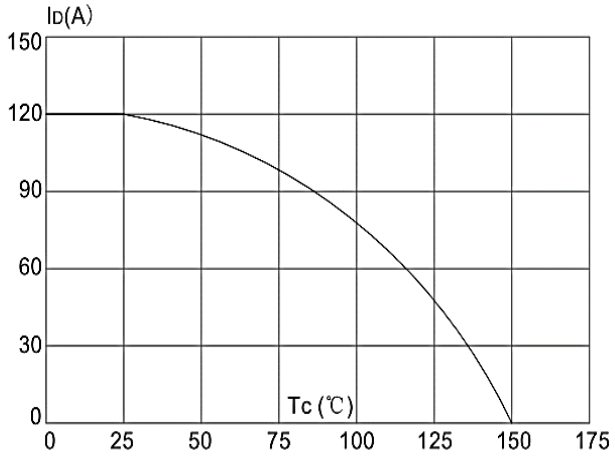


Figure 10: Maximum Continuous Drain Current

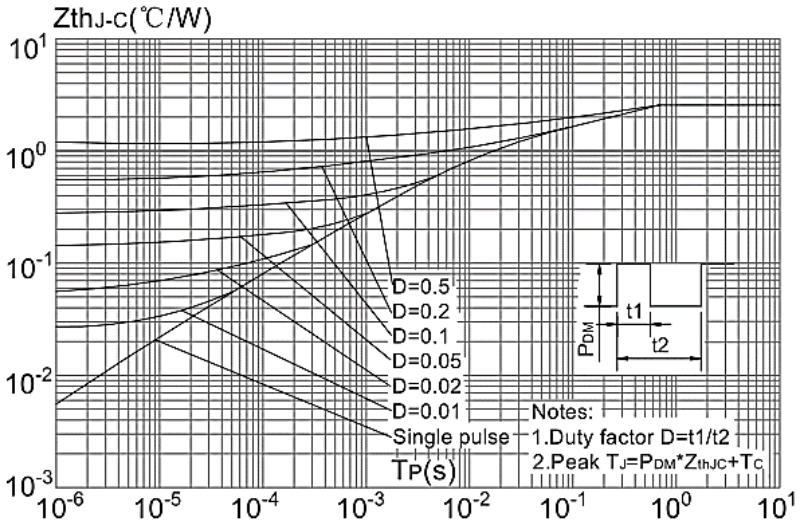
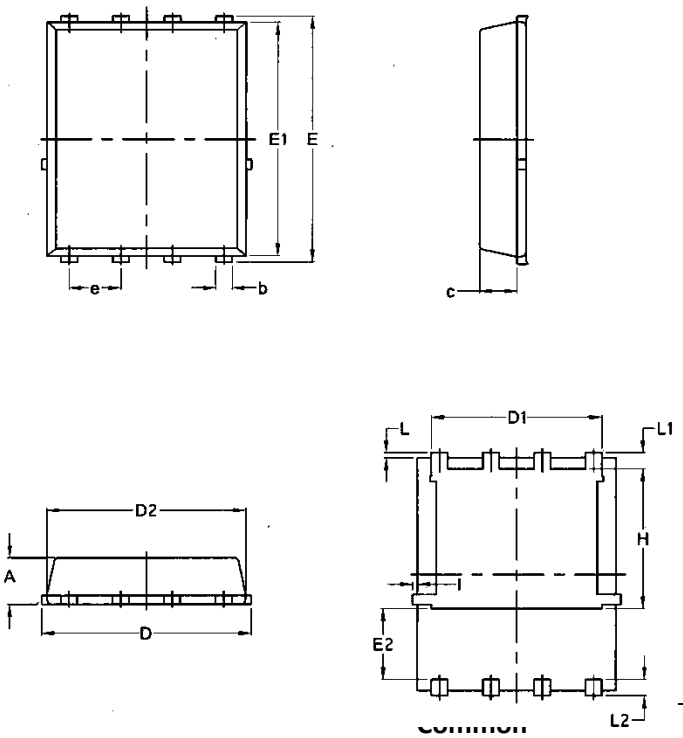


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

Package Mechanical Data-DFN5*6-8L-JQ Single



Symbol	Common			
	mm		Inch	
	Mim	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070

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AP150N03NF

30V N-Channel Enhancement Mode MOSFET

Edition	Date	Change
Rve1.0	2019/8/1	Initial release