

100V N-Channel Enhancement Mode MOSFET

Description

The AP140N10D uses advanced **APM-SGT_{II}** technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 10V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = 100V$ $I_D = 140A$

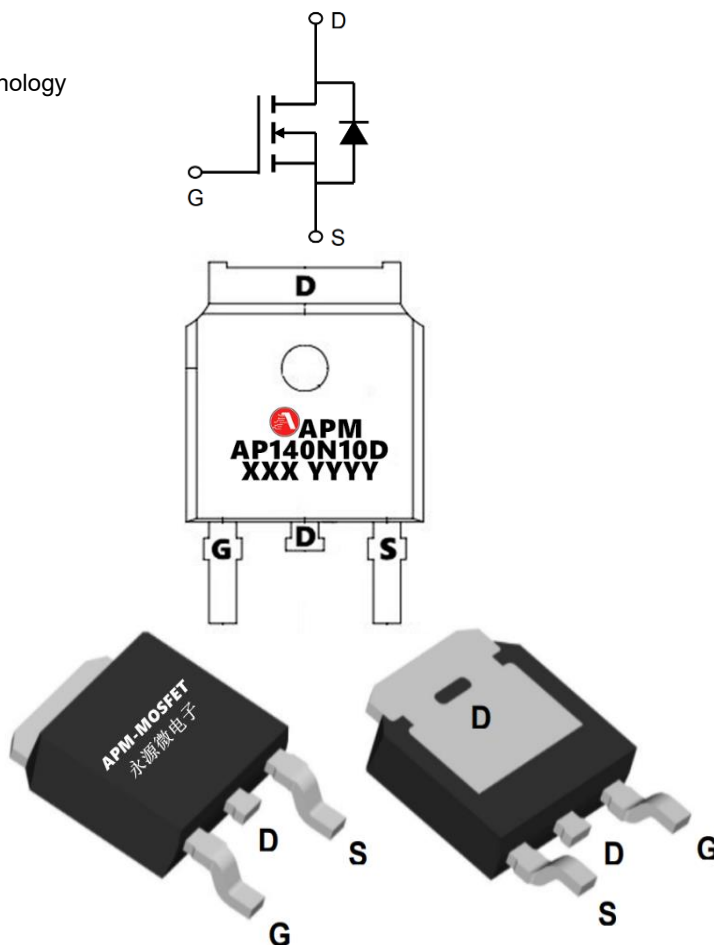
$R_{DS(ON)} < 5.5m\Omega$ @ $V_{GS}=10V$ (Type: 4.5m Ω)

Application

DC/DC Converter

LED Backlighting

Power Management Switches



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP140N10D	TO-252-3L	AP140N10D XXX YYYY	2500

Absolute Maximum Ratings ($T_C=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	140	A
$I_D@T_C=100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	85	A
IDM	Pulsed Drain Current	417	A
EAS	Single Pulse Avalanche Energy	245	mJ
IAS	Avalanche Current	42	A
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation ⁴	167	W
TSTG	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient	0.88	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case	62	$^\circ\text{C/W}$

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Electrical Characteristics ($T_c=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDSS	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	100	-	-	V
IGSS	Gate-body Leakage current	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	± 100	nA
IDSS	Zero Gate Voltage Drain Current $T_J=25^{\circ}\text{C}$	$V_{DS} = 100V, V_{GS} = 0V$	-	-	1	μA
IDSS	Zero Gate Voltage Drain Current $T_J=100^{\circ}\text{C}$		-	-	100	
VGS(th)	Gate-Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.0	2.9	4.0	V
RDS(on)	Drain-Source on-Resistance ²	$V_{GS} = 10V, I_D = 20A$	-	4.5	5.5	m Ω
Ciss	Input Capacitance	$V_{DS} = 50V, V_{GS} = 0V, f = 1MHz$	-	2816	-	pF
Coss	Output Capacitance		-	614	-	
Crss	Reverse Transfer Capacitance		-	7.4	-	
Rg	Gate Resistance	$V_{GS} = 0V, V_{DS} = 0V, f = 1MHz$	-	2.4	-	Ω
Qg	Total Gate Charge	$V_{GS} = 10V, V_{DS} = 50V, I_D = 20A$	-	42	-	nC
Qgs	Gate-Source Charge		-	9.7	-	
Qgd	Gate-Drain Charge		-	10.6	-	
td(on)	Turn-on Delay Time	$V_{GS} = 10V, V_{DS} = 50V, R_G = 3\Omega, I_D = 20A$	-	13	-	ns
tr	Rise Time		-	25	-	
td(off)	Turn-off Delay Time		-	43	-	
tf	Fall Time		-	37	-	
VSD	Diode Forward Voltage ²	$I_F = 20A, V_{GS} = 0V$	-	-	1.2	V
IS	Continuous Source Current ^{1,5}	$V_G = V_D = 0V$, Force Current	-	-	167	A
trr	Body Diode Reverse Recovery Time	$I_F = 20A, dI/dt = 100A/\mu s$	-	60	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	61	-	nC

Notes:

- 1、The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3、The EAS data shows Max. rating . The test condition is $V_{DD}=50V, V_{GS}=10V, L=0.4mH, I_{AS}=42A$
- 4、The power dissipation is limited by 150°C junction temperature
- 5、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

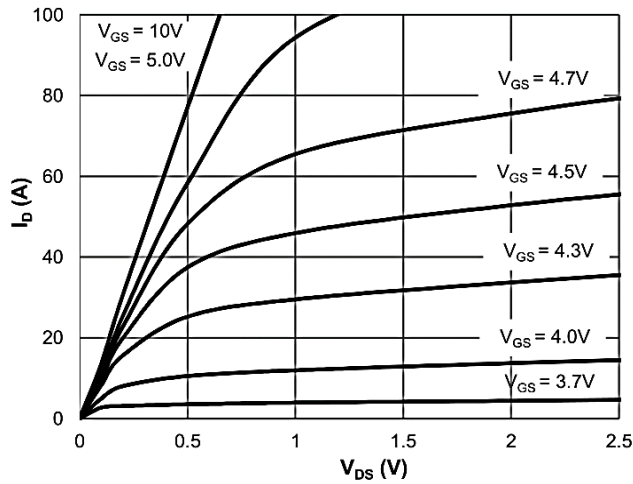


Figure 1: Saturation Characteristics

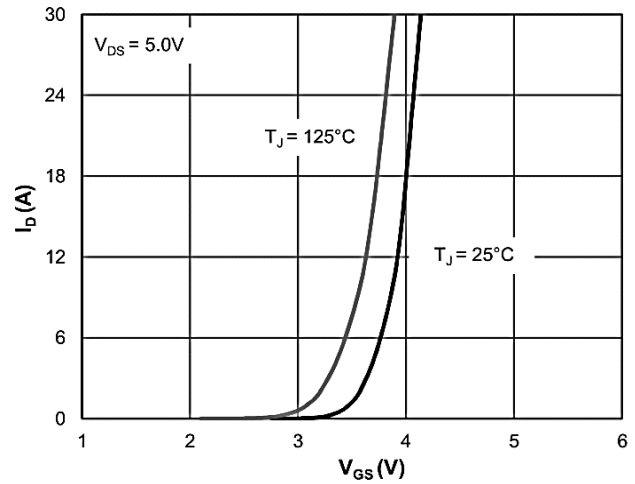


Figure 2: Transfer Characteristics

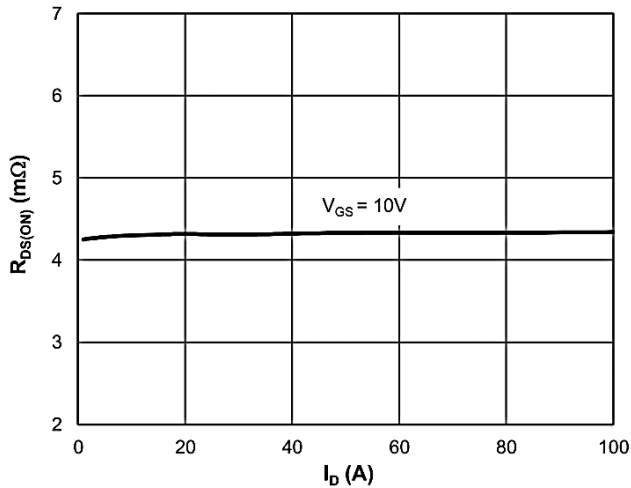


Figure 3: $R_{DS(ON)}$ vs. Drain Current

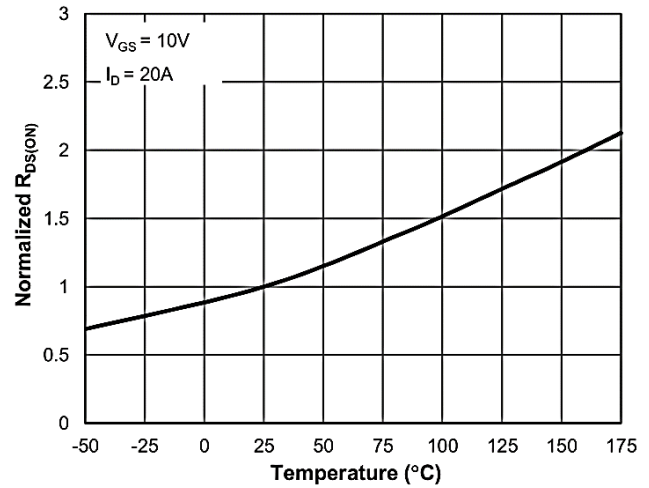


Figure 4: $R_{DS(ON)}$ vs. Junction Temperature

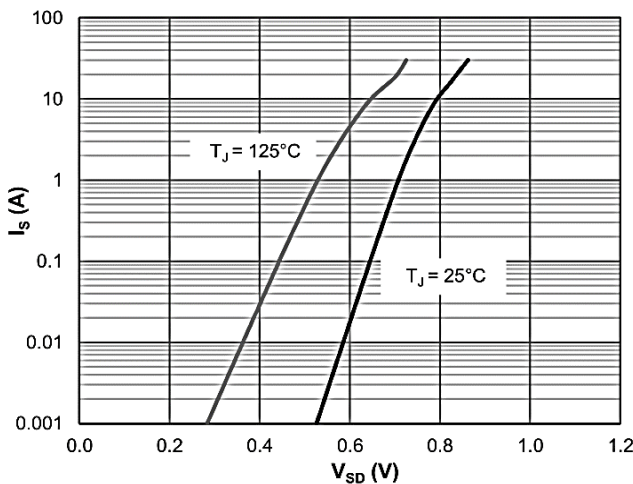


Figure 5: Body-Diode Characteristics

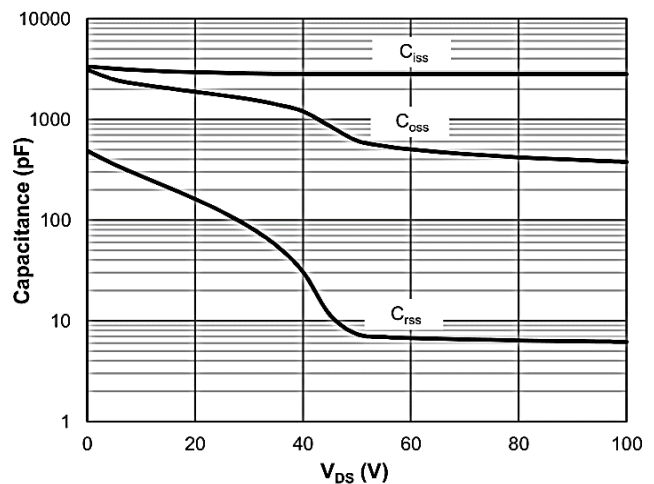


Figure 6: Capacitance Characteristics

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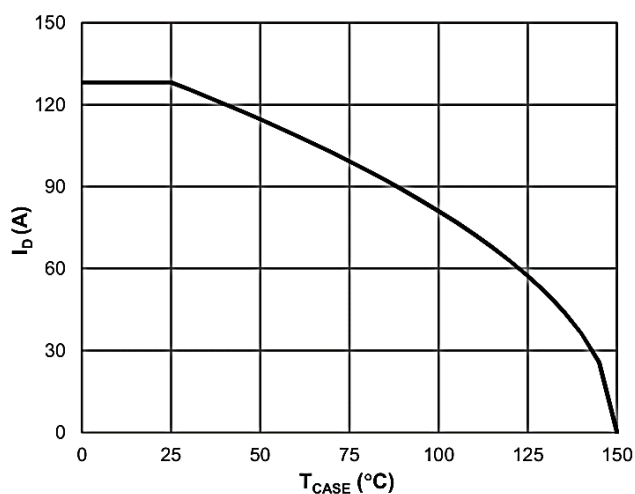


Figure 7: Current De-rating

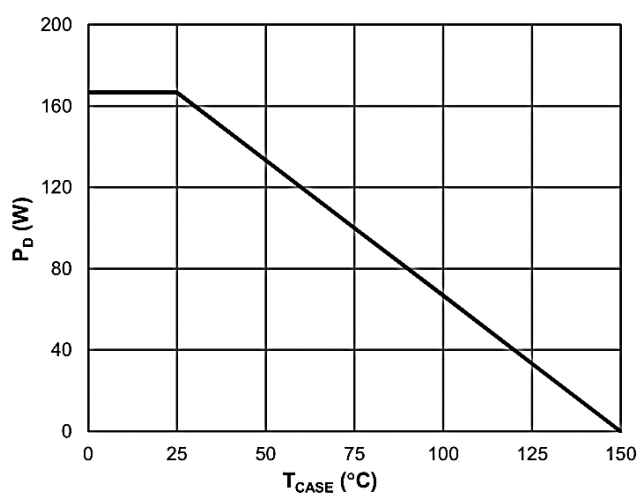


Figure 8: Power De-rating

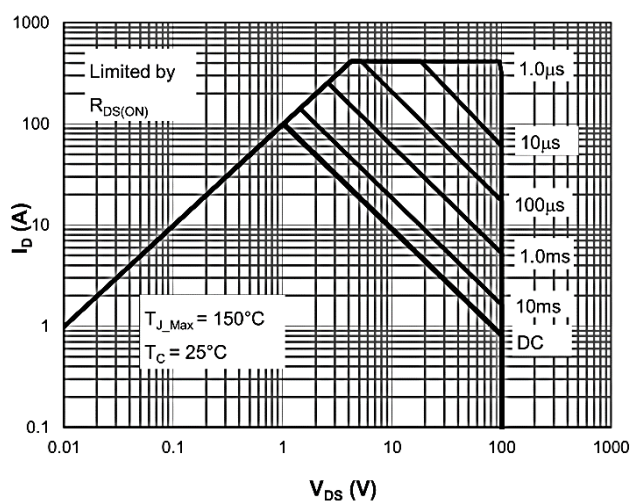


Figure 9: Maximum Safe Operating Area

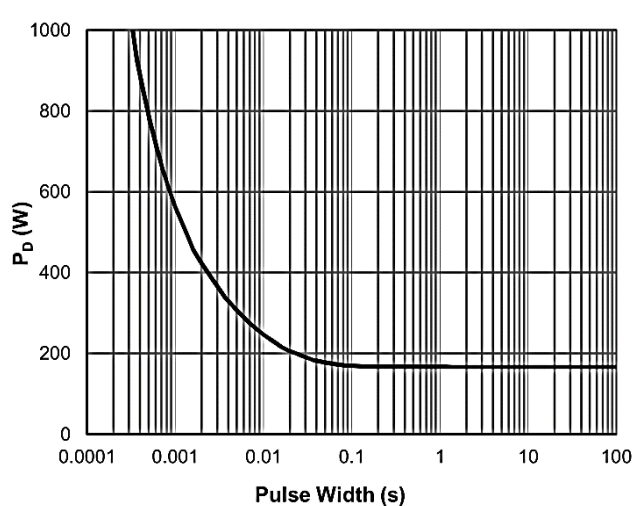


Figure 10: Single Pulse Power Rating, Junction-to-Case

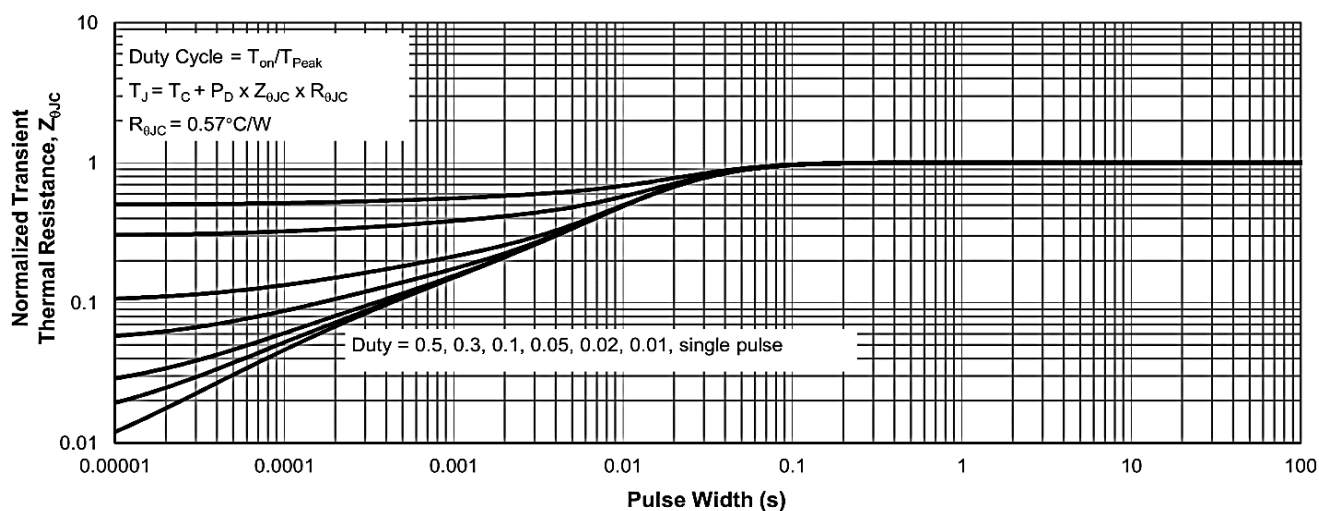
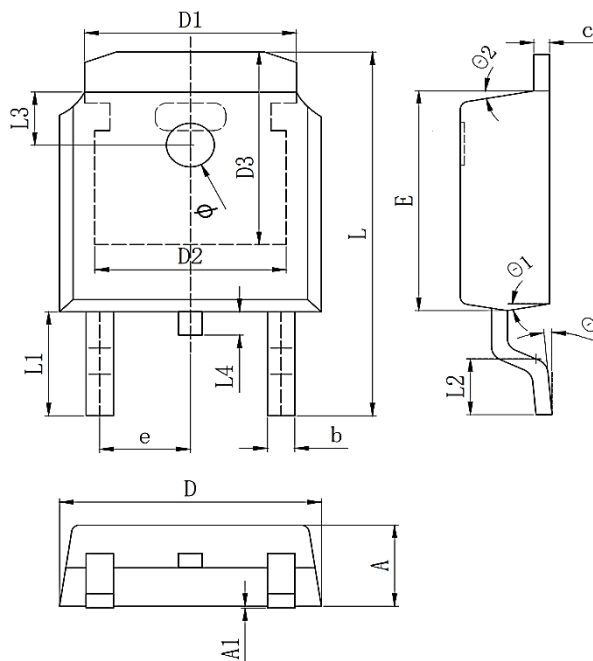


Figure 11: Normalized Maximum Transient Thermal Impedance

Package Mechanical Data-TO-252-3L



Symbol	Dim in mm		
	Min	Typ	Max
A	2.1	2.3	2.5
A1	0	0.064	0.128
b	0.64	0.75	0.86
c	0.45	0.52	0.6
D	6.4	6.6	6.8
D1	5.33REF		
D2	4.83REF		
D3	5.25REF		
E	5.9	6.1	6.3
e	2.286TYP		
L	9.8	10.1	10.4
L1	2.888REF		
L2	1.4	1.5	1.7
L3	1.65REF		
L4	0.6	0.8	1
ϕ	1.1	1.2	1.3
θ	0°		10°
θ_1	5°		10°
θ_2	5°		10°

100V N-Channel Enhancement Mode MOSFET**Attention**

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Edition	Date	Change
REV1.0	2022/8/5	Initial release

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