



## FEATURES

- Ideal for DDR-I, DDR-II and DDR-III  $V_{TT}$  Applications
- Sink and Source up to 2.5Amp
- Integrated Power MOSFETs
- Generates Termination Voltage for SSTL\_2, SSTL\_18, HSTL, SCSI-2 and SCSI-3 Interfaces.
- High Accuracy Output Voltage at Full-Load
- Output Adjustment by Two External Resistors
- Built-in Soft-start Function
- Shutdown for Suspend to RAM (STR) Functionality with High-Impedance Output
- Current Limiting Protection
- On-Chip Thermal Protection
- Available in ESOP-8 (Exposed Pad) Packages
- $V_{IN}$  and  $V_{CNTL}$  Under Voltage Protection
- RoHS Compliant and Halogen Free

## APPLICATION

- Desktop PCs, Notebooks, and Workstations
- Graphics Card Memory Termination
- Set Top Boxes, Digital TVs, Printers
- Embedded Systems
- Active Termination Buses
- DDR-I, DDR-II and DDR-III Memory Systems

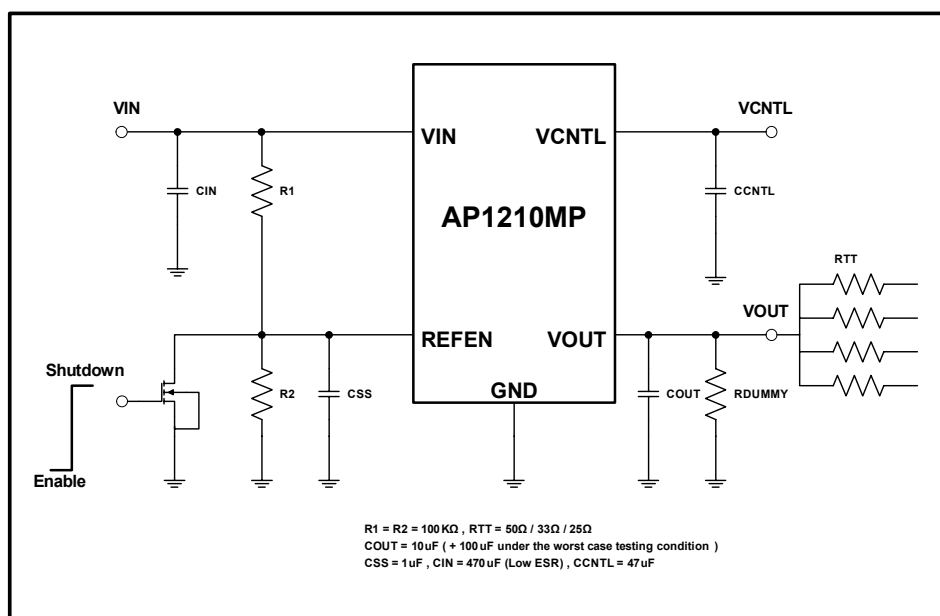
## DESCRIPTION

The AP1210MP is a simple, cost-effective and high-speed linear regulator designed to generate termination voltage in double data rate (DDR) memory system to comply with the JEDEC SSTL\_2 and SSTL\_18 or other specific interfaces such as HSTL, SCSI-2 and SCSI-3 etc. devices requirements. The regulator is capable of actively sinking or sourcing up to 2.5A while regulating an output voltage to within 40mV. The output termination voltage can be tightly regulated to track  $1/2V_{DDQ}$  by two external voltage divider resistors or the desired output voltage can be pro-programmed by externally forcing the REFEN pin voltage.

The AP1210MP also incorporates a high-speed differential amplifier to provide ultra-fast response in line/load transient. Other features include extremely low initial offset voltage, excellent load regulation, current limiting in bi-directions and on-chip thermal shut-down protection. Built-in softstart function avoids a misoperation by inrush current.

The AP1210MP are available in the ESOP-8 (Exposed Pad) surface mount packages.

## TYPICAL APPLICATION





## ABSOLUTE MAXIMUM RATINGS<sup>(Note1)</sup>

Input Voltage ( $V_{IN}$ )	6V
CNTL Pin Voltage ( $V_{CNTL}$ )	6V
Power Dissipation ( $P_D$ )	Internally Limited
Storage Temperature Range ( $T_{ST}$ )	-65 to +150°C
Lead Temperature (Soldering, 10sec.)	260°C
Thermal Resistance from Junction to Case ( $R_{thjc}$ )	28°C/W

Note1 : Exceeding the absolute maximum rating may damage the device.

## OPERATING RATING<sup>(Note2)</sup>

Input Voltage ( $V_{IN}$ )	2.5V to 1.1V $\pm 3\%$
CNTL Pin Voltage ( $V_{CNTL}$ )	5.5V or 3.3V $\pm 5\%$
Junction Temperature Range ( $T_J$ )	-40 to +125°C
Ambient Temperature Range ( $T_A$ )	-40 to +85°C

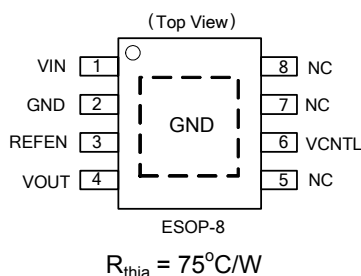
Note2 : The device is not guaranteed to function outside its operating conditions.

## ORDERING / PACKAGE INFORMATION

**AP1210X**

Package Type

MP : ESOP-8



## ELECTRICAL SPECIFICATIONS

( $V_{IN}=1.8\text{V}$ ,  $V_{CNTL}=3.3\text{V}$ ,  $V_{REFEN}=0.9\text{V}$ ,  $C_{OUT}=10\mu\text{F}$ (Ceramic),  $T_A=25^\circ\text{C}$ , unless otherwise specified)

Parameter	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
<b>Input</b>						
VCNTL Operation Current	$I_{CNTL}$	$I_{OUT} = 0\text{A}$	-	0.5	2.5	mA
Standby Current	$I_{STBY}$	$V_{REFEN}=0\text{V}$ (Shutdown)	-	2	5	$\mu\text{A}$
VIN Shutdown Current	$I_{VIN}$	$V_{REFEN}=0\text{V}$ (Shutdown)	-	-	5	$\mu\text{A}$
<b>UVP Function</b>						
VCNTL UVP Rising Threshold	$V_{COP}$	VCNTL Rising	1.9	2.3	2.7	V
VCNTL UVP Hysteresis	$V_{CHYS}$		-	0.35	-	V
VIN UVP Rising Threshold	$V_{IOP}$	V <sub>IOP</sub> Rising	0.7	0.84	1	V
VIN UVP Hysteresis	$V_{IHYS}$		-	0.1	-	V
<b>Output (DDR / DDRII / DDRIII)</b>						
Output Offset Voltage <sup>(Note3)</sup>	$\Delta V_{OS}$	$I_{OUT} = 10\text{mA}$	-20	-	20	mV
		$I_{OUT} = -10\text{mA}$	-20	-	20	
Load Regulation <sup>(Note4)</sup>	$\Delta V_{Load}$	$V_{IN}=1.8\text{V}$ , $V_{REFEN}=0.9\text{V}$ , $I_{OUT}=\pm 10\text{mA} \sim \pm 2.5\text{A}$	-20	-	20	
		$V_{IN}=1.5\text{V}$ , $V_{REFEN}=0.75\text{V}$ , $I_{OUT}=\pm 10\text{mA} \sim \pm 2.5\text{A}$	-20	-	20	
		$V_{IN}=1.2\text{V}$ , $V_{REFEN}=0.6\text{V}$ , $I_{OUT}=\pm 10\text{mA} \sim \pm 2.5\text{A}$	-20	-	20	
		$V_{IN}=1.1\text{V}$ , $V_{REFEN}=0.55\text{V}$ , $I_{OUT}=\pm 10\text{mA} \sim \pm 2.5\text{A}$	-20	-	20	



## ELECTRICAL SPECIFICATIONS (CONTINUED)

Parameter	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Protection						
Current Limit	I <sub>LIM</sub>		3	-	-	A
Thermal Shutdown Temperature	T <sub>SD</sub>	3.3V ≤ V <sub>CNTL</sub> ≤ 5V	-	150	-	°C
Thermal Shutdown Hysteresis	Δ T <sub>SD</sub>	3.3V ≤ V <sub>CNTL</sub> ≤ 5V	-	20	-	
ENABLE and Soft-Start						
REFEN Threshold	V <sub>EN</sub>		0.15	-	0.4	V
Soft-Start Interval	T <sub>SS</sub>	ΔV <sub>OUT</sub> =1V	-	0.2	-	ms

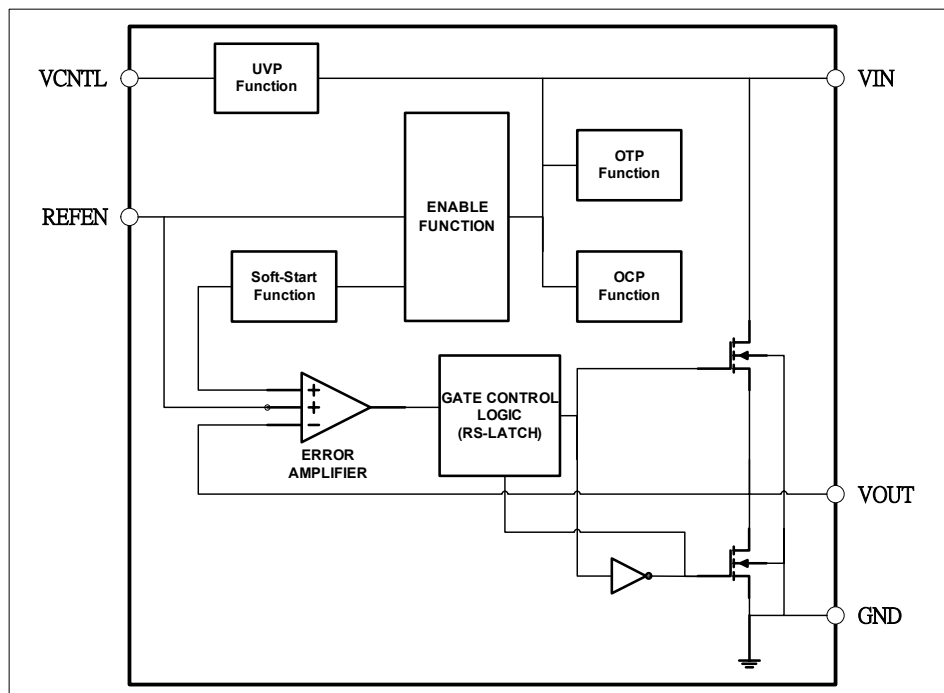
Note3.  $V_{OS}$  offset is the voltage measurement defined as  $V_{OUT}$  subtracted from  $V_{REFEN}$ .

Note4. Regulation is measured at constant junction temperature by using a 1ms(on) / 9ms(off) current pulse. Devices are tested for load regulation in the load range from 10mA to 2.5A for source and -10mA to -2.5A for sink capability.

## PIN DESCRIPTIONS

PIN SYMBOL	PIN DESCRIPTION
VIN	Power Input Voltage.
GND	Ground Pin
VOUT	Output Voltage
VCNTL	Gate Drive Voltage
REFEN	Reference Voltage Input and Chip Enable

## BLOCK DIAGRAM





## APPLICATION INFORMATION

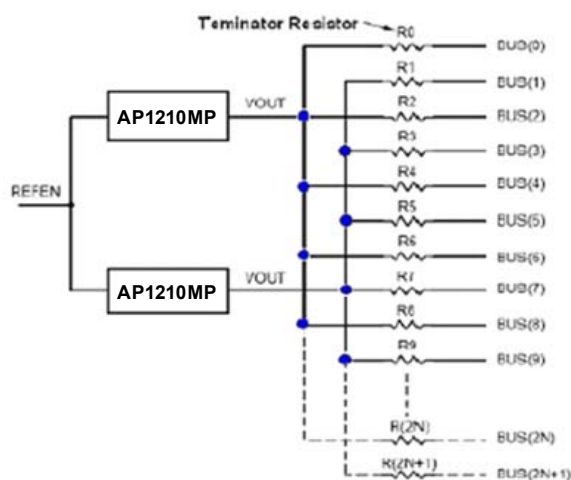
### Input Capacitor and Layout Consideration

Place the input bypass capacitor as close as possible to the AP1210MP. A low ESR capacitor larger than 470uF is recommended for the input capacitor. Use short and wide traces to minimize parasitic resistance and inductance.

Inappropriate layout may result in large parasitic inductance and cause undesired oscillation between AP1210MP and the preceding power converter.

### Consideration while designs the resistance of voltage divider

Make sure the sinking current capability of pull-down NMOS if the lower resistance was chosen so that the voltage on  $V_{REFEN}$  is below 0.15V. In addition, the capacitor and voltage divider form the lowpass filter. There are two reasons doing this design; one is for output voltage soft-start while another is for noise immunity.



### Thermal Consideration

AP1210MP regulators have internal thermal limiting circuitry designed to protect the device during overload conditions. For continued operation, do not exceed maximum operation junction temperature 125°C. The power dissipation definition in device is:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / R_{thja}$$

Where  $T_{J(MAX)}$  is the maximum operation junction temperature 125°C,  $T_A$  is the ambient temperature and the  $R_{thja}$  is the junction to ambient thermal resistance. The junction to ambient thermal resistance ( $R_{thja}$  is layout dependent) for ESOP-8 package (Exposed Pad) is 75°C/W on standard JEDEC 51-7 (4 layers, 2S2P) thermal test board. The maximum power dissipation at  $T_A = 25^\circ\text{C}$  can be calculated by following formula:

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / 75^\circ\text{C/W} = 1.33\text{W}$$

The thermal resistance  $R_{thja}$  of ESOP-8 (Exposed Pad) is determined by the package design and the PCB design. However, the package design has been decided. If possible, it's useful to increase thermal performance by the PCB design. The thermal resistance can be decreased by adding copper under the expose pad of ESOP-8 package. We have to consider the copper couldn't stretch infinitely and avoid the tin overflow



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**MARKING INFORMATION**

ESOP-8

