

## -100V P-Channel Enhancement Mode MOSFET

### Description

The AP10P10SI uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

### General Features

$V_{DS} = -100V$   $I_D = -10A$

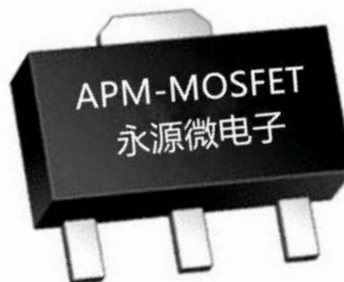
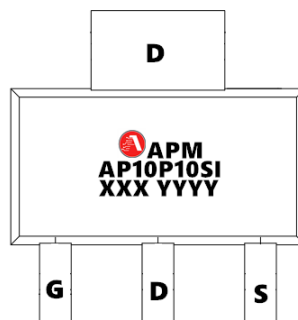
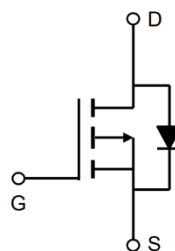
$R_{DS(ON)} < 100m\Omega$  @  $V_{GS} = 10V$  (Type: 85m $\Omega$ )

### Application

Brushless motor

Load switch

Uninterruptible power supply



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP10P10SI	SOT89-3L	AP10P10SI XXX YYYY	3000

### Absolute Maximum Ratings ( $T_C = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	-100	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-10	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-6.8	A
IDM	Pulsed Drain Current <sup>2</sup>	-60	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	80	mJ
IAS	Avalanche Current	-20	A
$P_D @ T_C = 25^\circ C$	Total Power Dissipation <sup>4</sup>	3.1	W
TSTG	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	85	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	2.6	$^\circ C/W$



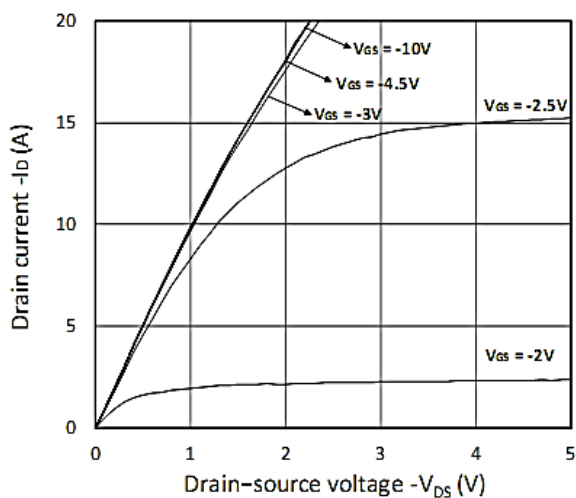
**-100V P-Channel Enhancement Mode MOSFET**
**Electrical Characteristics (T<sub>J</sub> =25 °C, unless otherwise noted)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =-250μA	-100	-110	-	V
IGSS	Gate-body Leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V	-	-	±100	nA
IDSS T <sub>J</sub> =25°C	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-100V, V <sub>GS</sub> = 0V	-	-	-1	μA
IDSS T <sub>J</sub> =100°C			-	-	-100	
VGS(th)	Gate-Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA	-1.2	-1.6	-2.5	V
RDS(on)	Drain-Source On-Resistance <sup>4</sup>	V <sub>GS</sub> = -10V, I <sub>D</sub> = -10A	-	85	100	mΩ
		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -6A	-	90	120	
gfs	Forward Transconductance <sup>4</sup>	V <sub>DS</sub> = -10V, I <sub>D</sub> = -10A	-	30	-	S
Ciss	Input Capacitance	V <sub>DS</sub> = -50V, V <sub>GS</sub> = 0V, f = 1MHz	-	3985	-	pF
Coss	Output Capacitance		-	85	-	
Crss	Reverse Transfer Capacitance		-	71	-	
Rg	Gate Resistance	f = 1MHz	-	4	-	Ω
Qg	Total Gate Charge	V <sub>GS</sub> = -10V, V <sub>DS</sub> = -50V, I <sub>D</sub> = -10A	-	65	-	nC
Qgs	Gate-Source Charge		-	10.2	-	
Qgd	Gate-Drain Charge		-	13	-	
td(on)	Turn-On Delay Time	V <sub>GS</sub> = -10V, V <sub>DD</sub> = -50V, R <sub>G</sub> = 3Ω, I <sub>D</sub> = -10A	-	12.8	-	ns
tr	Rise Time		-	30	-	
td(off)	Turn-Off Delay Time		-	82	-	
tf	Fall Time		-	61	-	
trr	Body Diode Reverse Recovery Time	I <sub>F</sub> = -10A, dI/dt = 100A/μs	-	62	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	56	-	nC
VSD	Diode Forward Voltage <sup>4</sup>	I <sub>S</sub> = -10A, V <sub>GS</sub> = 0V	-	-	-1.2	V
IS	Continuous Source Current T <sub>C</sub> = 25°C		-	-	-18	A

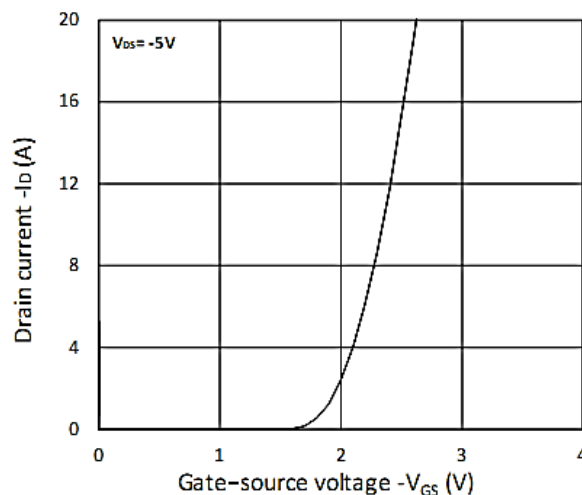
**Note :**

- 1、The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3、The EAS data shows Max. rating . The test condition is V<sub>DD</sub> = -72V, V<sub>GS</sub> = -10V, L = 0.1mH, I<sub>AS</sub> = -17A
- 4、The power dissipation is limited by 150°C junction temperature
- 5、The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub> , in real applications , should be limited by total power dissipation.

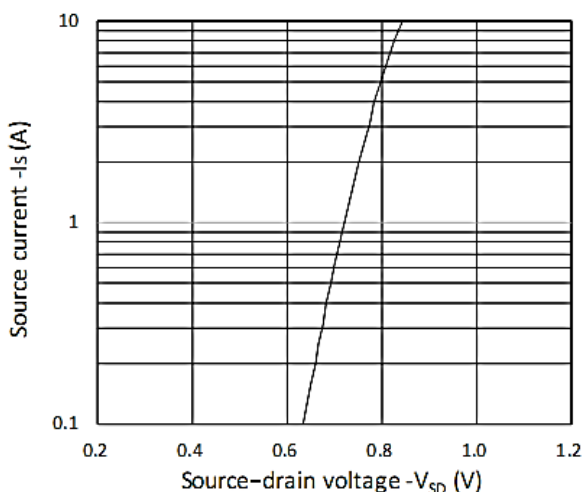
## Typical Characteristics



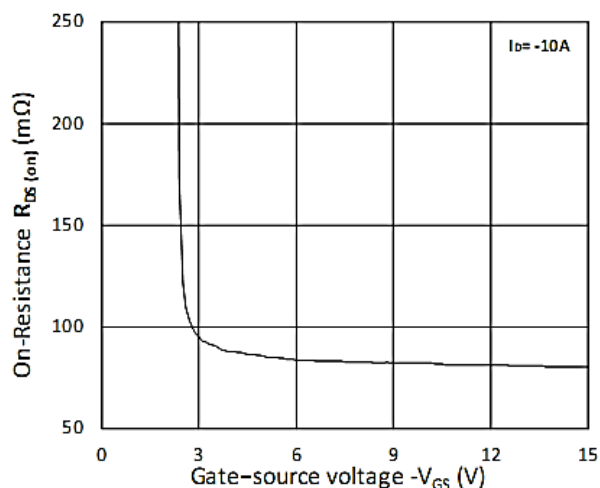
**Figure 1. Output Characteristics**



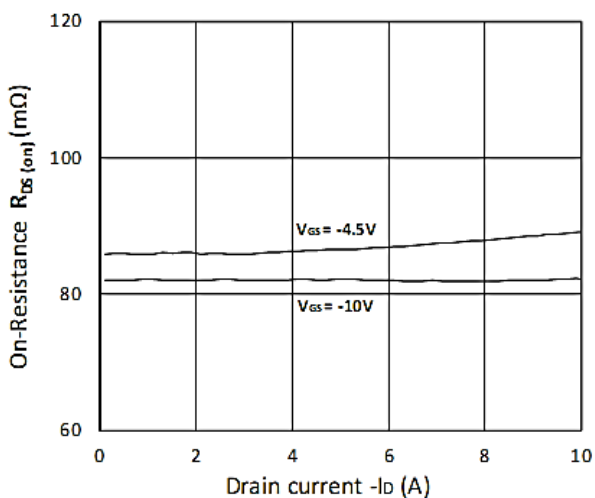
**Figure 2. Transfer Characteristics**



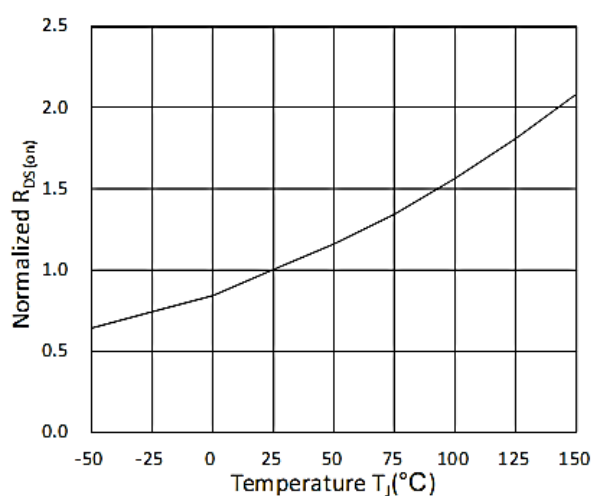
**Figure 3. Forward Characteristics of Reverse**



**Figure 4. R\_DS(on) vs. V\_GS**



**Figure 5. R\_DS(on) vs. I\_D**



**Figure 6. Normalized R\_DS(on) vs. Temperature**

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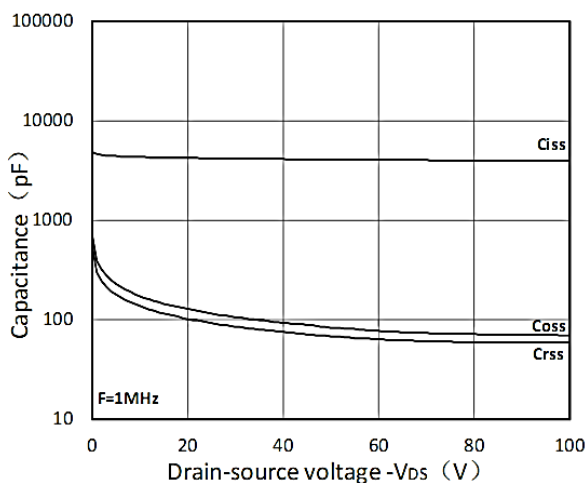


Figure 7. Capacitance Characteristics

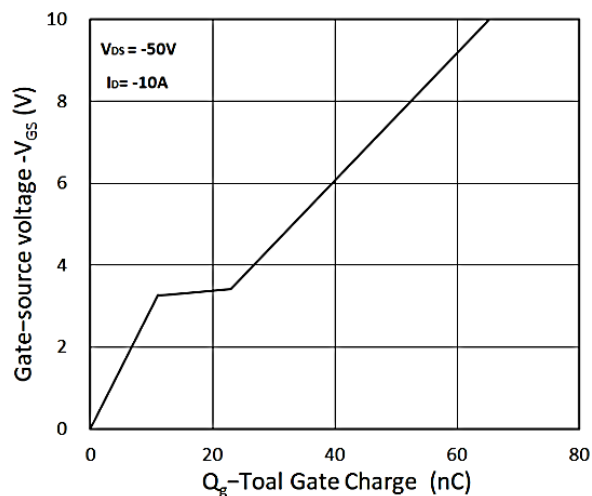


Figure 8. Gate Charge Characteristics

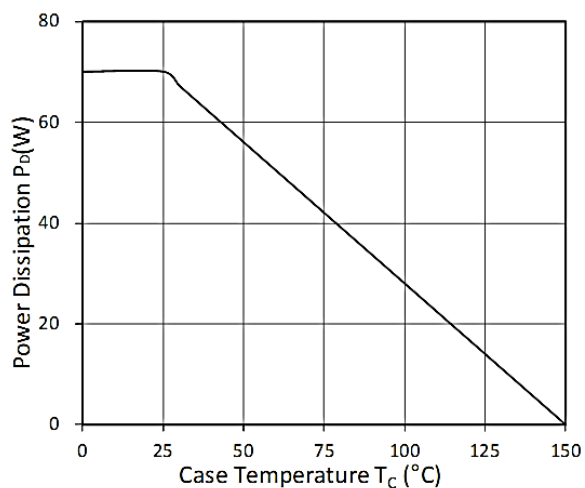


Figure 9. Power Dissipation

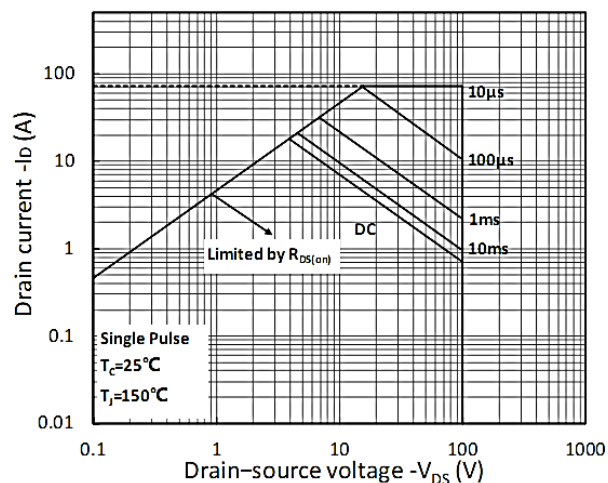


Figure 10. Safe Operating Area

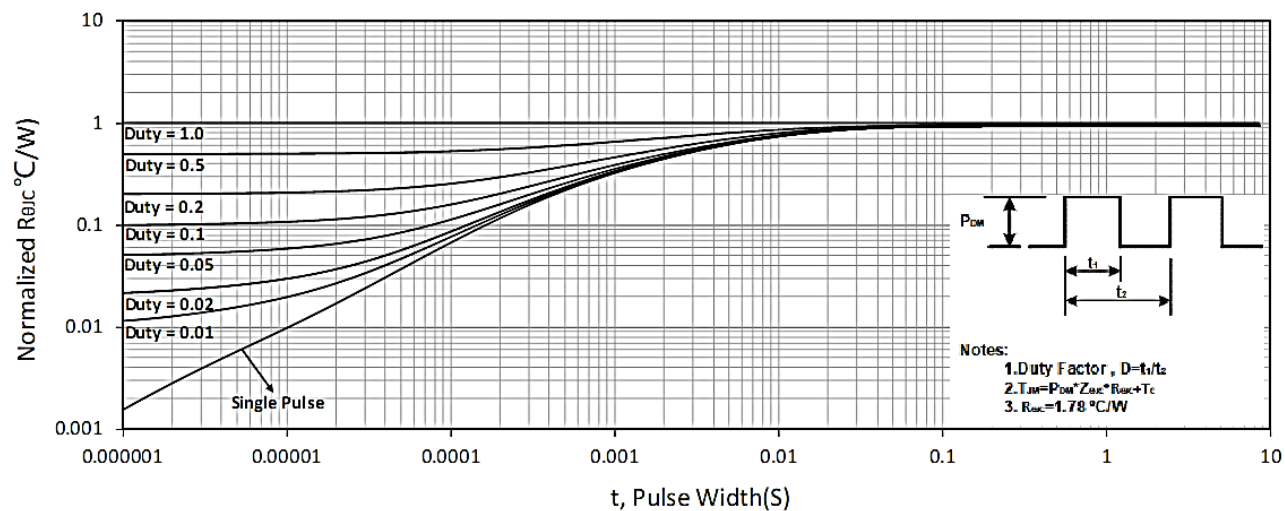
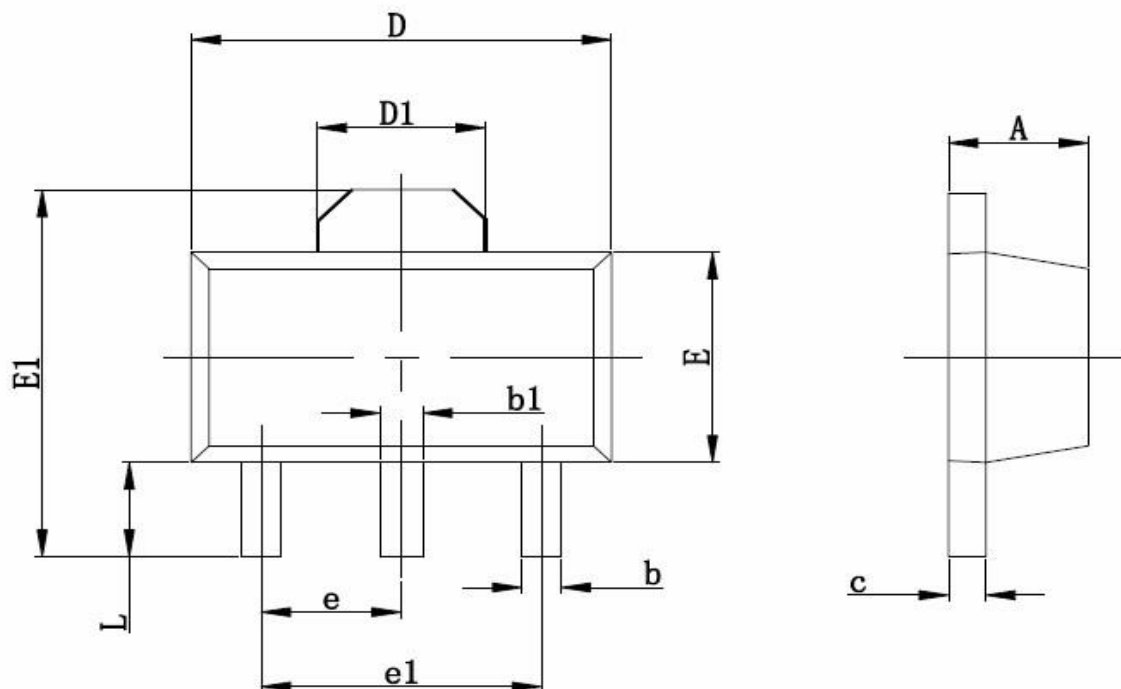


Figure 11. Normalized Maximum Transient Thermal Impedance

**Package Mechanical Data:SOT89-3L**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.400	1.600	0.055	0.063
b	0.350	0.520	0.013	0.197
b1	0.400	0.580	0.016	0.023
c	0.350	0.440	0.014	0.017
D	4.400	4.600	0.173	0.181
D1	1.550 REF		0.061 REF	
E	2.350	2.550	0.091	0.102
E1	3.940	4.250	0.155	0.167
e	1.500 TYP		0.060TYP	
e1	3.000 TYP		0.118TYP	
L	0.900	1.100	0.035	0.047

**-100V P-Channel Enhancement Mode MOSFET****Attention**

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Edition	Date	Change
REV1.0	2024/10/13	Initial release

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