AKM

AP1029ADR
32V H-Bridge DC Motor Driver IC

1.   General Description

The AP1029ADR is a 1ch H-Bridge motor driver that corresponds to an operating voltage of 32V. Four drive modes, which are forward, reverse, brake, and standby are available. An N-ch MOSFET is located at low side and a P-ch MOSFET is located at high side of the output block. The output voltage can be controlled externally or by PWM input signal. Since the AP1029ADR utilizes internal regulator outputs as control power, it can be operated by a single power supply so that external components are able to be reduced. It also features an under voltage lockout circuit, a thermal shutdown circuit and an over-current protection circuit.

2.   Features

- Operating Temperature Range   -40°C ~ 105°C
- Motor Driver Operating Voltage Range   5.5V ~ 32V
- Maximum Output Current (DC)   1.2 A (Ta=25°C)
- H-Bridge On Resistance   1.0Ω@Ta=25°C
- Switchable output voltage control function   Input Signal Control, External Voltage Control
- Built-in Start-up Function   Hard-start and Soft-start functions (selectable)
- Built-in 4.5V Output Regulator
- Anomaly Detection Output pin (FLG pin)
- Built-in Under Voltage Lockout Circuit   4.5V(typ)
- Built-in Thermal Shutdown Circuit   175°C(typ)
- Built-in Over Current Protection Circuit   1.5A(min)
- Package   16-pin QFN (3mm×3mm)

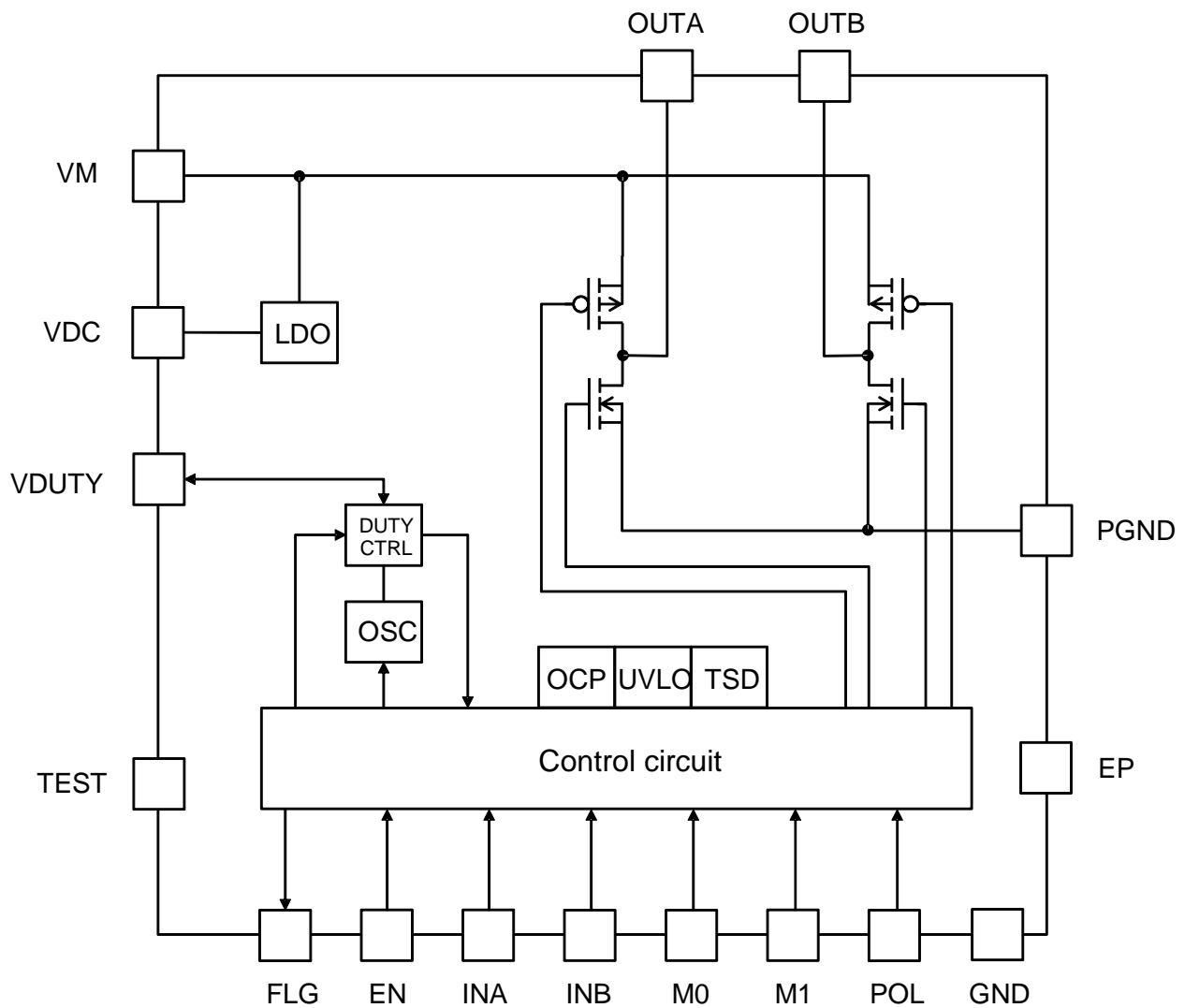## 3. Table of Contents

4. Block Diagram and Functions

Figure 1. Block Diagram

■ Functions

・ 4.5V Output LDO (LDO)
Generate a voltage of 4.5V from VM = 5.5 ~ 32V, and then output to the external terminal (VDC).

・ Oscillator(OSC)
50kHz oscillator. It is used as clock of the PWM chopper frequency.

・ VM Under Voltage Lockout (UVLO)
It is an under Voltage Lockout circuit for VM with hysteresis.

・ Thermal Shutdown (TSD)
It is an internal Thermal Shutdown detection circuit with hysteresis.

・ Over Current Protection (OCP)
It is an output stage overcurrent detection circuit for the OUTB and the OUTA pins. If the detected over current lasts for 10us, the OUTA and the OUTB become Hi-Z state for a certain period (350us) by this circuit. Hi-Z status will be released after 350us.

・ PWM Duty Control (DUTYCTRL)
It is a PWM duty circuit. It generates the PWM duty ratio that corresponds to the ratio of VM voltage and VDUTY voltage. The duty ration can be adjusted by setting the M0 and the M1 pins.

・ H-Bridge Driver
It consists of an N-ch LDMOS at low side and a P-ch LDMOS at high-side.

・ Anomaly Detection Output
FLG pin is an open drain output pin. It outputs "H" signal by connecting to an external pull-up resistor. During normal operation, it outputs "L". During standby state, overheat detection (TSD), over-current detection (OCP) or VM low voltage detection (UVLO) operation, it outputs "H" signal.
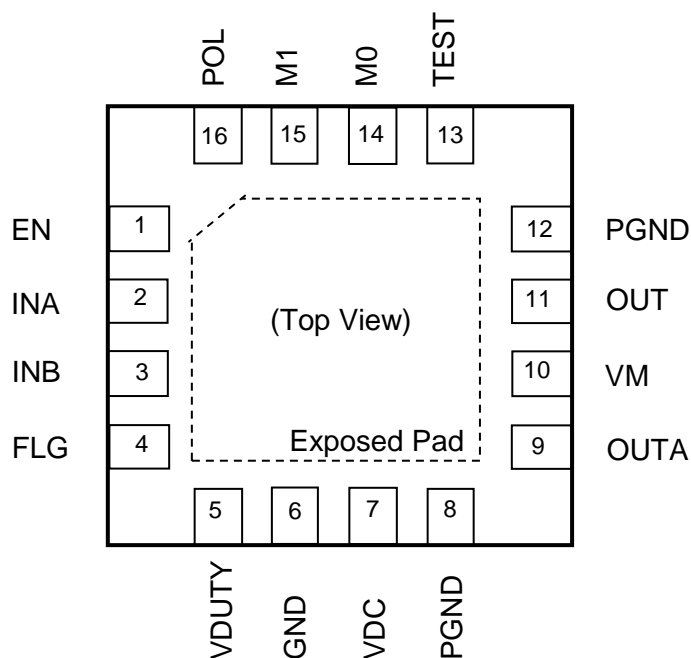
5.	Ordering Guide

AP1029ADR   -40°C ～+105°C   16-pin QFN

6. Pin Configurations and Functions

■ Pin Configurations

(Top View)

Exposed Pad

■ Functions

Pin Number	Name	I/O (Note 1)	Function	Condition
1	EN	I	Enable signal input	200kΩ Pull-down
2	INA	I	Control signal input	200kΩ Pull-down
3	INB	I	Control signal input	200kΩ Pull-down
4	FLG	O	Flag Output	N-ch open-drain output
5	VDUTY	I/O	Output Duty Setting	
6	GND	P	Ground	
7	VDC	O	Internal 4.5V regulator output	
8	PGND	P	Power GND	(Note 2)
9	OUTA	O	Motor driver output	
10	VM	P	Motor driver power supply	
11	OUTB	O	Motor driver output	
12	PGND	P	Power GND	
13	TEST	I	TEST Pin	(Note 2)
14	M0	I	Output ratio Control	200kΩ Pull-up
15	M1	I	Output ratio Control	200kΩ Pull-up
16	POL	I	Soft Start polarity	200kΩ Pull-up
Exposed Pad	EP	P	Heat Dissipation	(Note 2)

Note 1. I(Input pin), O(Output pin), P(Power pin), I/O(Input / Output pin)
Note 2. The exposed pad must be connected to GND.
Note 3. Let M0, M1, POL pin open or connect VDC pin when make their signals "H".

7. Absolute Maximum Ratings

Parameter	Symbol	min	max	Unit	Condition
Motor Power Supply Voltage	VM	-0.5	40	V	
VDC, EN, INA, INB, FLG Terminal	Vterm1	-0.5	5.5	V	
POL, VDUTY, M0, M1 Terminal	Vterm2	-0.5	VDC+0.5	V	VDC+0.5$\leqq$5.5V
VM Level Terminal (OUTA, OUTB)	Vterm3	-0.5	VM+V_F	V	VM+$V_F$$\leqq$40V
GND-PGND Between	-	-0.3	0.3	V	
Output Current	Iload	-	1.2	A	OUTA、OUTB
Power Dissipation	PD	-	2	W	Ta=25°C (Note 5)
		-	0.75	W	Ta=105°C (Note 5)
Junction Temperature	Tj	-	150	°C	
Storage Temperature	Tstg	-50	150	°C	

Note 4. All above voltages are with respect to GND=PGND=0V. GND and PGND must be connected to a ground plane.

Note 5. The rating calculated by θJA=60°C /W. The exposed pad must be connected to ground. The exposed pad must be connected to GND.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.
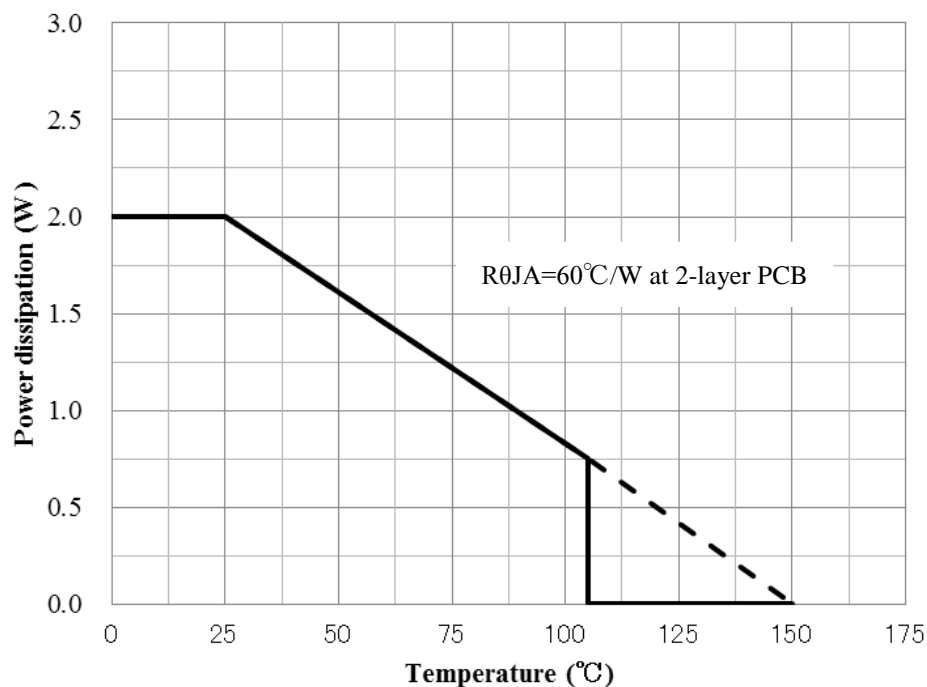

RθJA=60°C/W at 2-layer PCB

Figure 2. Maximum Power Dissipation

8. Recommended Operating Conditions

Parameter	Symbol	min	typ	Max	Unit	Condition
Motor Driver Supply Voltage	VM	5.5	12.0	32.0	V	
Input Frequency Range	Fin	-	-	200	kHz	M0=M1="H"
Operating Temperature Range	Ta	-40	-	105	°C	
VDUTY Input Voltage Range	V_{DUTY}	0.5	-	4.0	V	

Note 6. All above voltages are with respect to GND=PGND=0V.

9. Electrical Characteristics

(Ta = -40~105°C, VM=5.5~32V, unless otherwise specified.)

Parameter	Symbol	Condition	min	typ	max	Unit
Quiescent Current						
VM Quiescent Current at Power-OFF	I_{VMOFF}	EN= "L"	-	-	10	uA
VM Input Current at Operation	I_{VM}	EN= "H"	-	1.7	2.6	mA
H-Bridge Circuit						
Driver On Resistance (High Side＋Low Side)	R_{ON1}	$I_{load}=\pm100mA$, Ta=25°C	-	0.8	1.5	Ω
Driver On Resistance (High Side＋Low Side)	R_{ON2}	Iload=±1.0A, Ta=25°C	-	1.0	1.5	Ω
Driver On Resistance (High Side＋Low Side)	R_{ON3}	$I_{load}=\pm100mA$	-	0.8	1.5	Ω
Body Diode Forward Voltage	V_F	I_F=100mA	-	0.8	1.2	V
PWM Chopper Frequency	f_{PWM}	M0=M1= "L" (Note 7)	25	50	95	kHz
H-Bridge Output Delay Time ("L"→"H")	t_{PDLHHB}	tr=tf=10ns (Note 8)	-	-	1.0	us
H-Bridge Output Delay Time ("H"→"L")	t_{PDHLHB}	tr=tf=10ns (Note 8)	-	-	1.0	us
H-Bridge Output Pulse Width	t_{PWOHB}	M0=M1= "H", INA=200kHz, PWL=1us, tr=tf=10ns	0.6	0.9	-	us
Output Duty Ratio 1	D_{UTY1}	VM=12V, VDUTY=1.5V M0=M1= "L"	20	25	30	%
Output Duty Ratio 2	D_{UTY2}	VM=12V, VDUTY=1.5V M0= "H", M1= "L"	40	50	60	%
Output Duty Ratio 3	D_{UTY3}	VM=12V, VDUTY=1.5V M0= "L", M1= "H"	80	-	-	%

Parameter	Symbol	Condition	min	typ	max	Unit
4.5V Output Regulator						
Internal Regulator Output Voltage	V_{DC}	I_{DC}=0.1mA	4.0	4.5	5.0	V
Control Logic						
Input High Level Voltage	V_{IH}		2.0	-	-	V
Input Low Level Voltage	V_{IL}		-	-	0.8	V
Input Pulse Rise Time	t_R	M0=M1= "H"	-	-	1.0	us
Input Pulse Fall Time	t_F	M0=M1= "H"	-	-	1.0	us
Input High Level Current (EN, INA, INB)	I_{IH1}	V_{IH}=3.0V	7.5	15	30	uA
Input High Level Current (M0, M1, POL)	I_{IH1}	V_{IH}=VDC	-1	-	1	uA
Input Low Level Current (EN, INA, INB)	I_{IL2}	V_{IL}=0V	-1	-	1	uA
Input Low Level Current (M0, M1, POL)	I_{IL2}	VDC=4.5V, V_{IL}=0V	11.25	22.5	45	uA
Output High Level Voltage(VDUTY)	V_{OH}	INA=INB="L", POL="H", M1="L" or M0="L", Io=-1mA	VDC-0.4	-	-	V
Output Low Level Voltage(VDUTY)	V_{OL}	INA=INB="L", POL="L", M1="L" or M0= "L", Io=+1mA	-	-	0.4	V
FLG-On Resistance	R_{ONFLG}	Io=+1mA	-	-	500	Ω
Protection Circuit						
VM Under Voltage Detect Voltage	VM_{UV}		4.0	4.5	5.0	V
Thermal Shutdown Temperature	T_{TSD}	(Note 9)	150	175	200	°C
Temperature Hysteresis	T_{TSDHYS}	(Note 9)	-	30	-	°C
Over Current Protection	I_{OCP}		1.5	-	-	A

Note 7. Refer to Figure 4.
Note 8. Refer to Figure 3.
Note 9. Not tested in production.

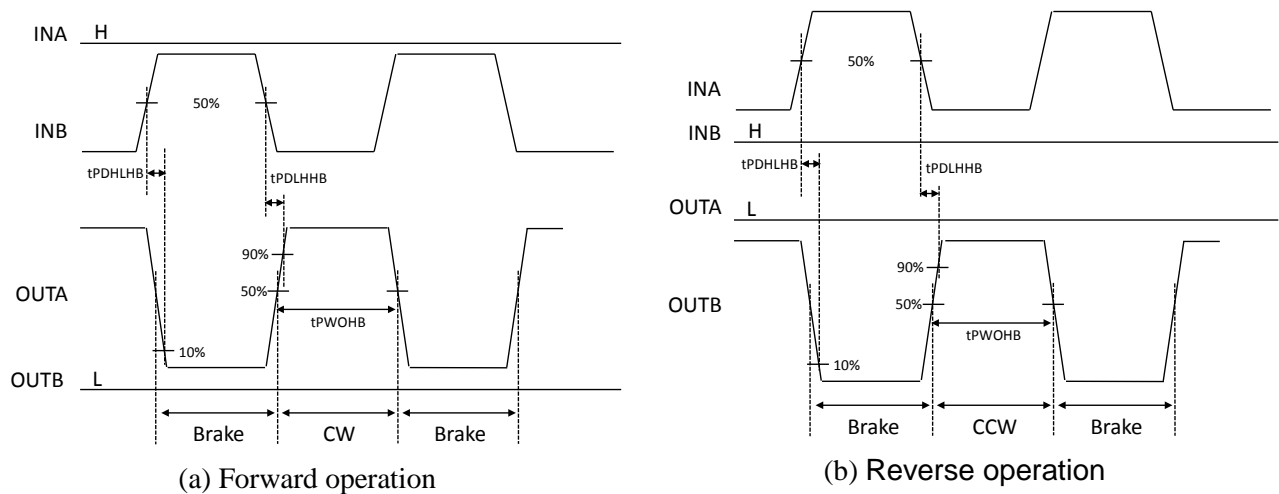(a) Forward operation

(b) Reverse operation

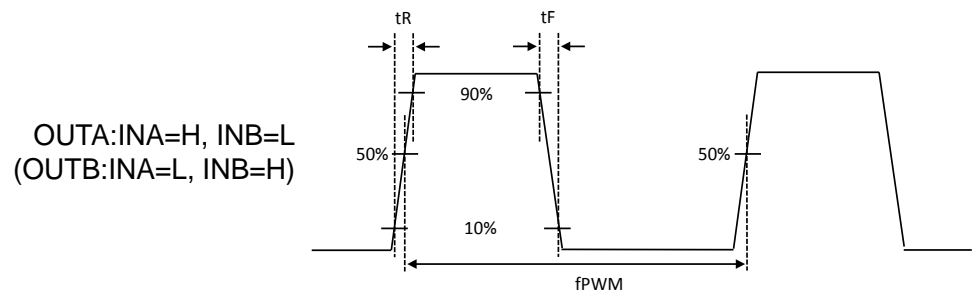Figure 3. Output delay time timing chart (EN="H")

Figure 4. Output Rise /Fall Timing Chart (PWM Control Mode, EN="H")

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10. Functional Descriptions

10.1 Output Voltage

Output voltage (Vout), is controlled by the PWM control mode that depends on the external reference voltage input to the VDUTY pin. However, Vout never exceeds VM. Vout is affected by on-resistance, load current and etc. under loaded condition.

$$Vout = VDUTY \times N \quad \text{(under no-load condition)}$$

"N" is set by the M1 and the M0 pins as follows. However, in the case of M0 pin = M1 pin = "H", the AP1029ADR will not be in PWM control mode but be in Input control mode according to the INA and the INB inputs. Start-up function does not work at this time. When the AP1029ADR is used in input control mode, make sure that the VDUTY pin and the POL pin are Open.

For example, Vout will be 3V by setting M1 = M0 pins = "L" when VDUTY is 1.5V, and It will be 6V by setting M0 = "H" and M1 = "L" when VDUTY is 1.5V.

Table 1. Output Voltage Setting Table

M1	M0	Mode of operation	Start-up function
L	L	N=2、PWM control mode	On
L	H	N=4、PWM control mode	On
H	L	N=8、PWM control mode	On
H	H	Input control mode (INA and INB Inputs response operation)	Off

10.2 Control Logic

The relationship between the input and output of each mode are shown below.

Table 2. Truth Table

Input			Output		Function
EN	INA	INB	OUTA	OUTB	
H	L	L	Hi-Z	Hi-Z	Standby(idle)
H	L	H	L	H(PWM)	Reverse
H	H	L	H(PWM)	L	Forward
H	H	H	L	L	Brake(stop)
L	-	-	Hi-Z	Hi-Z	Stop

Note 10. See Figure 8 and Figure 9 for timing chart of Standby and Stop. See Figure 3 for timing chart of Brake.

10.3 Start-up Function

The AP1029ADR has a start-up function. The VDUTY pin is used to set the Duty of the PWM control mode. In addition, by connecting the RDT1 and the RDT2 capacitances and the CDT resistance as shown in Figure 5, the AP1029ADR will execute a start-up operation. Start-up operation can be switched by setting the POL pin. Hard-start operation will be executed when the POL pin = "L" and Soft-start operation will be executed when the POL pin = "H".

Hard-start operation is for the situation when motor torque is needed at start-up.
Soft-start operation is for the situation when motor needs to rotate slowly at start-up.

Start-up function works in the following cases.
① INA or INB becomes "H" from standby mode. (Note that the initial mode should be standby, not brake.)
② the IC recovers from protection status.

Table 3. Start-up settings

INA	INB	POL	VDUTY pin status
L	L	L	H（Duty=100%）
L	L	H	L（Duty=0%）
H	-	-	Hi-Z
-	H	-	Hi-Z

How to use start-up function is shown below.

When the POL pin= "L", the EN pin= "H" and the INA = INB pins = "L", High side of the VDUTY pin output (MP1) is turned on, therefore the external capacitor (CDT) is charged by the VDC voltage. High side of the VDUTY pin output (MP1) will be turned off and capacity of the CDT is discharged by the RDT2 external resistor if INA = INB ≠ "L" is input, and then hard-start operation is executed. The VDUTY pin voltage is determined and stabilized by the RDT1 and the RDT2 external resistors. (Refer to Figure 6)
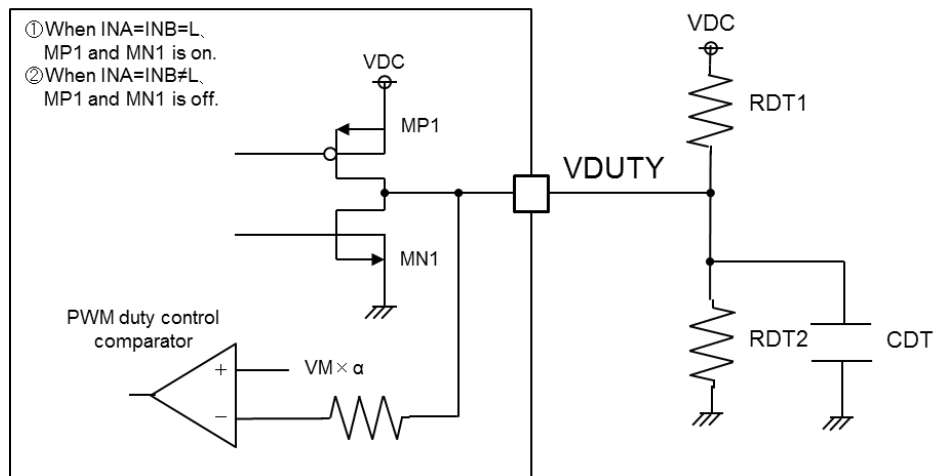

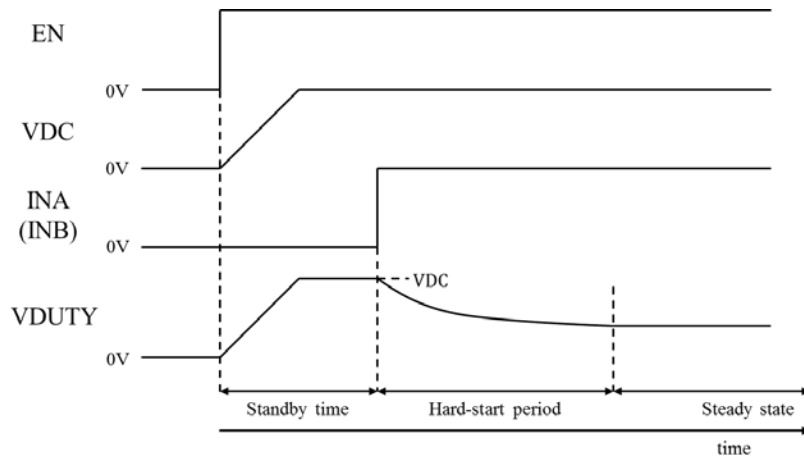Figure 5. Start-up Circuit Example

Figure 6. Start-up Operation Example (Hard Start: POL = "L", pull-up power supply = VDC)
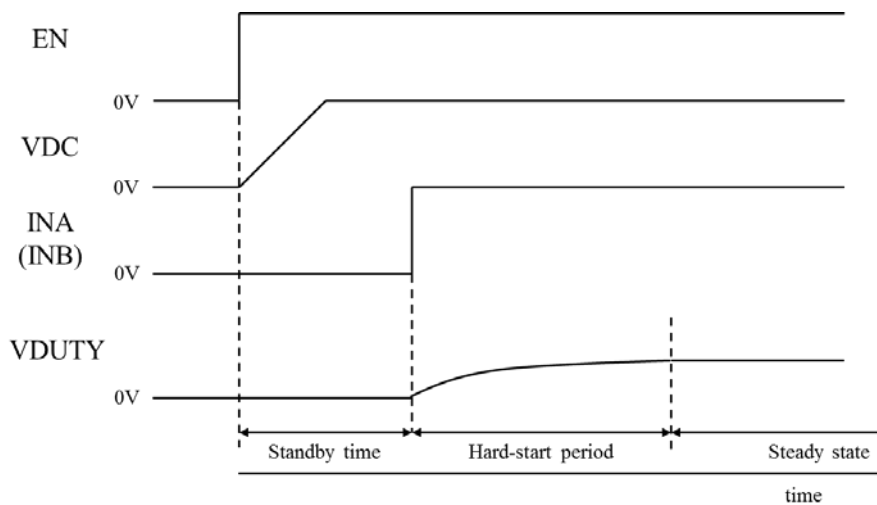

Figure 7. Start-up Operation Example (Soft-Start: POL = "H", pull-up power supply = VDC)

VDUTY voltage after certain time(t) can be calculated as follows.

Soft-start :

$$VDUTY(V) = VDC - \frac{RDT1*VDC}{RDT1+RDT2}\left(1 + \frac{RDT2}{RDT1}\exp\left(-\frac{RDT1+RDT2}{CDT*RDT1*RDT2}*t\right)\right)$$

Hard-start :

$$VDUTY(V) = \frac{RDT2*VDC}{RDT1+RDT2}\left(1 + \frac{RDT1}{RDT2}\exp\left(-\frac{RDT1+RDT2}{CDT*RDT1*RDT2}*t\right)\right)$$

Sample Calculation:

(Condition; VDC=4.5V, RDT1=RDT2=1MΩ, CDT=1nF)

    VDUTY after 500us

        In case of Soft start : 1.422V

        In case of Hard start : 3.078V

    VDUTY after 5ms

        In case of Soft start : 2.250V

        In case of Hard start : 2.250V

10.4 Operation Description After Enable Input Level Trasition

4.5V LDO output will rise by applying a 5.5V voltage or more to the VM pin and setting the EN pin = "H". Input the INA and the INB signals 3ms (t1 period) after the EN pin = "H", waiting for the stabilization of the VDC output. After the certain stabilization time of VDC output (t1 period), The IC becomes Stanby and INA and INB input become valid. Figure 8 is timing chart from VM power supply to INA, INB input is valid.

When using start-up function, stabilization time may take more than 3ms depends on the value of the external resistance and capacitor connected to the VDUTY pin. In this case, input timing of INA and INB should be after stabilization of VDUTY pin voltage.

4.5V LDO output stops after inputting "L" to EN pin. Within 100ms(t2 period), OUTA and OUTB become Hi-Z(Stop). Do not change input levels of INA and INB, because OUTA and OUTB changes according to input level of INA and INB during t2 period. Figure 9 is timing chart from IN="H" becomes "L" to OUTA=OUTB = Hi-Z.
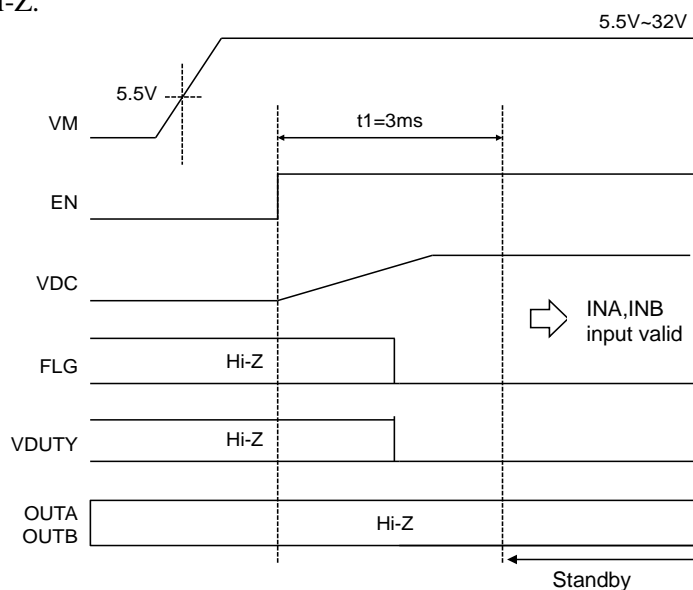

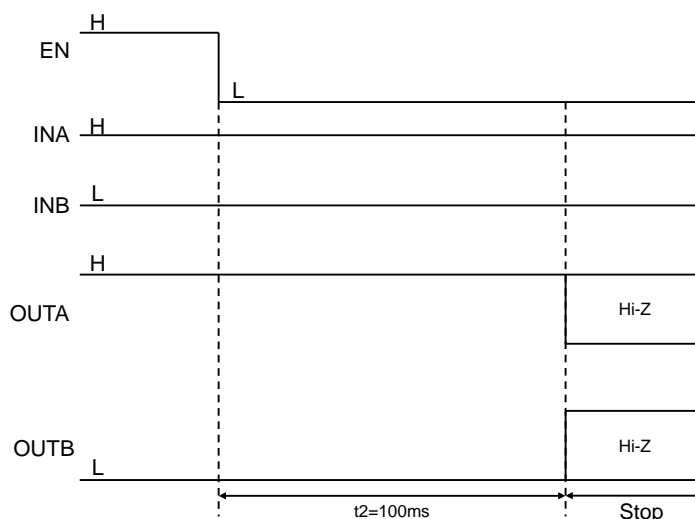
Figure 8. Timing Chart of EN voltage input after power-up

Figure 9. Timing Chart from EN="H" becomes "L" to OUTA= OUTB=Hi-Z

10.5 Protection Circuits

·   VM Under Voltage Lockout

The OUTA and the OUTB outputs are set to Hi-Z state when the VM voltage becomes 4.5V (typ) or less to prevent malfunction of the IC. The FLG pin becomes Hi-Z state at the same time.

·   Thermal Shutdown

When an abnormal high temperature 175°C (typ) is detected, the OUTA and the OUTB outputs are set to Hi-z state to prevent getting damages by self-heating. The internal 4.5V LDO is stopped and the FLG pin becomes Hi-Z state at the same time. The AP1029ADR restarts when the temperature drops to under 145°C (typ).

·   Over Current protection

The AP1029ADR integrates an over current protection circuit that protects the device from damages caused by output short of H-bridge driver, short-to-ground and short-to-supply. When a MOSFET current more than 1.5A lasts for 10us, the OUTA and the OUTB outputs are set to Hi-Z state for 350us. The FLG pin becomes Hi-Z state at the same time. After 350us, the AP1029ADR returns to normal operation automatically.
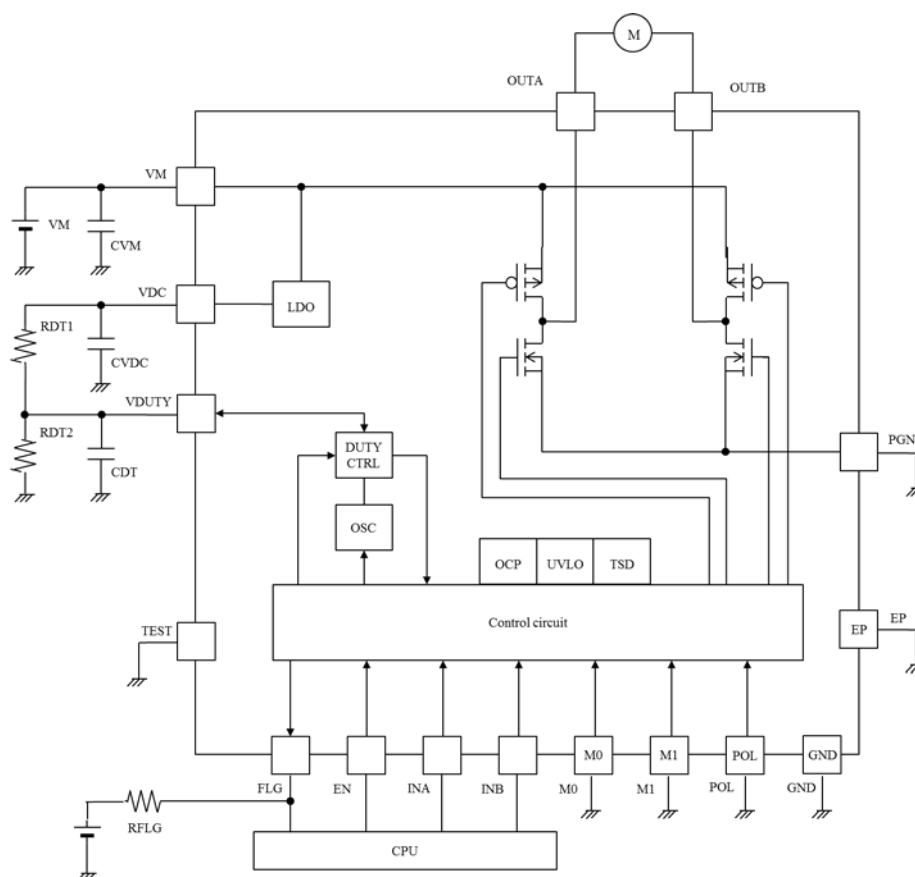
11. Recommended External Circuits

Figure 10. Recommended External Circuit

Table 4. Recommended External Components

Item	min	typ	max	Unit	Note
CVM	-	1.0	-	μF	Ceramic Capacitor
	-	47	-	μF	Electrolytic Capacitor
CVDC	-	1.0	-	μF	Ceramic Capacitor
RDT1	-	0.2	-	MΩ	(Note 11)
RDT2	-	0.1	-	MΩ	(Note 11)
RFLG	-	1.0	-	MΩ	
CDT	-	100	-	nF	

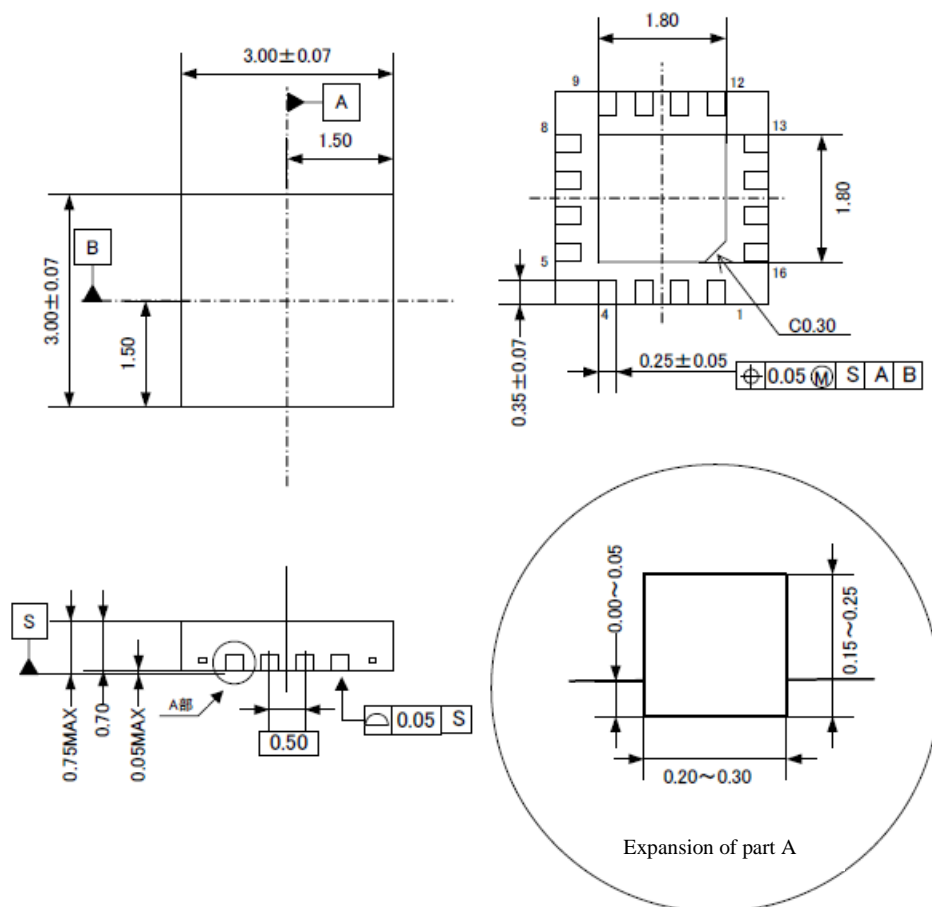Note 11. RDT1+RDT2 must be 100kΩ or more.
Note 12. Above values are examples. Please choose appropriate external components for your system board.
Note 13. Connection capacitance of CVM and CVC should be determined in consideration of the load
current profile, the load capacitance, the line resistance and etc. of the actual system board.
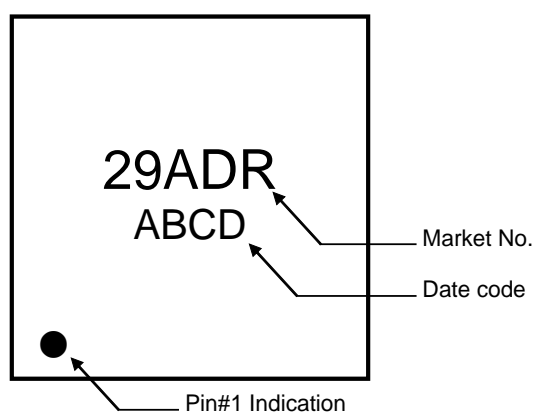Note 14. Use resistive divider in case external voltage is applied to the VDUTY pin.

12. Package

■ Outline Dimensions

3.00±0.07
1.50
3.00±0.07
1.50

1.80
1.80
0.35±0.07
0.25±0.05
C0.30
⊕ 0.05 Ⓜ S A B

S
0.75MAX
0.70
0.05MAX
A部
0.50
⌒ 0.05 S

0.00~0.05
0.15~0.25
0.20~0.30

Expansion of part A

■ Marking

29ADR
ABCD
Market No.
Date code
Pin#1 Indication

A   : Year code (Last 1 digit)
B,C   : Week code
D   : Management code

13. Revise History

Date (YY/MM/DD)	Revision	Page	Contents
17/01/13	00	-	First Edition

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