



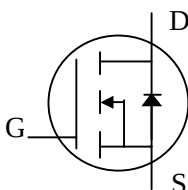
N-channel Enhancement-mode Power MOSFET

Simple Drive Requirement

SO-8 Compatible with Heatsink

Low On-resistance

RoHS-compliant, halogen-free

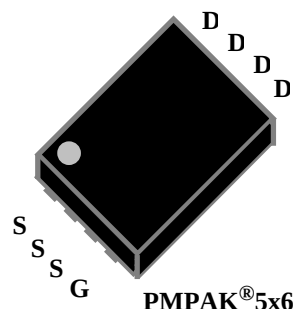


BV_{DSS}	30V
$R_{DS(ON)}$	5.5m Ω
I_D	70A

Description

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The PMPAK[®]5x6 package is specially designed for DC-DC converter applications, with a foot print that is compatible with the popular SO-8 and offers a backside heat sink and lower package profile.



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D at $T_C=25^\circ\text{C}$	Continuous Drain Current (Chip)	70	A
I_D at $T_A=25^\circ\text{C}$	Continuous Drain Current ³	24	A
I_D at $T_A=70^\circ\text{C}$	Continuous Drain Current ³	19	A
I_{DM}	Pulsed Drain Current ¹	250	A
P_D at $T_C=25^\circ\text{C}$	Total Power Dissipation	44.6	W
P_D at $T_A=25^\circ\text{C}$	Total Power Dissipation	5	W
E_{AS}	Single Pulse Avalanche Energy ⁴	28.8	mJ
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Maximum Thermal Resistance, Junction-case	2.8	$^\circ\text{C/W}$
Rthj-a	Maximum Thermal Resistance, Junction-ambient ³	25	$^\circ\text{C/W}$

Ordering Information

AP0503GMT-HF-3TR

RoHS-compliant halogen-free PMPAK[®]5x6, shipped on tape
and reel (3000pcs/reel)

PMPAK[®] is a registered trademark of Advanced Power Electronics Corp.



Electrical Specifications at $T_j=25^{\circ}\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=30A$	-	-	5.5	m Ω
		$V_{GS}=4.5V, I_D=20A$	-	-	10.5	m Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1	-	3	V
g_{fs}	Forward Transconductance	$V_{DS}=10V, I_D=20A$	-	50	-	S
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=30V, V_{GS}=0V$	-	-	1	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Q_g	Total Gate Charge ²	$I_D=30A$	-	9.2	15	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=24V$	-	2.5	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{GS}=4.5V$	-	5.7	-	nC
$t_{d(on)}$	Turn-on Delay Time ²	$V_{DS}=15V$	-	7.5	-	ns
t_r	Rise Time	$I_D=30A$	-	80	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega, V_{GS}=10V$	-	18	-	ns
t_f	Fall Time	$R_D=0.5\Omega$	-	5	-	ns
C_{iss}	Input Capacitance	$V_{GS}=0V$	-	930	1500	pF
C_{oss}	Output Capacitance	$V_{DS}=25V$	-	280	-	pF
C_{rss}	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	100	-	pF
R_g	Gate Resistance	$f=1.0\text{MHz}$	-	1.5	2.3	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$I_S=30A, V_{GS}=0V$	-	-	1.2	V
t_{rr}	Reverse Recovery Time ²	$I_S=10A, V_{GS}=0V,$	-	47	-	ns
Q_{rr}	Reverse Recovery Charge	$dI/dt=100A/\mu s$	-	57	-	nC

Notes:

1. Pulse width limited by maximum junction temperature
2. Pulse test
3. Surface mounted on 1 in² copper pad of FR4 board, $t \leq 10\text{sec}$, 60°C/W at steady state.
4. Starting $T_j=25^{\circ}\text{C}$, $V_{DD}=25V$, $L=0.1\text{mH}$, $R_G=25\Omega$, $I_{AS}=24A$.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

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Typical Electrical Characteristics

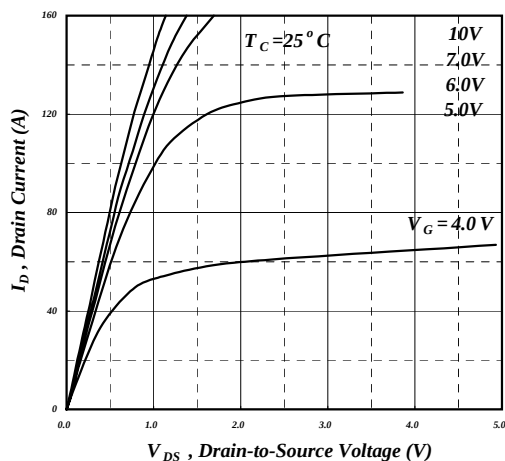


Fig 1. Typical Output Characteristics

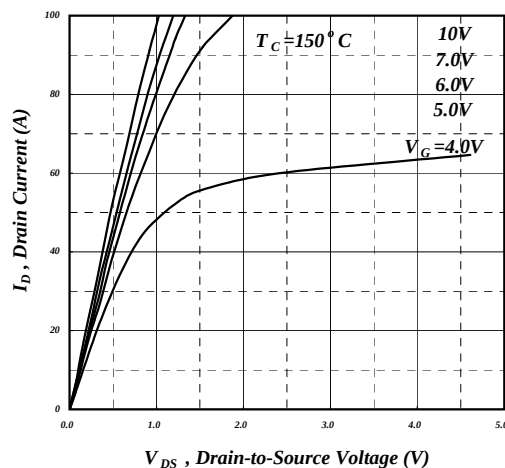


Fig 2. Typical Output Characteristics

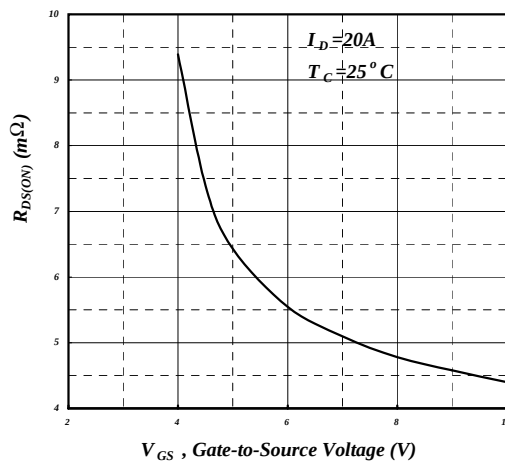


Fig 3. On-Resistance vs. Gate Voltage

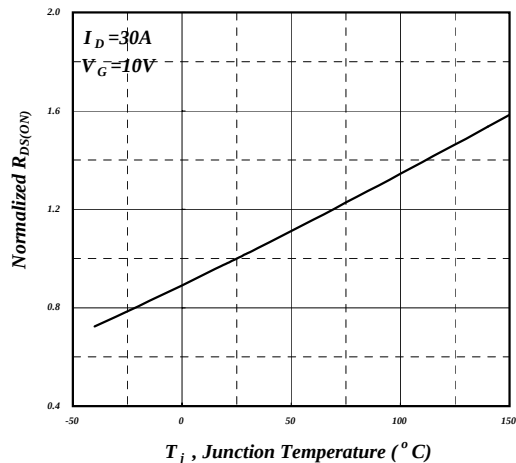


Fig 4. Normalized On-Resistance
vs. Junction Temperature

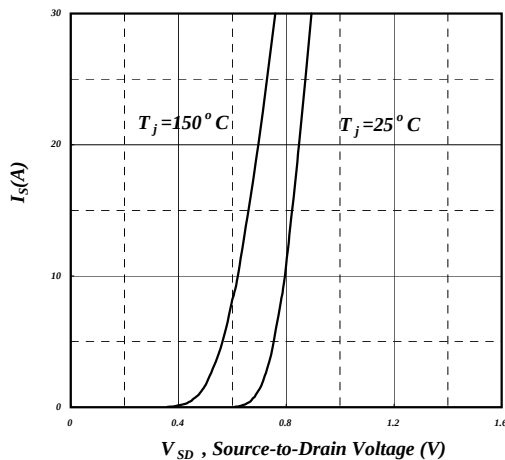


Fig 5. Forward Characteristic of
Reverse Diode

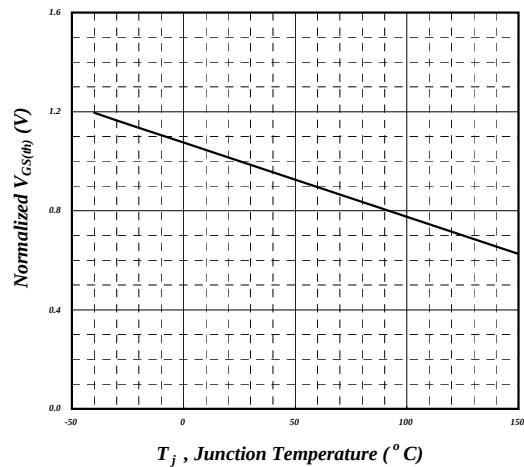


Fig 6. Gate Threshold Voltage vs.
Junction Temperature



Typical Electrical Characteristics (cont.)

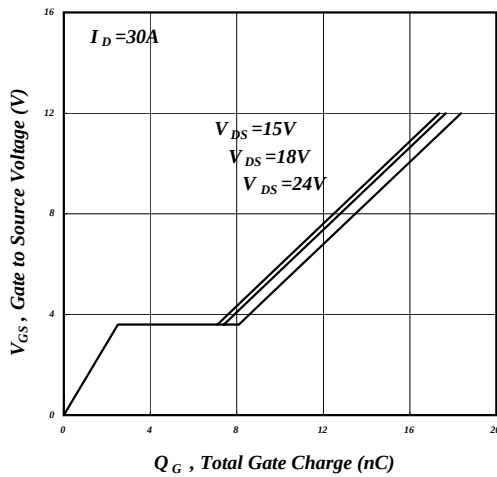


Fig 7. Gate Charge Characteristics

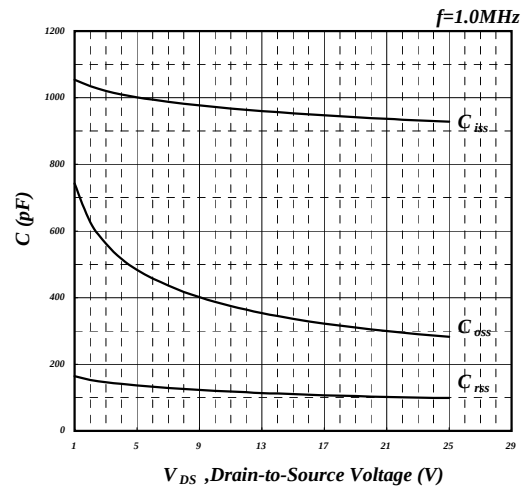


Fig 8. Typical Capacitance Characteristics

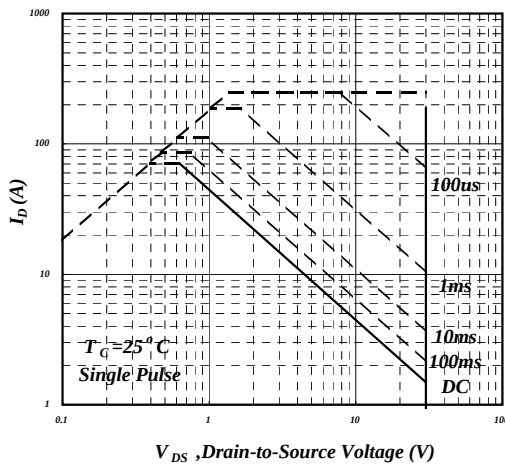


Fig 9. Maximum Safe Operating Area

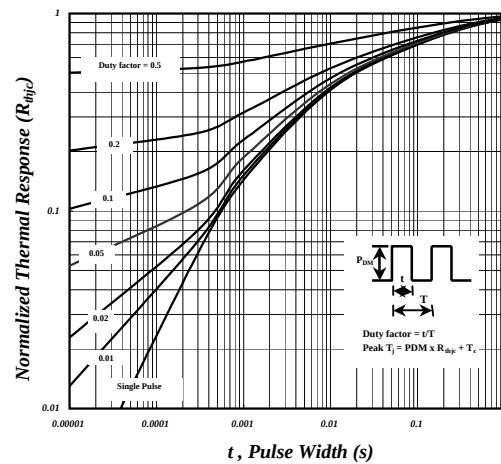


Fig 10. Effective Transient Thermal Impedance

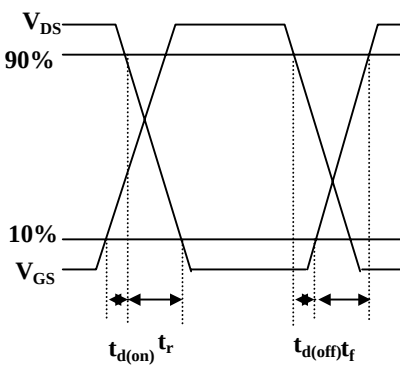


Fig 11. Switching Time Waveforms

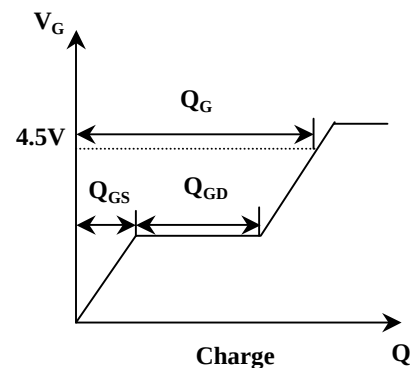
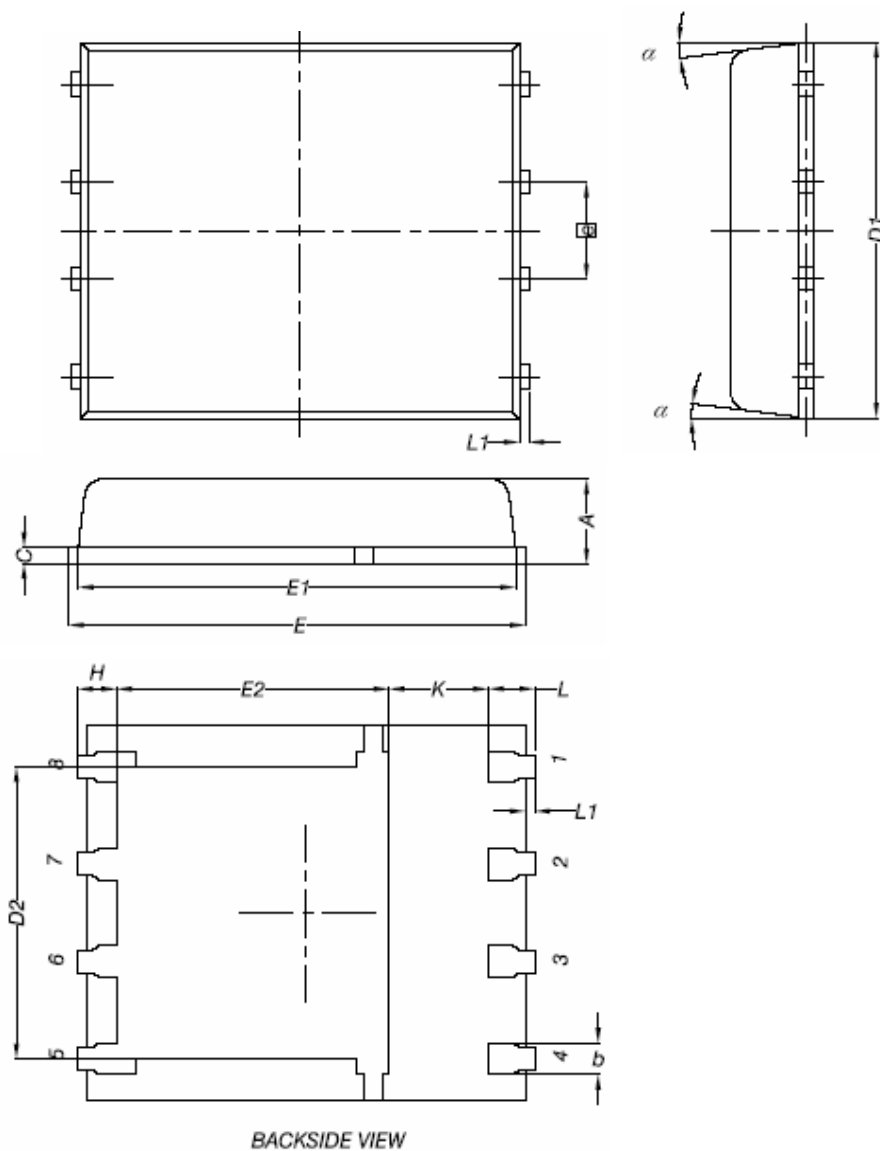


Fig 12. Gate Charge Waveform



Package Dimensions: PMPAK[®]5x6



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	0.90	1.00	1.10
b	0.33	0.41	0.51
C	0.20	-	-
D1	4.80	4.90	5.10
D2	-	-	4.20
E	5.90	6.00	6.10
E1 (Reference)	5.70	5.75	5.80
E2 (Reference)	3.38	3.58	3.78
e	1.27 BSC		
H	-	-	0.62
K (Reference)	0.70	-	-
L	0.51	0.61	0.71
L1	-	-	0.20
α (Reference)	0°	-	12°

1. All dimensions are in millimeters.
2. Dimensions do not include mold protrusions.

Marking Information:

