ALPHA & OMEGA SEMICONDUCTOR

AOZ59141DI

40V MOSFET Driver for Synchronous Buck Converter

General Description

AOZ59141DI is a 40V high efficiency synchronous buck dual MOSFET driver to drive two n-channel MOSFET for both High-Side and Low-Side. The driver is optimized for operation in the synchronous buck configuration. The driver for Low-Side MOSFET can deliver up to 4A sinking current, capable to hold the Low-Side gate off even at high transient dv/dt.

The driver features Tri-State PWM and FCCM outputs for accurate control of the power MOSFETs switching activities. It is compatible with 5V (CMOS) logic and supports Tri-State PWM.

A number of features are provided making the AOZ59141DI a highly versatile driver for CPU power supply application. A bootstrap switch is integrated in the driver. The Low-Side MOSFET can be driven into diode emulation mode to provide asynchronous operation and improve light-load performance.

Features

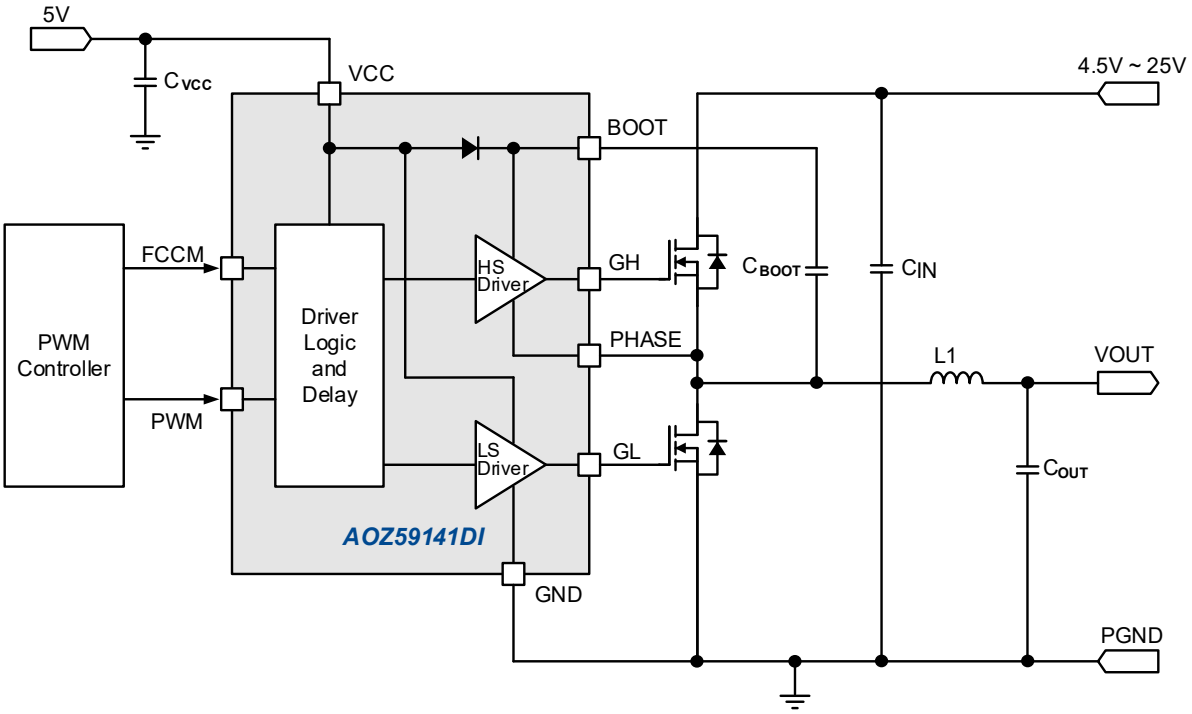
- 4.5V to 5.5V input supply range
- Up to 40V BOOT supply voltage
- Dual drivers for N-channel high-side and low-side MOSFET
- Up to 2 MHz switching operation
- 5V PWM/tri-state input compatible
- 4A Low-side driver sinking capability
- Under-voltage lockout protection
- FCCM signal pin control for diode emulation /CCM operation
- Standard 2 mm x 2 mm DFN-8L package

Applications

- CPU core power supplies
- Point of load DC/DC converters

Green Product

Typical Application

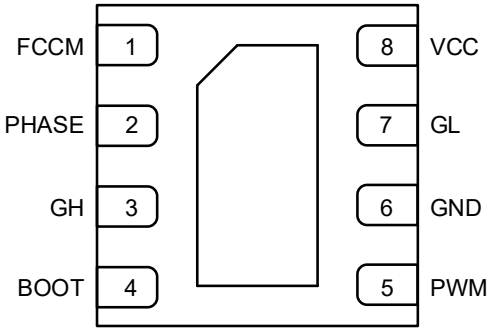


Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ59141DI	-40 °C to +125 °C	DFN2x2-8L	RoHS

AOS products are offered in packages with Pb-free plating and compliant to RoHS standards.
Please visit https://aosmd.com/sites/default/files/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration



DFN2x2-8L
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	FCCM	Continuous conduction mode of operation when FCCM = High.
2	PHASE	Discontinuous mode and diode emulation mode is active when FCCM = Low.
3	GH	High impedance on the input of FCCM will turn both High-Side and Low-Side driver to Low.
4	BOOT	Switching node connected to the Source of High-Side MOSFET and the Drain of Low-Side MOSFET.
5	PWM	High-Side gate driver output.
6	GND	High-Side MOSFET Gate Driver supply rail. Connect a 100 nF ceramic capacitor between BOOT and the PHASE (Pin 2).
7	GL	PWM input signal from the controller IC. This input is compatible with 5 V and Tri-State Logic.
8	VCC	Signal Ground.
16	EN	Low-Side gate driver output.
EXP	EXP	5 V Bias for Internal Logic Blocks. Ensure to position a 1 µF MLCC directly between VCC and GND (Pin 6).

Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
Low Voltage Supply (VCC)	-0.3 V to 7 V
Control Inputs (PWM, FCCM)	-0.3 V to (VCC + 0.3 V)
Bootstrap Voltage DC (BOOT-GND)	-0.3 V to 40 V
Bootstrap Voltage Transient (1) (BOOT-GND)	-8 V to 47 V
Bootstrap Voltage DC (BOOT-PHASE)	-0.3 V to 7 V
BOOT Voltage Transient(1) (BOOT-PHASE)	-0.3 V to 9 V
Switch Node Voltage DC (PHASE/ VSWH)	-0.3 V to 40 V
Switch Node Voltage Transient(1) (PHASE/VSWH)	-8 V to 45 V
Low-Side Gate Voltage DC (GL)	(GND - 0.3 V) to (PVCC + 0.3 V)
Low-Side Gate Voltage Transient (2) (GL)	(GND - 2.5 V) to (PVCC + 0.3 V)
High-Side Gate Voltage DC (GH)	(PHAS E- 0.3 V) to BOOT
High-Side Gate Voltage Transient (1) (GH)	(PHASE – 5 V) to BOOT
Storage Temperature (TS)	-65 °C to +150 °C
Max Junction Temperature (TJ)	150 °C
ESD Rating(3)	±2 kV

Notes:
1. Peak voltages can be applied for 10 ns per switching cycle.
2. Peak voltages can be applied for 20 ns per switching cycle.
3. Devices are inherently ESD sensitive, handling precaution are required. Human body model rating: 1.5Ω in series with 100 pF.

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
Low Voltage Supply VCC	4.5 V to 5.5 V
Control Inputs (PWM, FCCM)	0 V to VCC
Operating Frequency	200 kHz to 2 MHz

Electrical Characteristics[4]

T_J = 25 °C to 125 °C. Typical values reflect 25 °C ambient temperature; VCC = 5 V, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
General						
V_{CC}	Low Voltage Supply		4.5		5.5	V
$R_{\Theta JC}$ [4]	Thermal Resistance	PCB Temp = 100°C		20		°C/W
$R_{\Theta JA}$ [4]				85		°C/W
Input Supply and UVLO						
V_{CC_UVLO}	Under-Voltage Lockout	VCC Rising		3.5	3.9	V
V_{CC_HYST}		VCC Hysteresis		400		mV
I_{VCC}	Control Circuit Bias Current	FCCM = Floating PWM = Floating		3		µA
		FCCM = 5 V PWM = Floating		170		
		FCCM = 5 V PWM = Floating		180		
PWM Input						
V_{PWMH}	Logic High Input Voltage		4.2			V
V_{PWML}	Logic Low Input Voltage				0.72	V
I_{PWM_SRC}	PWM Pin Input Current	PWM = 0 V		-200		µA
I_{PWM_SNK}		PWM = 5 V		200		µA
V_{TRI}	PWM Tri-State Window		1.6		3.4	V
V_{PMW_FLOAT}	PWM Tri-State Voltage Clamp	PWM = Floating		2.5		V
FCCM Input						
V_{FCCM_H}	Logic High Input Voltage		3.9			V
V_{FCCM_L}	Logic Low Input Voltage				1.1	V
I_{FCCM_SRC}	FCCM Pin Input Current	FCCM = 0 V		-50		µA
I_{FCCM_SNK}		FCCM = 5 V		50		µA
V_{TRI}	FCCM Input Tri-State Threshold Window	FCCM = Floating	2.0		3.0	V
t_{PS4_EXIT}	Power Stage 4 Exit Latency			5	15	µs

Note:
4. All voltages are specified with respect to the corresponding AGND pin.

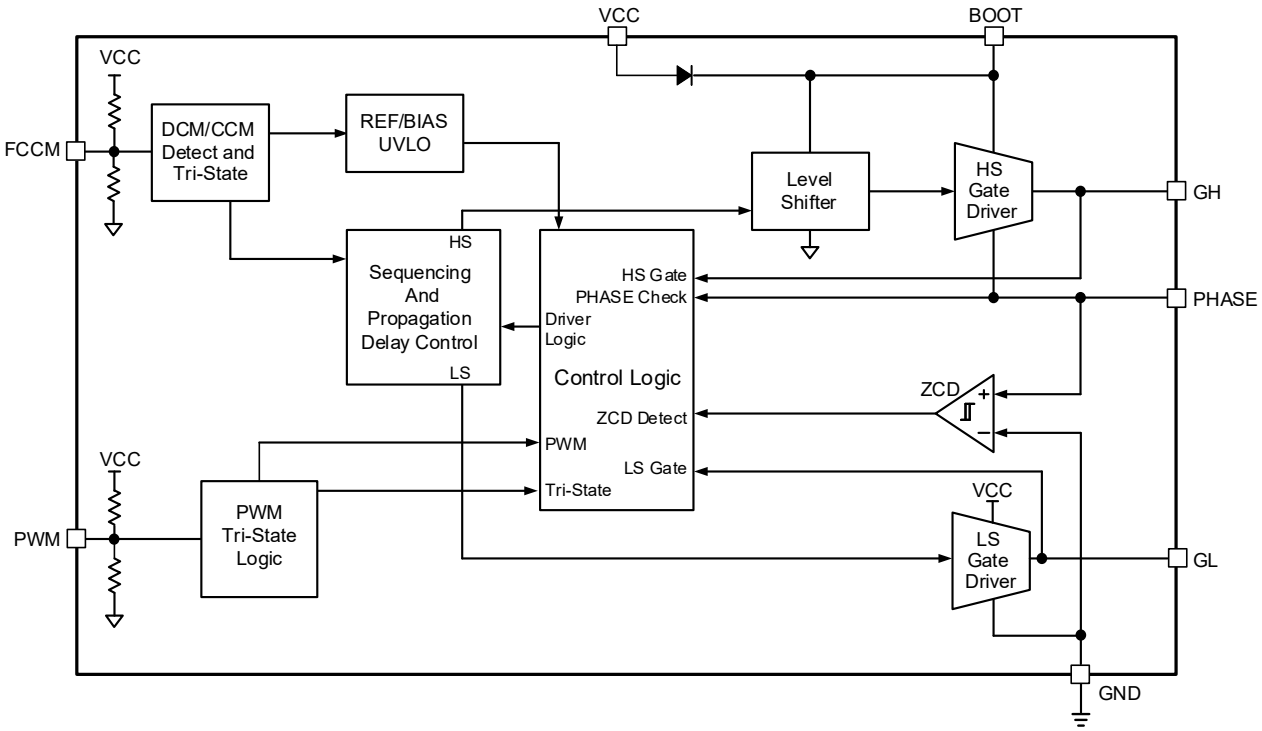
Electrical Characteristics[4]

T_J = 25 °C to 125 °C. Typical values reflect 25 °C ambient temperature; VCC = 5 V, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Gate Driver Timing						
t_{RISE_GH}	High-Side Driver Rise Time	3 nF Load		8		ns
t_{FALL_GH}	High-Side Driver Fall Time	3 nF Load		8		ns
t_{RISE_GL}	Low-Side Driver Rise Time	3 nF Load		8		ns
t_{FALL_GL}	Low-Side Driver Fall Time	3 nF Load		4		ns
t_{PDLU}	PWM to High-Side Gate	PWM: H → L, VSWH: H → L		30		ns
t_{PDLL}	PWM to Low-Side Gate	PWM: L → H, GL: H → L		25		ns
t_{PDHU}	Low-Side to High-Side Gate Deadtime	GL: H → L, GH: L → H		15		ns
t_{PDHL}	High-Side to Low-Side Gate Deadtime	VSWH: H → 1V, GL: L → H		13		ns
t_{TSSHD}	Tri-State Shutdown Delay	PWM: L → VTRI, GL: H → L and PWM: H → VTRI, VSWH: H → L		150		ns
t_{TSEXIT}	Tri-State Propagation Delay	PWM: VTRI → H, VSWH: L → H PWM: VTRI → L, GL: L → H		45		ns
t_{LGMIN}	LS Minimum On Time	FCCM = L		350		ns
Gate Driver Output						
R_{GH_SRC}	High-Side Source Resistance	Current = 500mA		1		Ω
I_{GH_SRC}	High-Side Source Current	GH-PHASE = 2.5V		2		A
R_{GH_SNK}	High-Side Sink Resistance	Current = 500mA		1		Ω
I_{GH_SNK}	High-Side Sink Current	GH-PHASE = 2.5V		2		A
R_{GL_SRC}	Low-Side Source Resistance	Current = 500mA		1		Ω
I_{GL_SRC}	High-Side Source Current	GL = 2.5V		2		A
R_{GL_SNK}	High-Side Sink Resistance	Current = 500mA		0.5		Ω
I_{GL_SNK}	High-Side Sink Current	GL = 2.5V		4		A

Note:
4. All voltages are specified with respect to the corresponding AGND pin.
5. Characterization value. Not tested in production.

Functional Block Diagram



Timing Diagrams

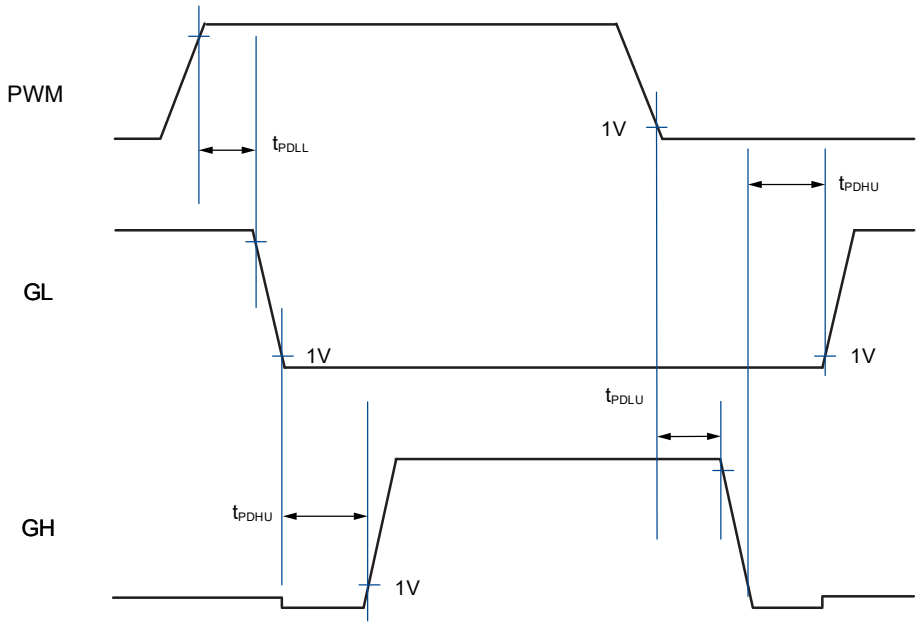


Figure 1. PWM Logic Input Timing Diagram

Timing Diagrams

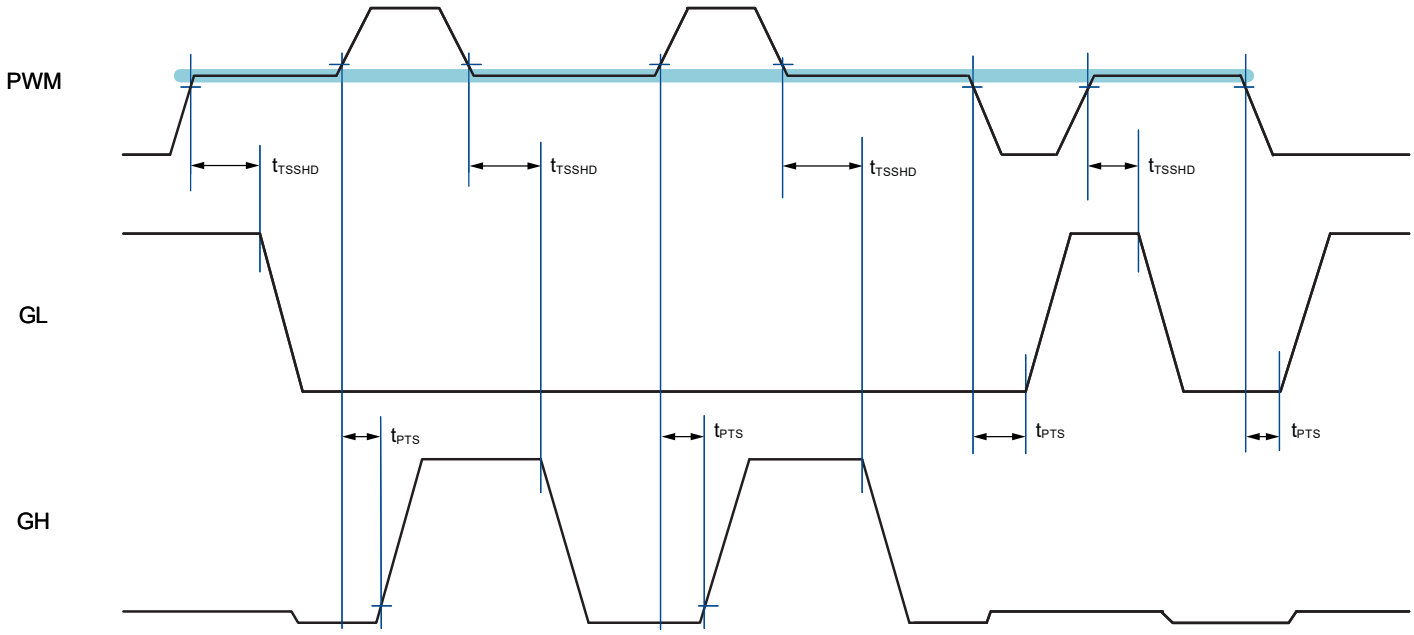


Figure 2. PWM Logic Input Timing Diagram

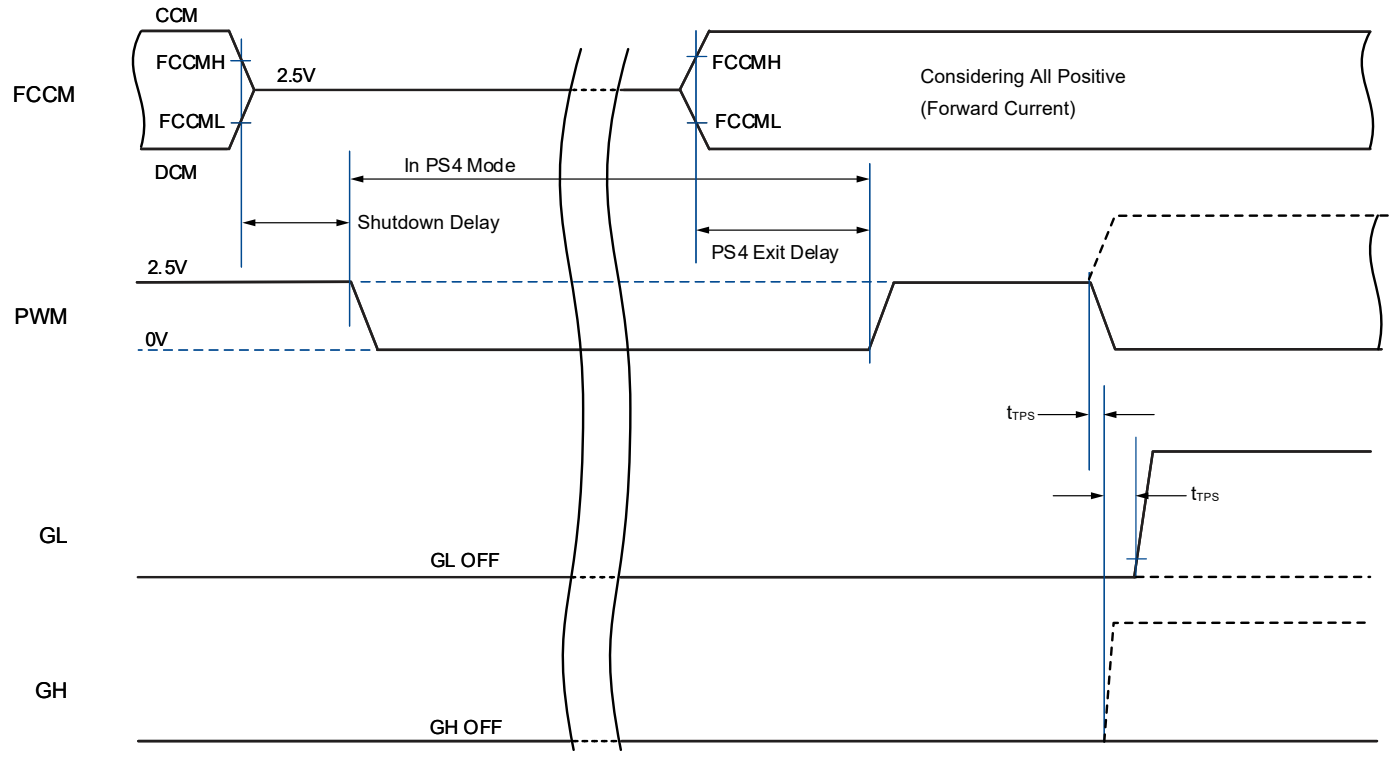


Figure 3. PWM Tri-State Hold Off and Exit Timing Diagram

Typical Characteristics

T_A = 25 °C, VCC = 5V, unless otherwise specified.

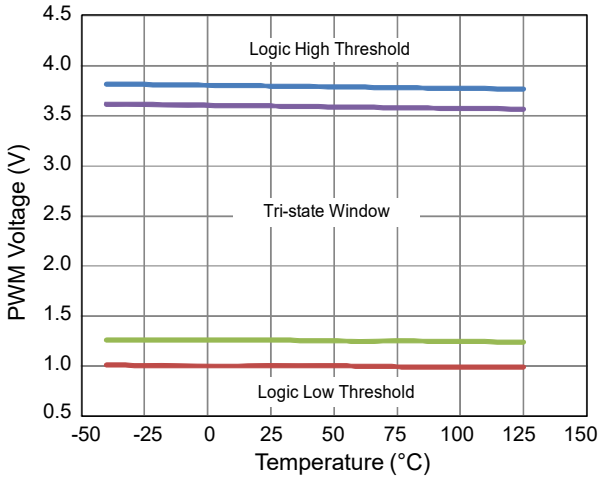


Figure 4. PWM Threshold vs. Temperature

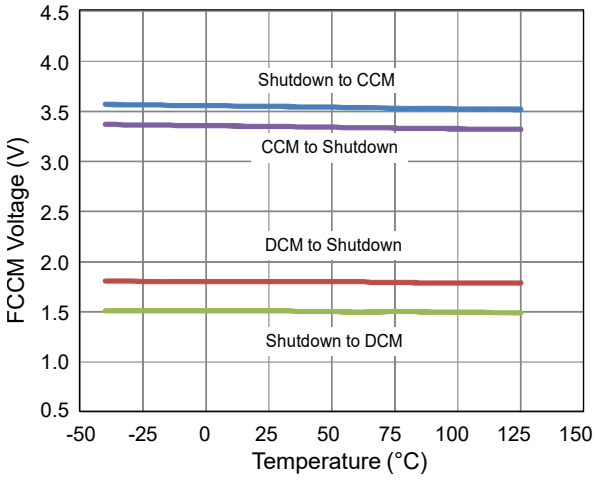


Figure 5. PWM Threshold vs. Temperature

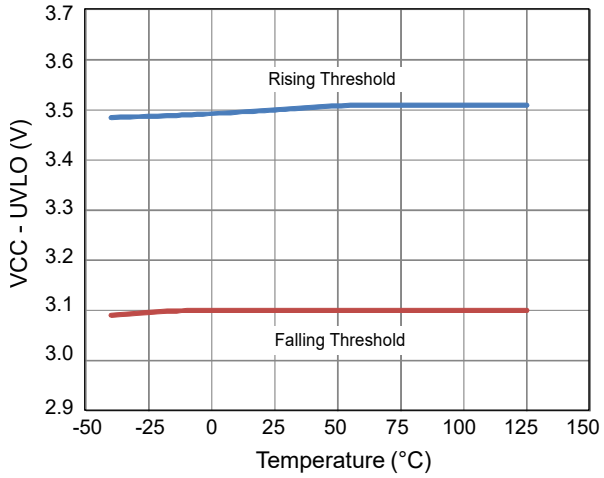


Figure 6. UVLO (VCC) Threshold vs. Temperature

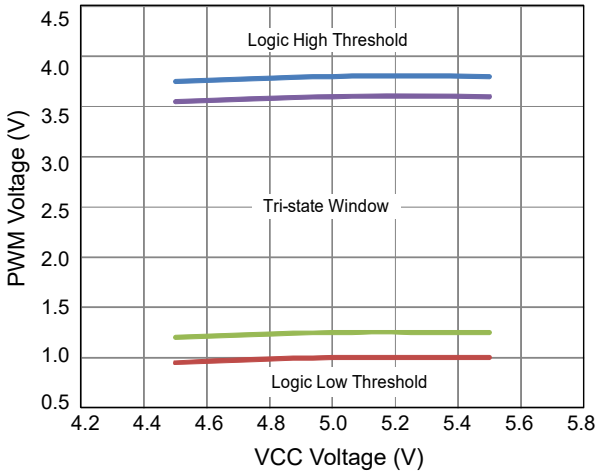


Figure 7. PWM Threshold vs. VCC Voltage

Application Information

AOZ59141DI is a dual channel synchronous driver IC designed to work over an input voltage range of 4.5V to 5.5V. High current MOSFET Gate Drivers are integrated in the package to minimize parasitic loop inductance for optimum switching efficiency.

Bootstrap Power Supply for High-Side Driver

The boost supply for driving the High-Side MOSFET is generated by connecting a small capacitor (100 nF) between the BOOT (Pin 4) and the switching node PHASE (Pin 2). It is recommended that this capacitor CBOOT should be connected to the device across Pin 2 and Pin 4 as close as possible. A bootstrap switch is integrated into the device to reduce external component count. An optional resistor RBOOT in series with CBOOT between 1Ω to 5Ω can be used to slow down the turn on speed of the High-Side driver output to achieve lower switching node spikes at the external power stage.

Input Voltage VCC and Under-Voltage Lockout

AOZ59141DI is rated to operate over a wide input range from 4.5V to 5.5V. The PHASE and BOOT is rated to operate up to 40V at the power stage.

AOZ59141DI starts up to normal operation when VCC rises above the Under-Voltage LockOut (UVLO) threshold voltage. The UVLO release is set at 3.5V typically.

PWM Input

AOZ59141DI is compatible with 5V (CMOS) PWM logic. Refer to Figure 1 for PWM logic timing and propagation delays diagram between PWM input and the gate driver outputs.

The PWM is also compatible with Tri-State input. When the PWM output from the external PWM controller is in high impedance or not connected both High-Side and Low-Side driver output are turned off. Table 1 shows the thresholds level for high-to-low and low-to-high transitions as well as Tri-State window.

There is a Holdoff Delay between the corresponding PWM Tri-State signal and the gate drivers to prevent spurious triggering of Tri-State mode which may be caused by noise or PWM signal glitches. The Holdoff Delay is typically 150 ns.

Table 1. PWM Input and Tri-State Threshold

Threshold	VPWMH	VPWML	VTRIH	VTRIL
AOZ59141DI	4.2V	0.72V	2.0V	3.0V

Note: See Figure 2 for propagation delays and Tri-State window

Diode Mode Emulation of Low-Side MOSFET (FCCM)

AOZ59141DI can operate in the diode emulation or pulse skipping mode using FCCM (Pin 1). This enables the High-Side and Low-Side driver to operate in asynchronous mode during start up, light load or under pre-bias conditions.

When FCCM is high, the module will operate in Continuous Conduction Mode (CCM). The Driver logic will use the PWM signal and generate both the High-Side and Low-Side complementary gate drive outputs with minimal anti-overlap delays to avoid cross conduction.

When FCCM is low, the module can operate in Discontinuous Conduction Mode (DCM). The High-Side MOSFET gate drive output is not affected but Low-Side MOSFET will enter diode emulation mode. See Table 2 for the truth table for PWM and FCCM inputs.

Table 2. PWM and FCCM Control Logic Truth Table

FCCM	PWM	GH	GL
L	L	L	H if IL > 0A L if IL < 0A
L	H	H	L
H	L	L	H
H	H	H	L
L	Tri-State	L	L
H	Tri-State	L	L
Tri-State	X	L	L

Gate Drives

AOZ59141DI is a high current high-speed driver that generates the floating gate driver for the external High-Side MOSFET and a complementary driver for the external Low-Side MOSFET. An internal shoot through protection scheme is implemented to ensure that both drivers cannot be turned on at the same time. The operation of PWM signal transition is illustrated as below.

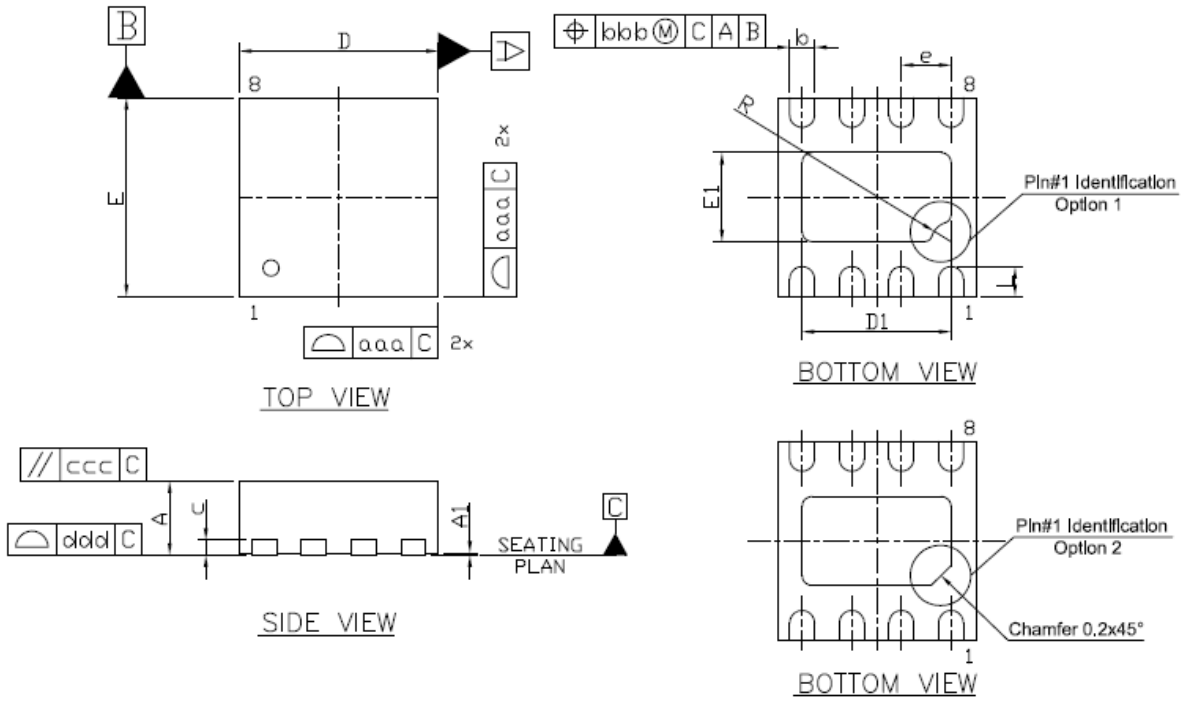
1. PWM from logic Low to logic High

When the falling edge of Low-Side Gate Driver output GL goes below 1V, the blanking period is activated. After a pre-determined value (t_{PDHU}), the complementary High-Side Gate Driver output GH is turned on.

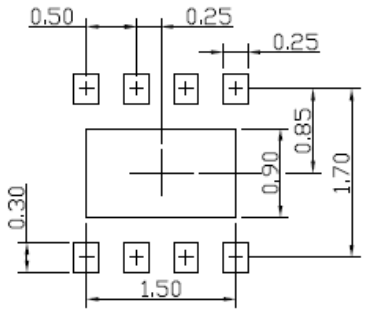
2. PWM from logic High to logic Low

When the falling edge of the switching node PHASE goes below 1V, the blanking period is activated. After a pre-determined value (t_{PDHL}), the complementary Low-Side Gate Driver output GL is turned on.

Package Dimensions, DFN2x2-8L



RECOMMENDED LAND PATTERN



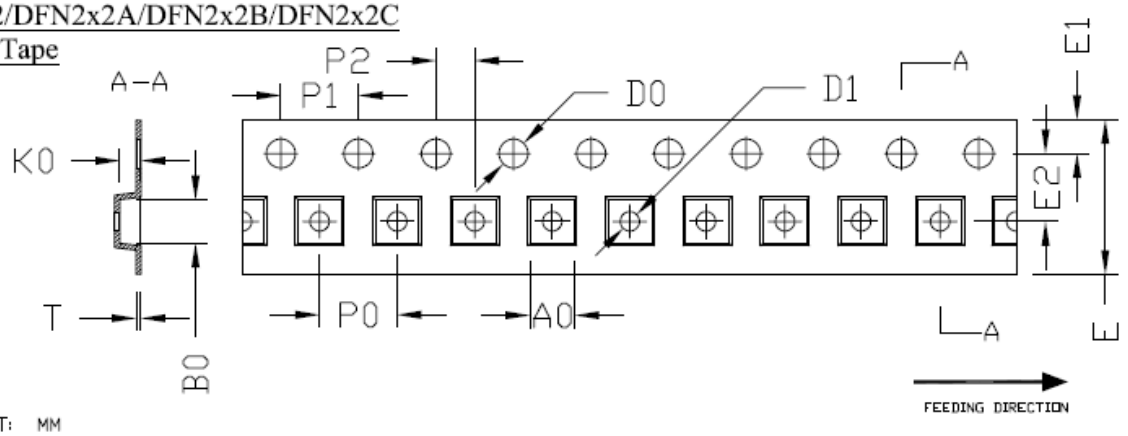
UNIT: mm

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.18	0.25	0.30	0.007	0.010	0.012
c	—	0.20 Ref	—	—	0.008 Ref	—
D	1.90	2.00	2.10	0.075	0.079	0.083
D1	1.35	1.50	1.60	0.053	0.059	0.063
E	1.90	2.00	2.10	0.075	0.079	0.083
E1	0.75	0.90	1.00	0.030	0.035	0.039
e	0.50 BSC			0.020 BSC		
L	0.20	0.30	0.40	0.008	0.012	0.016
R	0.20			0.008		
aaa	0.15			0.006		
bbb	0.10			0.004		
ccc	0.10			0.004		
ddd	0.08			0.003		

NOTE
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. CONTROLLING DIMENSION IS MILLIMETER.
   CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
3. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.10mm. AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
4. COPLANARITY ddd APPLIERS TO THE TERMINALS AND ALL OTHER BOTTOM SURFACE METALLIZATION.

Tape and Reel Dimensions, DFN2x2-8L

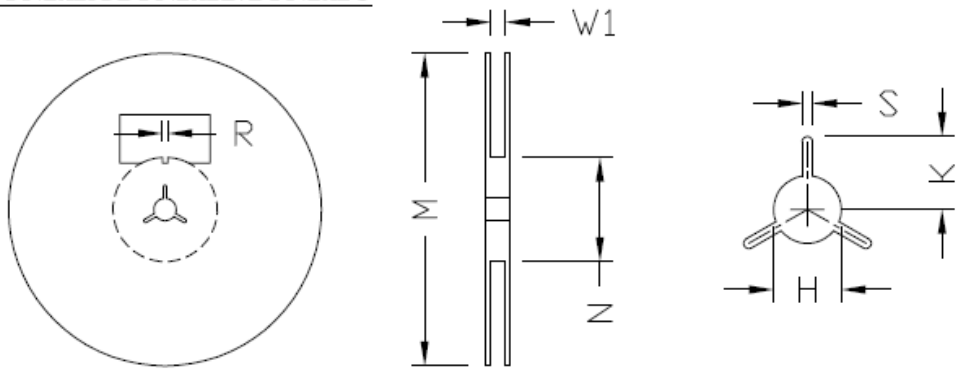
DFN2x2/DFN2x2A/DFN2x2B/DFN2x2C
Carrier Tape



UNIT: MM

OPTION	PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
1	DFN 2x2 DFN 2x2A DFN 2x2B DFN 2x2C	2.25 ±0.05	2.25 ±0.05	1.00 ±0.05	1.50 +0.10 −0	1.00 +0.25 −0	8.00 +0.30 −0.10	1.75 ±0.10	3.50 ±0.05	4.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.254 ±0.02
2		2.30 ±0.20	2.30 ±0.20	1.00 ±0.20	1.50 +0.10 −0	1.00 MIN.	8.00 +0.30 −0.10	1.75 ±0.10	3.50 ±0.05	4.00 ±0.20	4.00 ±0.20	2.00 ±0.05	0.30 ±0.05

DFN2x2/DFN2x2A/DFN2x2B/DFN2x2C
REEL



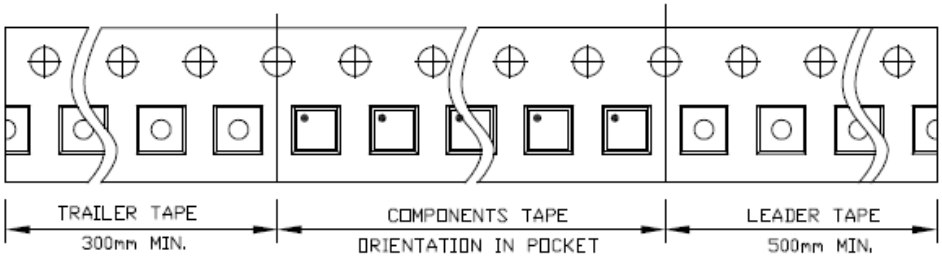
UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W1	H	S	K	R
8	ø180	ø180.0 ±0.50	60.0 ±0.50	8.4 +1.5 −0.0	13.0 ±0.20	1.5 MIN.	13.5 MIN.	3.0 ±0.50

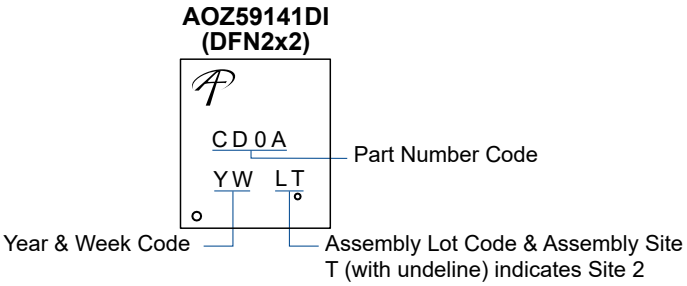
DFN2x2/DFN2x2A/DFN2x2B/DFN2x2C TAPE

Leader / Trailer
& Orientation
Unit Per Reel:
3000pcs

Normal Orientation



Part Marking



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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.