AOZ17517QI

ECPower™ 20V 0.65mΩ 60A Smart eFuse

General Description

AOZ17517QI is a current-limiting protection eFuse targeting applications that require front end protection at the input line. Both VIN and VOUT terminals are rated at 27V absolute maximum. There is a programmable soft-start feature that controls the inrush current for highly capacitive loads. It also has Input Under-Voltage Lock Out (UVLO), and Thermal Shut Down Protection (TSD). The device can be configured for latch off or auto retry after a fault shutdown.

AOZ17517QI features an internal over current protection circuit that protects the supply from large load current. The over current threshold can be set externally with a resistor. AOZ17517QI also integrates accurate analog current and voltage monitoring signals. It can also be paralleled for higher current applications.

Multiple devices can operate concurrently and seamlessly distribute the current during the startup phase.

AOZ17517QI is available in 5mm x 5mm 32-pin QFN package.

Features

- 4.5V to 20V input voltage operating range
- 60A maximum output current
- 27V abs max voltage rating on VIN and VOUT pin
- Typical RON: 0.65 mΩ
- Programmable Output Soft Start
- Programmable Current Limit
- Short-Circuit Protection
- Input Under-Voltage Lock Out (UVLO)
- Thermal Shut Down Protection (TSD)
- Accurate Current Monitor
- Analog Temperature Output
- Current Sharing for Higher Current Applications
- ±2kV HBM ESD rating
- ±1kV CDM ESD rating

Applications

- Server
- PC Card
- Networking
- High power industrial 12V rail protection

GREEN Product

Typical Application

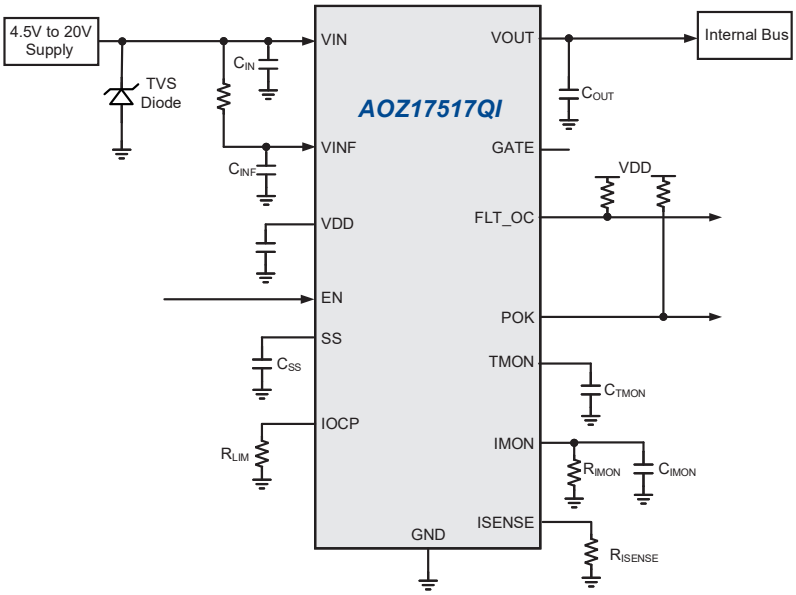


Figure 1. Stand-alone Application

Typical Application

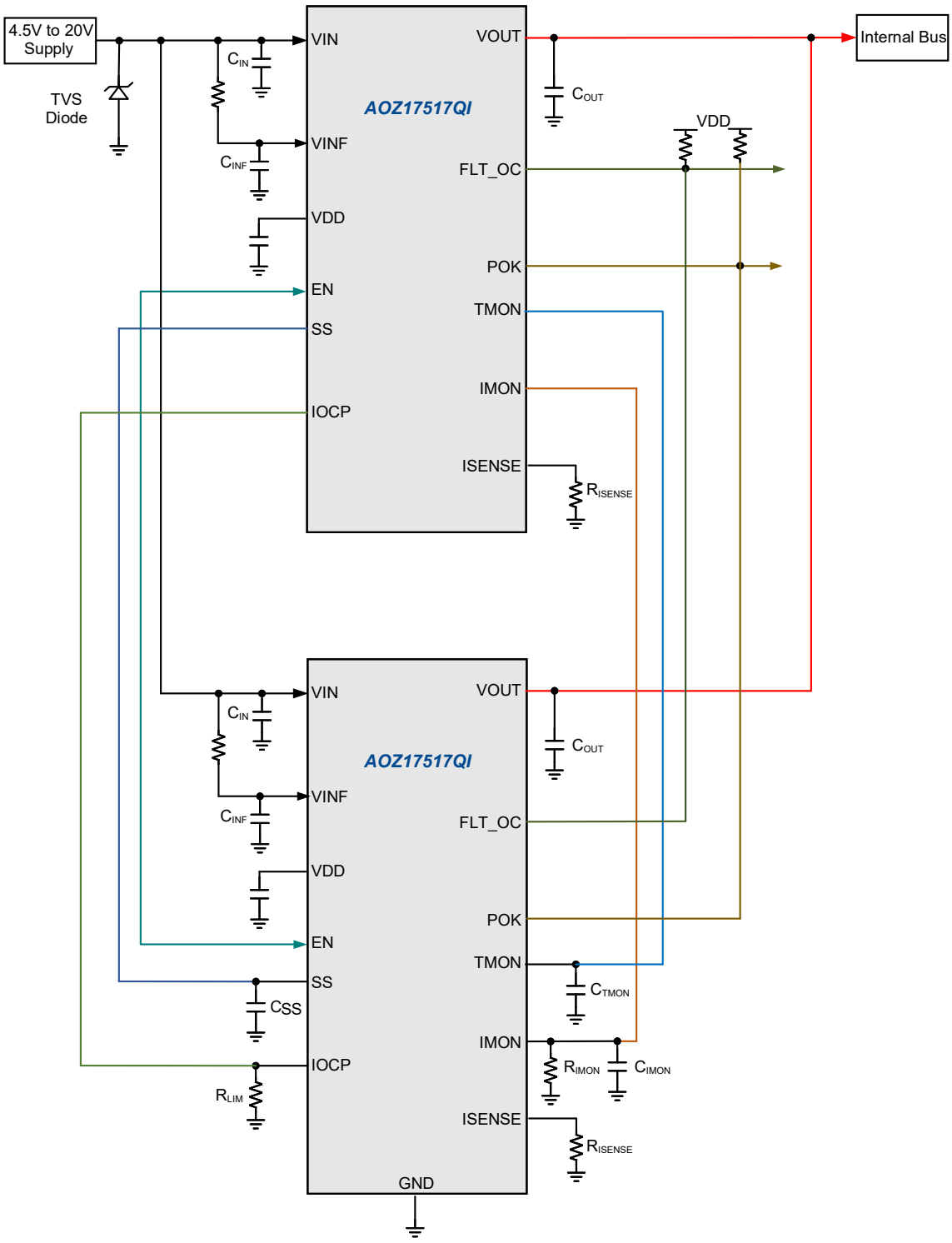


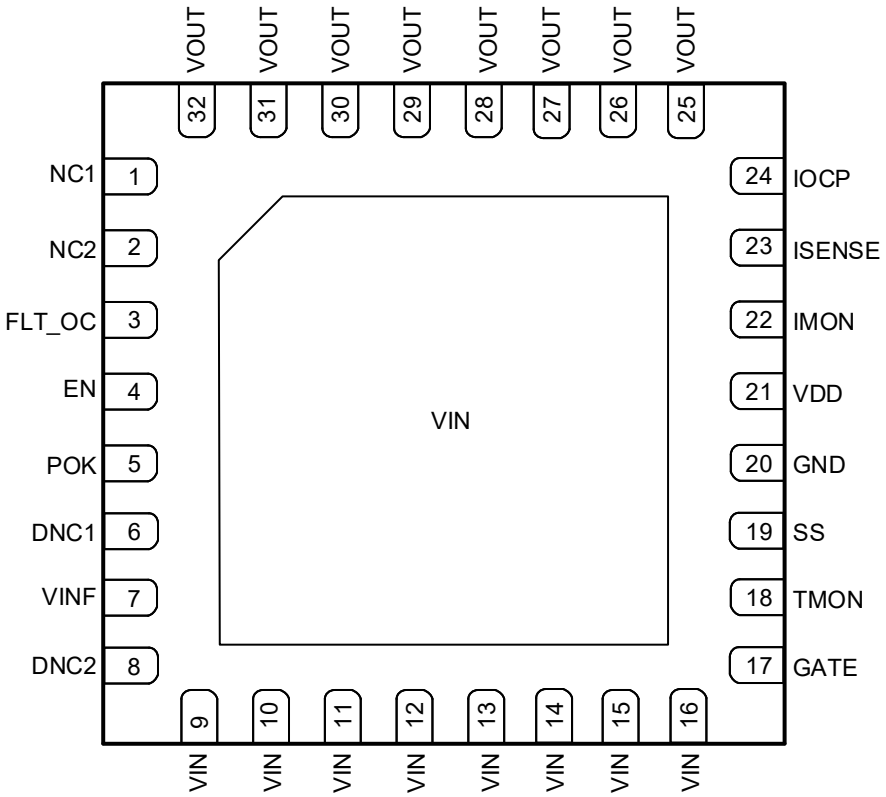
Figure 2. Parallel Application

Ordering Information

Part Number	Fault Recovery	Operating Voltage Range	Package	Environmental
AOZ17517QI-01	Auto-restart	4.5V — 20V	QFN5x5-32L	RoHS
AOZ17517QI-02	Latch-off	4.5V — 20V	QFN5x5-32L	RoHS

AOS products are offered in packages with Pb-free plating and compliant to RoHS standards.
Please visit https://aosmd.com/sites/default/files/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration



QFN5x5-32L
(Top Transparent View)

Pin Description

Pin Number	Pin Name	Pin Function
1	NC1	No Connection1.
2	NC2	No Connection2.
3	FLT_OC	Open-drain output to indicate overcurrent condition. Low indicates the device is in over current condition. The FLT_OC output does not report over current during soft−start.
4	EN	Enable input. Active high.
5	POK	OK status indicator output (Open Drain). Low indicates that the switch was turned off by a fault.
6	DNC1	Do Not Connect1. Reserved for test.
7	VINF	Control circuit power supply input. Connect to VIN pins through an RC filter.
8	DNC2	Do Not Connect2. Reserved (Source sense connection).
9,10,11,12, 13,14,15,16, EPAD	VIN	Supply input. Connected to main power supply.
17	GATE	Gate pin of the internal MOSFET
18	TMON	Analog temperature monitor output.
19	SS	Soft Start control. Connect a capacitor CSS from SS to GND to set the soft start time.
20	GND	Ground
21	VDD	Linear regulator output for biasing internal circuities. Connect 2.2 uF-10 uF capacitor from this pin to ground.
22	IMON	Analog current monitor output.
23	ISENSE	Current sense feedback output (current). Scaling the voltage developed at this pin with a resistor to ground makes this also an input for several current limiting functions and overcurrent indicator OC.
24	IOCP	Over current threshold setpoint input for normal operation (after soft−start). Connect a 1% resistor RIOCP from IOCP to GND to set the current limit threshold.
25,26,27,28, 29,30,31,32	VOUT	Source of the internal N-Channel MOSFET. Connect to load. They are internally connected together.

Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
VIN, VINF, VOUT to GND	-0.3V to +27V
VDD to GND	-0.3V to +6V
Signal pins (EN, SS)	-0.3V to +VDD
Junction Temperature (T_J)	+150°C
Storage Temperature (T_S)	-65°C to +150°C
ESD Rating HBM All Pins	±2kV

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
VIN,VINF to GND	4.5V to 20V
EN, Isense, SS, FLT_OC, I_{OCP}, I_{MON}, T_{MON} ,POK to GND	0V to 5V
Switch DC Current (I_{SW})	0A to 60A
Junction Temperature (T_J)	-40°C to +125°C

Electrical Characteristics

$V_{VIN} = V_{VINF} = 12.0V$, $V_{EN} = 3.3V$, $C_{VINF} = 0.1\mu F$, $C_{VDD} = 4.7\mu F$, $C_{TIMON} = 0.1\mu F$, $R_{TMON} = 1k\Omega$, C_{SS} = 100nF (unless specified otherwise)
Min/Max values are valid for the temperature range -40°C ≤ $T_A = T_J$ ≤ 125°C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
General						
V_{IN}	Input Supply Voltage	R_{IOCP} = 121kΩ	4.5		20	V
V_{DD}	VDD Output Voltage	I_{VDD} = 0mA, VINF = 6V	4.65	5	5.35	V
$I_{VDD\_Capability}$	VDD Current Capability	VINF = 5.5V		40		mA
I_{VDD_Limit}	VDD Current Limit	VINF = 12V	50	90		mA
$V_{DD\_Dropout}$	VDD Dropout Voltage	VINF = 4.5V, I_{VDD} = 25mA		200	350	mV
$V_{DD\_UVLO\_R}$	Under-Voltage Lockout Threshold	VDD rising	3.6	4	4.4	V
$V_{DD\_UVLO\_F}$	Under-Voltage Lockout Threshold	VDD falling	3.2	3.6	4	V
$V_{DD\_UVLO\_HYS}$	Under-Voltage Lockout Hysteresis			400		mV
I_{IN_ON}	VIN Input Quiescent Current	EN = 3.3V, I_{OUT} = 0A		3.5	5	mA
I_{IN_OFF}	VIN Input Shutdown Current	EN = 0V		3.5	5	mA
R_{ON}	Switch On Resistance	I_{OUT} = 1A, T_J=25°C		0.65	1.0	mΩ
Enable						
I_{EN}	EN Bias current			5		µA
V_{EN_H}	Enable Input Logic High Threshold	EN rising, FET ON	1.2	1.4	1.6	V
V_{EN_L}	Enable Input Logic Low Threshold	EN falling	1.1	1.3	1.5	V
V_{EN_DIS}	Enable Input Logic Threshold to enable VOUT discharge circuit	EN falling, FET OFF & Vout Discharge Circuit(500Ω) ON		1.0		V
Output Ramp Control (SS)						
I_{SS}	SS charging current	VSS = 0V		6		µA
A_{VSS}	Gain to VOUT			8		V/V
IMON/ISENSE						
IMON/IOUT ISENSE/IOUT	IMON/IOUT gain or ISENSE/IOUT gain			10		µA/A
Accuracy (single eFuse)	IMON or ISENSE Accuracy	IOUT = 10A T_A=25°C	-3.0		+3.0	%
		IOUT > 10A T_A=25°C (Note 1)	-3.0		+3.0	%
		IOUT > 10A T_A=0 to 85°C (Note 1)	-4.5		+4.5	%

Electrical Characteristics

V_{VIN} = V_{VINF} = 12.0V, V_{EN} = 3.3V, C_{VINF} = 0.1µF, C_{VDD} = 4.7µF, C_{TIMON} = 0.1µF, R_{TMON} = 1kΩ, C_{SS} = 100nF (unless specified otherwise)
Min/Max values are valid for the temperature range -40°C ≤ T_A = T_J ≤ 125°C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Over Current Protection (OCP)						
V_{CL}	Current Limit Voltage	R_{IOCP} = 121kΩ	98	100	102	%VIOCP
t_{HOLD}	Max Current Limit hold off time	During soft start		250		µs
		After soft start, Vout reach 90% of Vin		1000		
I_{IOCP}	IOCP Bias Current		9.6	10	10.4	µA
V_{Isense_Clamp}	Isense Current Source Clamp Voltage			3		V
I_{SC_TH}	Short Circuit Threshold			100		A
$t_{SC\_Resopnse}$	Short Circuit Response Time (Note 1)	From IOUT >I_{SC_TH} until gate pull down		500		ns
FLT_OC OUTPUT						
$V_{FLT\_OC\_TH\_R}$	Over Current Rising Threshold		80	85	90	% VIOCP
$V_{FLT\_OC\_TH\_F}$	Over Current Falling Threshold		75	80	85	% VIOCP
$V_{FLT\_OC\_LOW}$	FLT_OC Output Low Voltage	Isink = 100µA			0.1	V
$I_{FLT\_OC\_leak}$	FLT_OC Out Leakage Current	VOC = 5V		3.5	100	nA
$T_{FLT\_OC\ Delay\_R}$	Delay Rising			1		µs
$T_{FLT\_OC\ Delay\_F}$	Delay Falling			1		µs
TMON OUTPUT						
T_{mon_bias}	Bias Voltage	T_J = 25°C		450		mV
T_{mon_gain}	Gain			10		mV/°C
R_{Tmon}	Load Capability			1		kΩ
$I_{Tmon\_pull\ down}$	Pull Down Current			50		µA
POK OUTPUT						
V_{POK_Low}	Output Low Voltage	Isink = 100µA			0.1	V
$I_{POK\_Leakage}$	Out Leakage Current	5V		3.5	100	nA
$T_{POK\ Delay\_R}$	Delay Rising			1		µs
$T_{POK\ Delay\_F}$	Delay Falling			1		µs
FET Health Check						
V_{DS_TH}	VDS Short Threshold	Startup delay if Vout > V_{DS_TH} when EN goes Hi		90%		VIN
V_{DS_OK}	VDS Short OK Threshold	Startup resume if Vout falls below V_{DS_OK}		80%		VIN
Thermal Shutdown (TSD)						
T_{SD}	Thermal Shutdown Threshold	Temperature rising		150		°C
T_{SD_HYS}	Thermal Shutdown Hysteresis	Temperature falling (AOZ17517QI-01 only)		25		°C
Dynamic Characteristics						
t_{D_ON}	Turn-On Delay Time			1		ms
t_{D_OFF}	Turn-Off Delay Time			1.5		µs
t_{Retry}	Retry Time after fault occurs	AOZ17517QI-01 only		1		s

Thermal Characteristics

Symbol	Parameter	Typ	Units
$R_{th(J-C)}$	Thermal Resistance from junction to case (Note 2)	2	°C/W
$R_{th(J-A)}$	Thermal Resistance from junction to ambient (Note 2)	25	°C/W

Notes:
1. Guarantee by characterization and design.
2. The thermal resistances are measured on AOZ17517QI evaluation board, which is 2OZ copper 8-layer FR4 board.

Functional Block Diagram

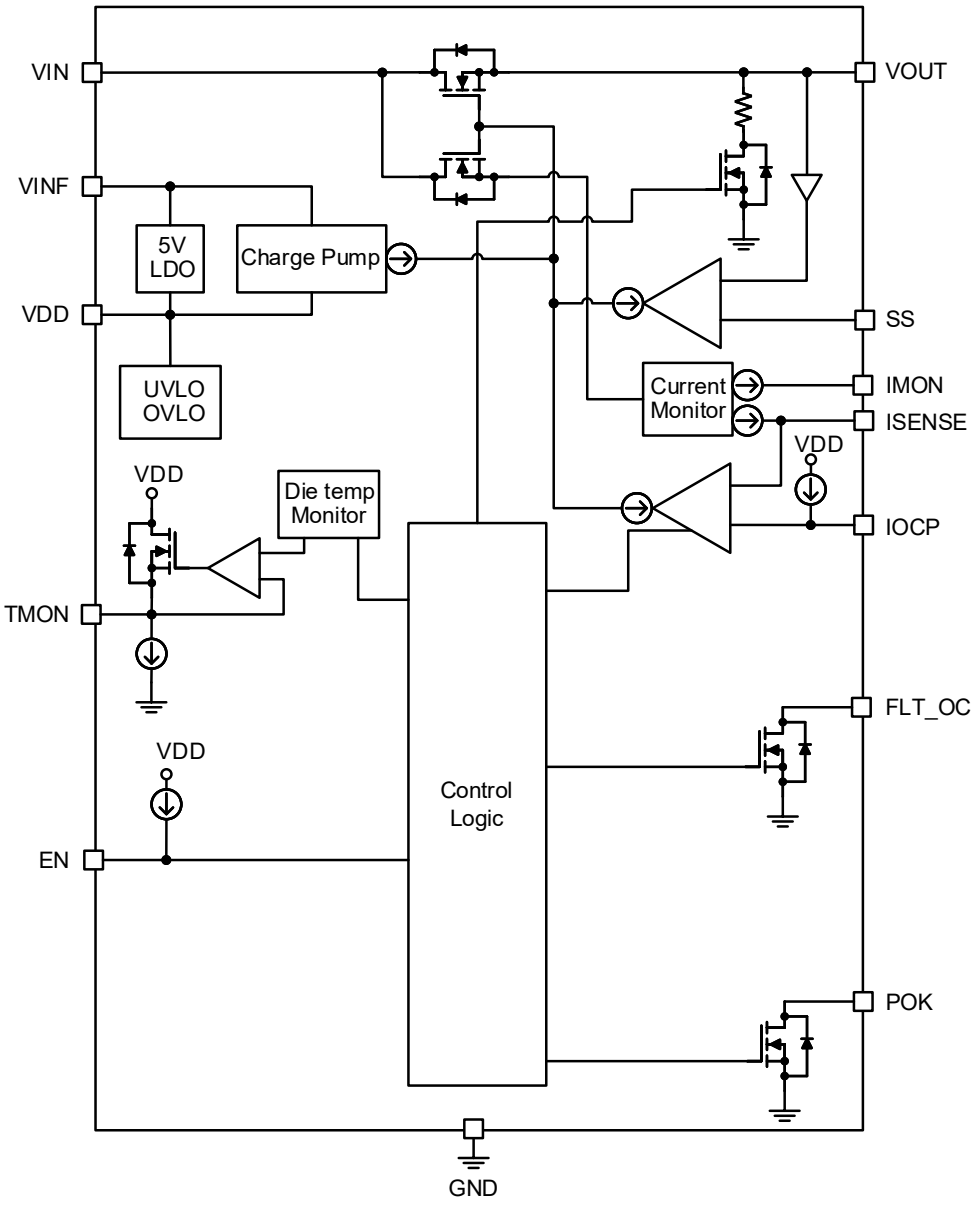


Figure 3. Functional Block Diagram

Timing Diagrams

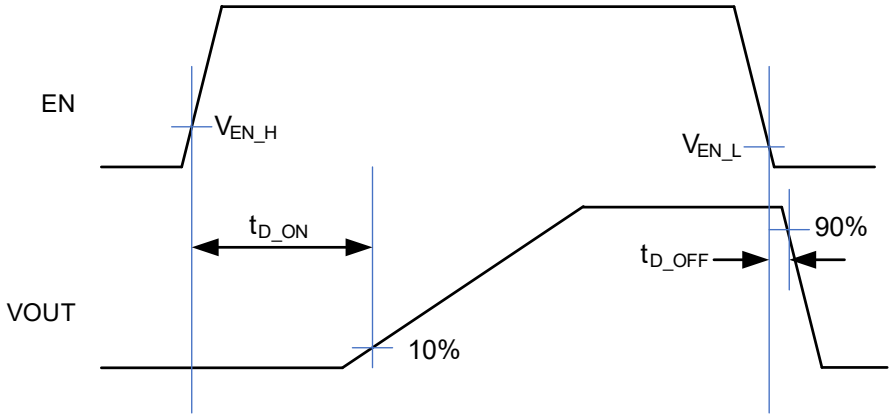
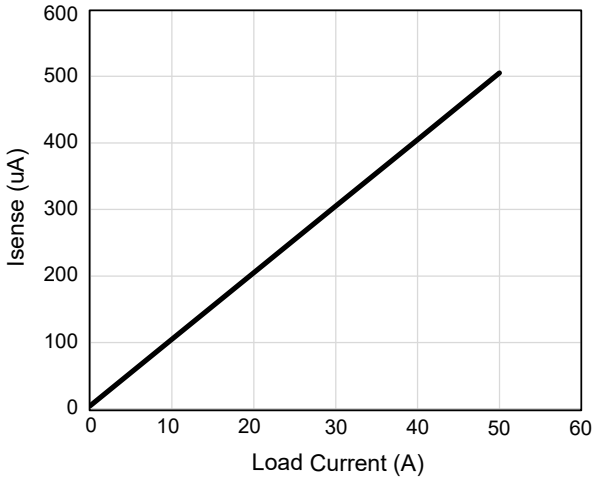


Figure 4. Turn-on and Turn-off Delay Time

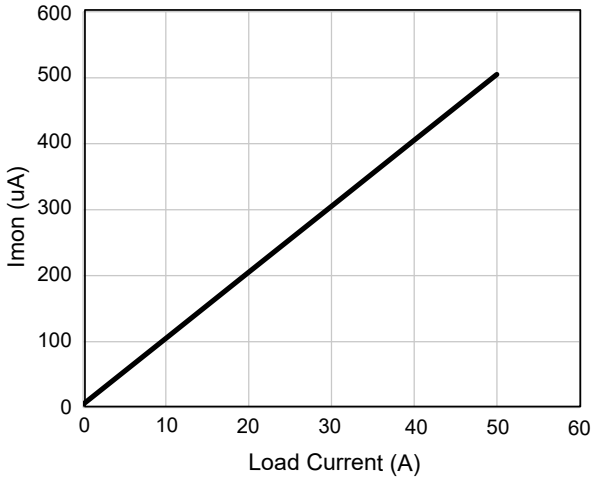
Typical Characteristics

Test Conditions: VIN = 12V, R_{ISENSE} = 2kΩ, C_{SS} = 200nF, R_{IOCP} = 121kΩ, T_A = 25°C, unless otherwise specified.

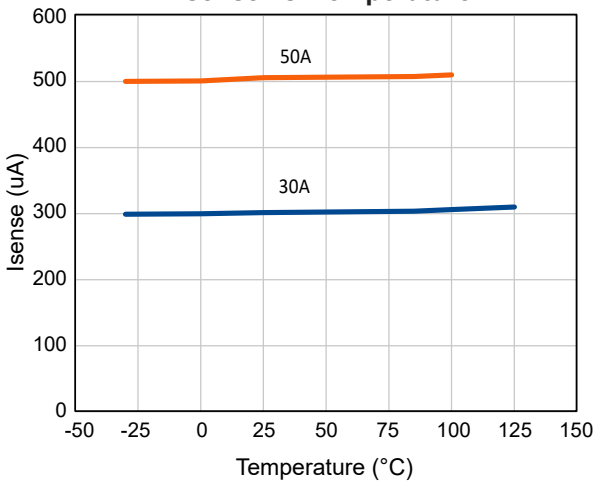
Isense vs. Load Current



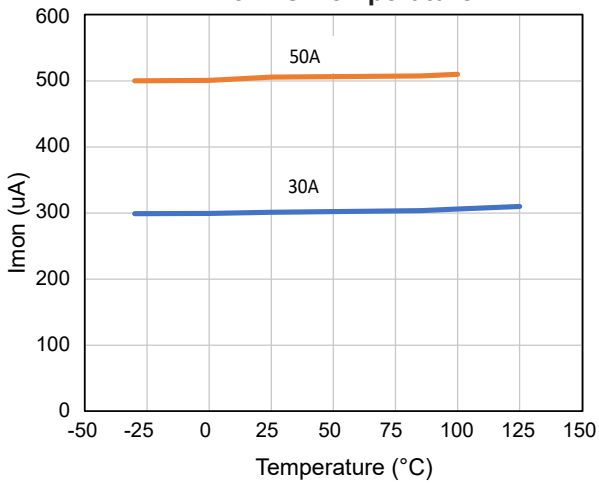
Imon vs. Load Current



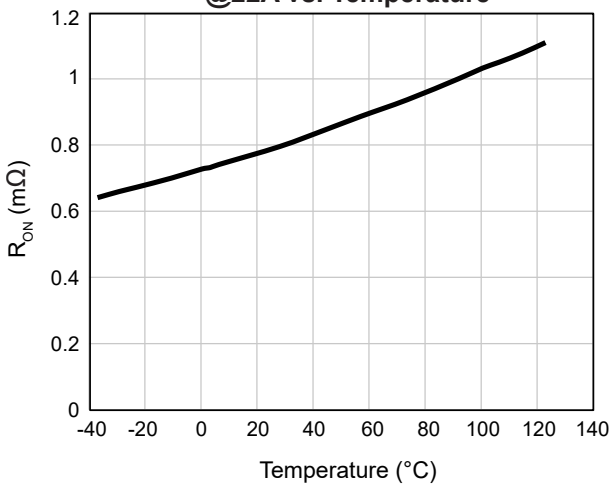
Isense vs. Temperature



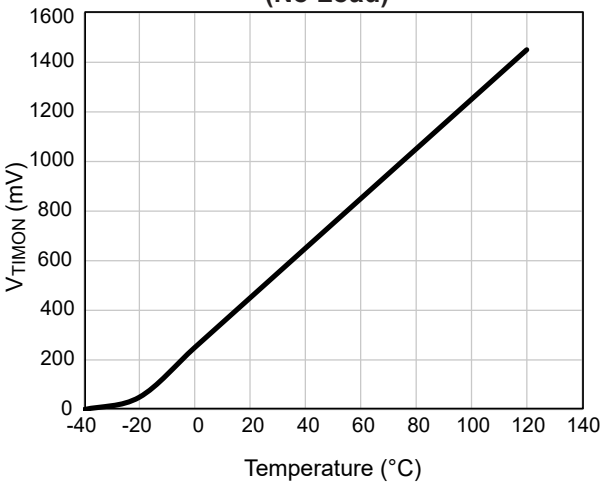
Imon vs. Temperature



Output Switch R_{ON} @22A vs. Temperature



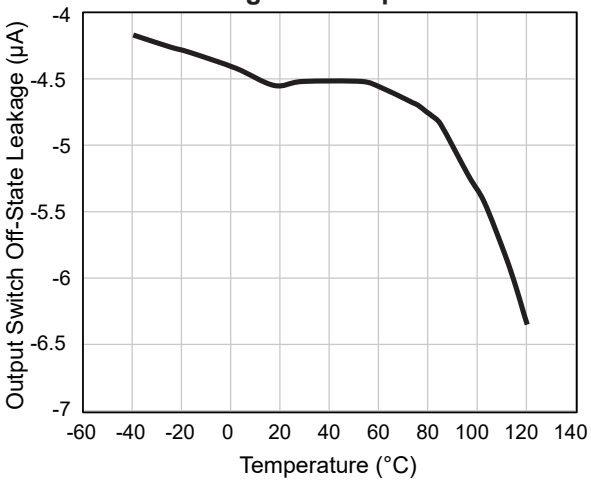
V_{Tmon} vs. Temperature (No Load)



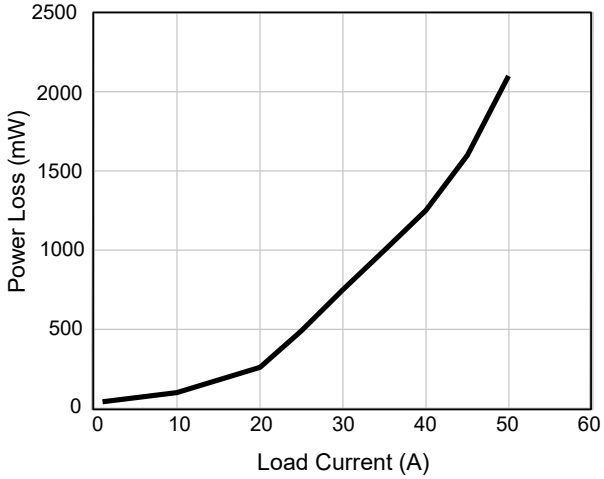
Typical Characteristics

Test Conditions: VIN = 12V, R_{ISENSE} = 2kΩ, C_{SS} = 200nF, R_{IOCP} = 121kΩ, T_A = 25°C, unless otherwise specified.

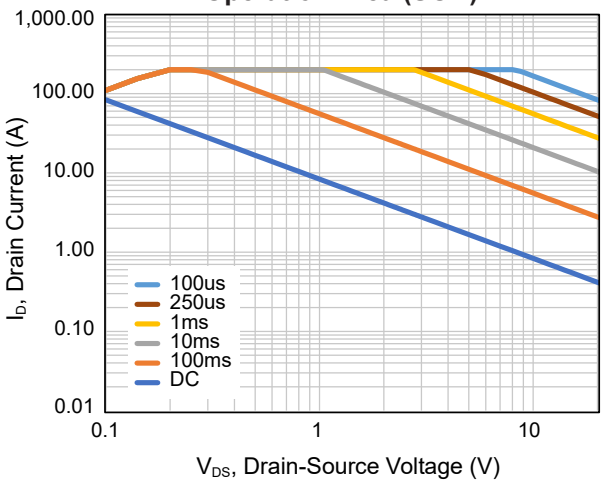
Output Switch Off-state Leakage vs. Temperature



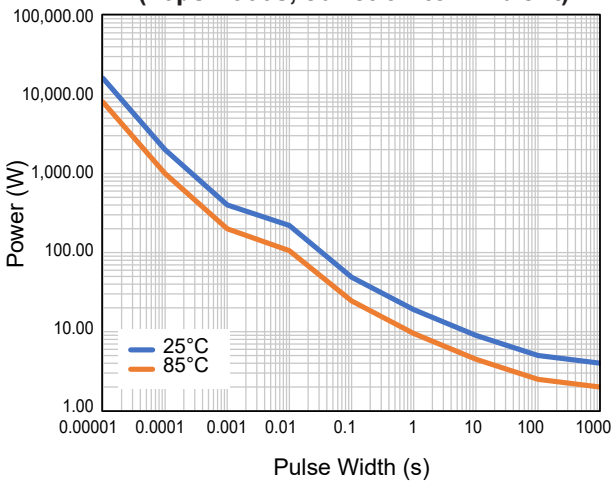
Power Loss vs. Load Current



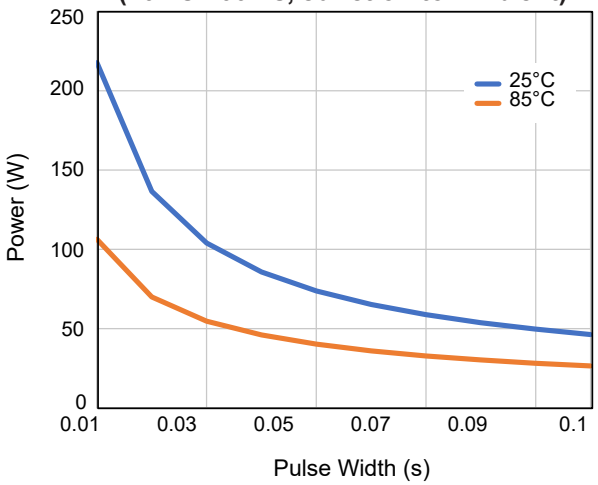
Internal MOSFET Safe Operation Area (SOA)



Single Pulse Power Rating (10µs-1000s, Junction to Ambient)



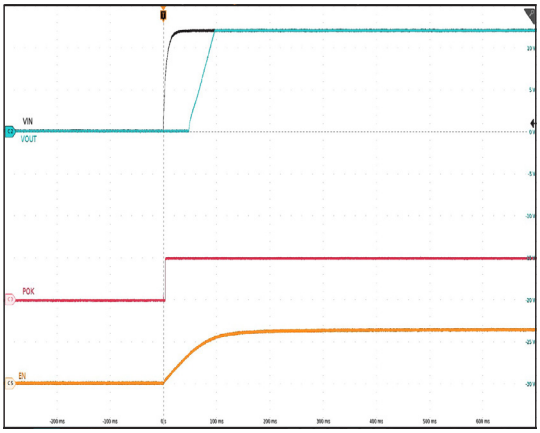
Single Pulse Power Rating (10ms-100ms, Junction to Ambient)



Typical Characteristics

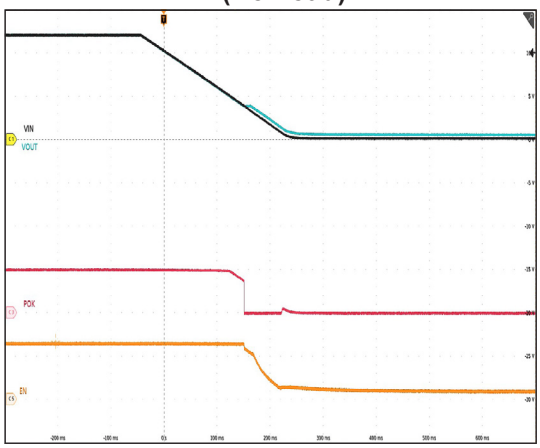
Test Conditions: VIN = 12V, R_{ISENSE} = 2kΩ, C_{SS} = 200nF, R_{IOCP} = 121kΩ, T_A = 25°C, unless otherwise specified.

Startup by Vin (No Load)



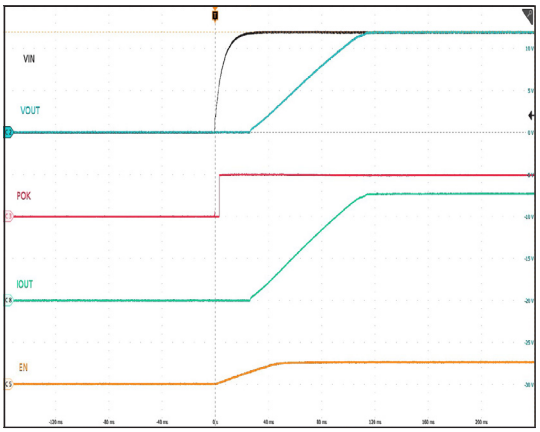
VIN (5V/div)
VOUT (5V/div)
POK (5V/div)
EN (2V/div)
100ms/div

Shutdown by Vin (No Load)



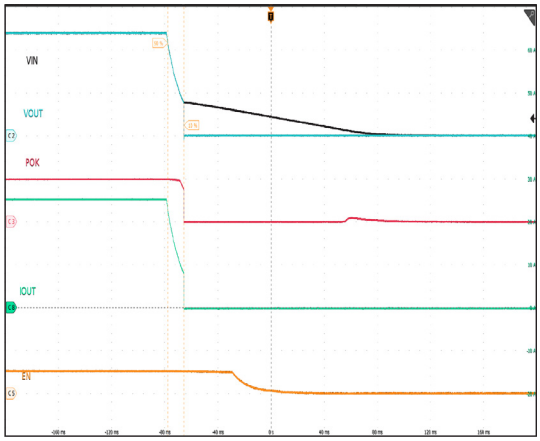
VIN (5V/div)
VOUT (5V/div)
POK (5V/div)
EN (2V/div)
100ms/div

Startup by Vin (I_{OUT}=25A)



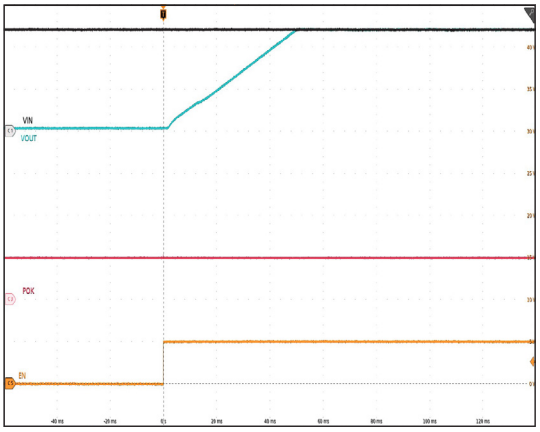
VIN (5V/div)
VOUT (5V/div)
POK (5V/div)
IOUT (10A/div)
EN (5V/div)
40ms/div

Shutdown by Vin (I_{OUT}=25A)



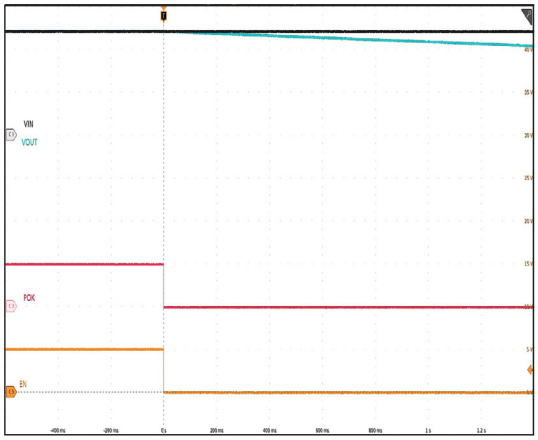
VIN (5V/div)
VOUT (5V/div)
POK (5V/div)
IOUT (10A/div)
EN (5V/div)
40ms/div

Startup by EN (No Load)



VIN (5V/div)
VOUT (5V/div)
POK (5V/div)
EN (5V/div)
20ms/div

Shut Down by EN (No Load)

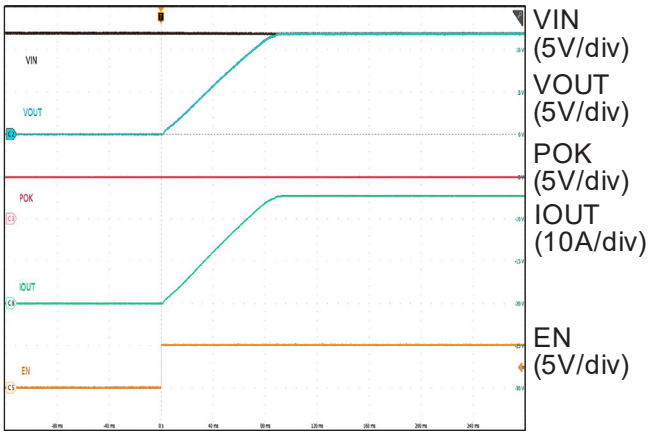


VIN (5V/div)
VOUT (5V/div)
POK (5V/div)
EN (5V/div)
200ms/div

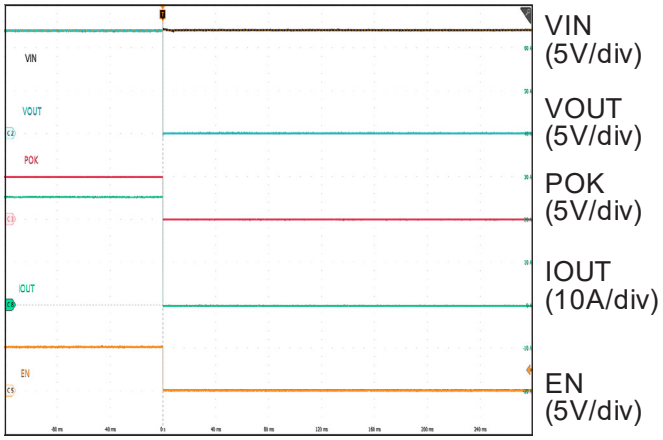
Typical Characteristics

Test Conditions: VIN = 12V, R_{ISENSE} = 2kΩ, C_{SS} = 200nF, R_{IOCP} = 121kΩ, T_A = 25°C, unless otherwise specified.

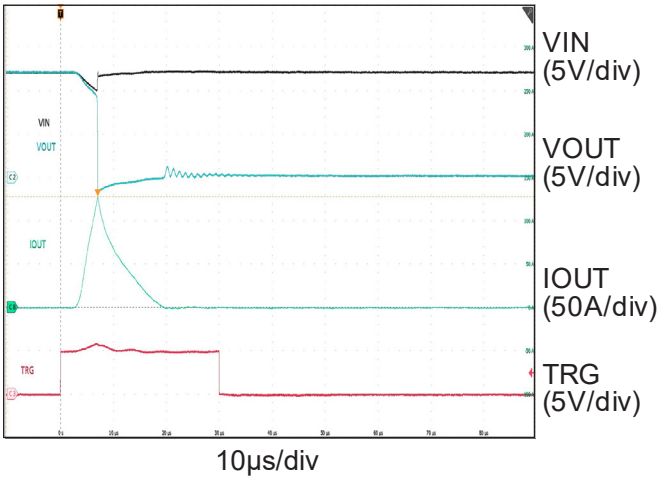
Startup by EN (I_{OUT}=25A)



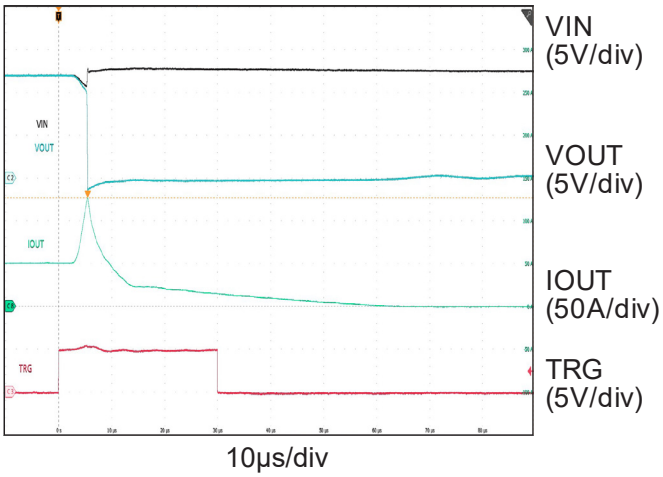
Shutdown by EN (I_{OUT}=25A)



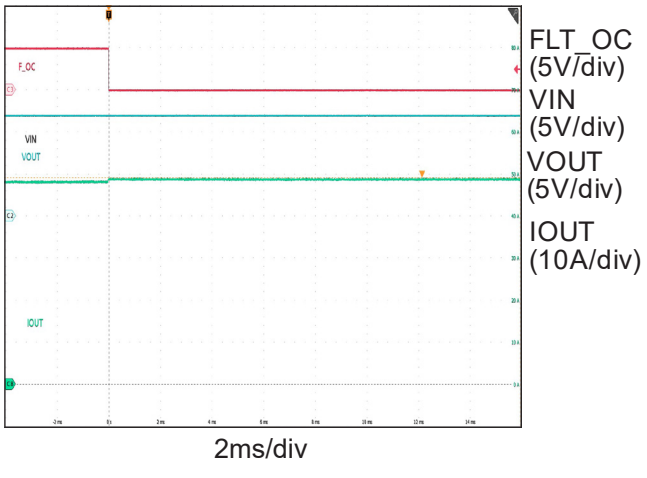
Short Circuit during Normal Operation (I_{OUT}=0A)



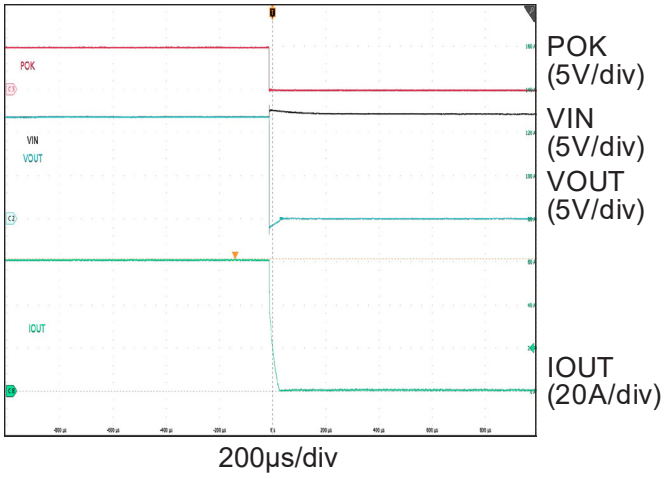
Short Circuit during Normal Operation (I_{OUT}=50A)



FLT_OC indication for Current Limit during Normal Operation



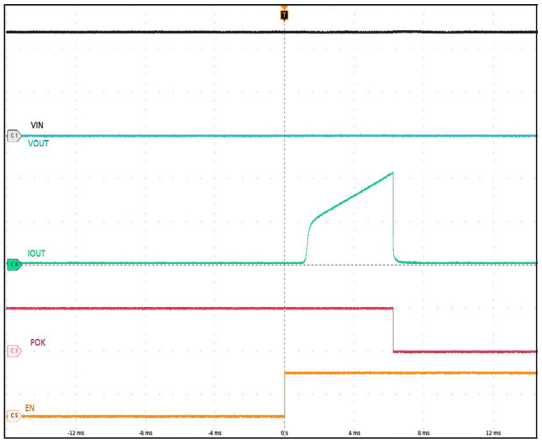
OCP during Normal Operation (I_{OUT}=60A)



Typical Characteristics

Test Conditions: VIN = 12V, R_{ISENSE} = 2kΩ, C_{SS} = 200nF, R_{IOCP} = 121kΩ, T_A = 25°C, unless otherwise specified.

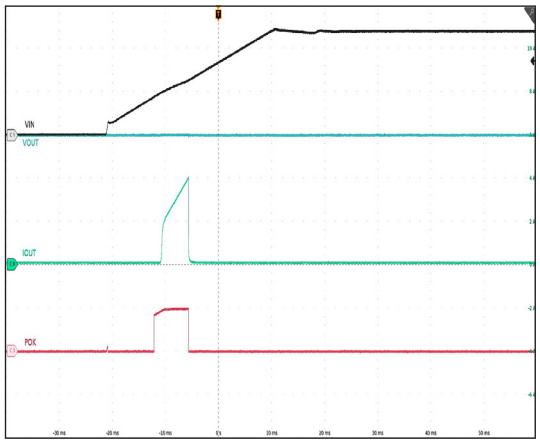
OCP during Startup by EN



VIN (5V/div)
VOUT (5V/div)
IOUT (2A/div)
POK (5V/div)
EN (5V/div)

4ms/div

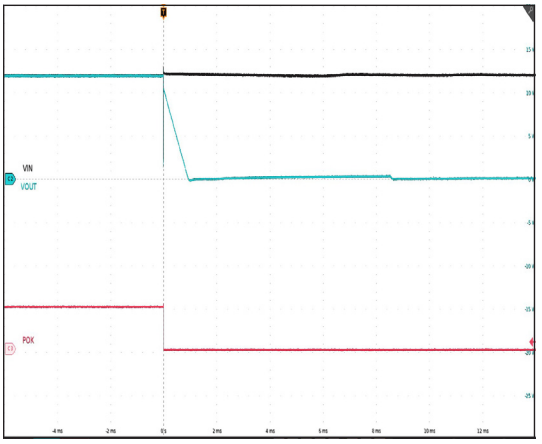
OCP during Startup by Vin (EN=High)



VIN (5V/div)
VOUT (5V/div)
IOUT (2A/div)
POK (5V/div)

10ms/div

Short FET's Gate during Normal Operation (I_{OUT}=20A)



VIN (5V/div)
VOUT (5V/div)
POK (5V/div)

2ms/div

General Information

The AOZ17517QI is an N-channel MOSFET co-packaged with a smart hot swap controller. It is suited for High-side current limiting and fusing in hot-swap applications. It can be used either alone, or in a parallel configuration for higher current applications.

Enable

The EN pin is the ON/OFF control for the power switch. The device is enabled when EN pin is higher than V_{EN_H}, VDD is not in under-voltage lockout state, VDD > $V_{DD\_UVLO\_R}$, and POK is released high. EN pin can be driven to a logic high or logic low state to guarantee operation. The EN pin has an internal pull-up current generator connected to the internal LDO(VDD), therefore, if the pin is not connected to an external controller IC, it goes to the ON-state (device enabled). The 5 µA EN bias current can be used to charge an external capacitor to delay the enable time.

Internal LDO (VDD)

The internal LDO (Low Drop Out) regulator generates 5V from VIN to bias the internal circuits. The LDO should be able to supply at least 30mA. The recommended decoupling capacitor in the VDD pin is 2.2 µF to 10 µF. The VDD voltage is monitored for UVLO.

Input Under-Voltage Lockout (UVLO)

The under-voltage lockout (UVLO) circuit monitors the VDD voltage. The power switch is only allowed to turn on when input voltage is higher than UVLO threshold ($V_{DD\_UVLO\_R}$). Otherwise the switch is off.

Current Monitor (IMON) and Current Sense (ISENSE)

IMON and ISENSE provide output current information. The IC supplies the current 10 µA/A (per switch current) from these two pins. Resistors from pins to ground convert the current information into voltage level.

An IMON current, proportional to the load current flowing through the FET, is imposed on an external R_{IMON}, converting the sensed current into a voltage. A capacitor in parallel with the IMON resistor can be used to low−pass filter the IMON signal without affecting any internal operation of the device.

In parallel configuration, the IMON pins of the parallel devices have to be connected together. The voltage on the IMON pin (Bus) represents the average of the currents through the devices on the same bus (I_{out}/N).

The ISENSE pin also sources current 10 µA/A (per switch current). A resistor from the pin to ground converts the current info into voltage level. The voltage on ISENSE pin is used for the overcurrent protection and current sharing.

In parallel configuration, the voltage on the ISENSE pin represents the current through each individual device.

Programmable Over-Current Protection (IOCP)

A resistor from the IOCP pin to ground set the over current threshold. The IOCP bias current, 10 µA, with the external resistor sets the voltage threshold for the current limit. The voltage on the ISENSE pin is used to compare with this voltage threshold for the current limit loop.

During soft start, the current limit is clamped according to the SOA limits.

The IOCP pin voltage determines the over−current indication point by comparing its voltage against the ISENSE pin voltage. The IOCP voltage can be applied by an external voltage source, such as D/A converter, or developed across a programming resistor to ground by the IOCP bias current, 10 µA. The recommended range of IOCP voltage is 0.2 − 1.55V.

A 250 µs current limit timer (t_{HOLD}) starts after over-current detection. Once the timer elapses, the internal MOSFET is shut down and the POK indicator is pulled to low status, to inform the system controller that a shutdown not due to EN.

Short Circuit Protection

During steady state, if the output voltage drops > 65mV below input voltage (equivalent to 100A), the device interprets as short circuit condition and shuts down immediately (<500 ns).At the same time, FLT_OC pin is asserted, and POK is pulled low.

Programmable Soft Start

The AOZ17517QI start up delay and soft start time are programmable externally through SS pin. The soft start delay and ramp time can be estimated using the equations below:

$$C_{SS} = \frac{t_{ON} \times I_{SS} \times AV_{SS}}{V_{IN}}$$

where C_{SS} is in nF and t_{ON} in ms.

Iss=6 uA and AVss=8V/V

The minimum soft start time (Css = open) is 1 ms. The typical Css values for different tss are shown in Table 1.

Table 1. Soft Start Time vs Css Capacitor Value

tss(ms)	Css(nF)	tss(ms)	Css(nF)
10	47	60	270
20	82	70	330
30	120	80	330
40	180	90	470
50	220	100	470

The actual soft start time may not be equal to the estimated value from the above equation if the operating condition exceeds the SOA of the power switch.

The maximum load capacitor value AOZ17517QI can power up depends on the soft-start time. When VIN=12V, R_{Isense}=2kΩ, R_{load}=2.4Ω, the relationship for different quantity devices in parallel operations are shown in the Figure 5.

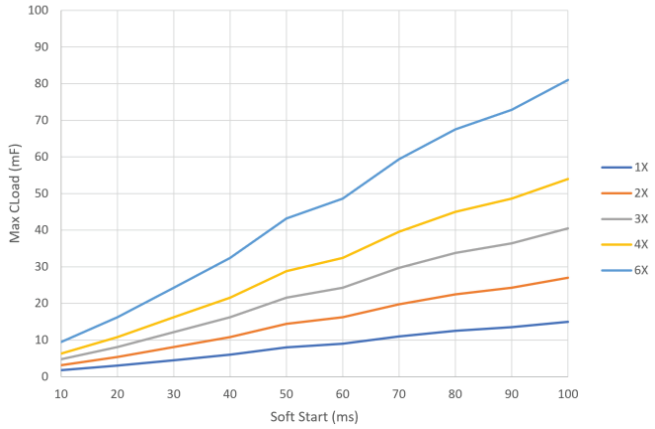


Figure 5. Maximum CLOAD vs. Softstart Time(Isense=2kΩ, Rload22.4Ω, VIN=12V)

FLT_OC

FLT_OC is an open-drain, active-low output that reports the over-current warning when VOUT ≥ 85%VIN. Once VISENSE is higher than 85% of the IOCP voltage, FLT_OC is driven low. When VISENSE drops below the threshold, FLT_OC is released high again. The VFLT_OC_TH trip points are based on a percentage of VIOCP. Recommended pull up resistor is 100 kΩ to VDD.

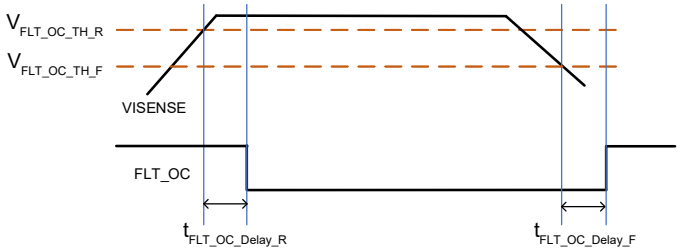


Figure 6. FLT_OC Delay Time

POK

POK is open−drain output that requires an external pull up 100kΩ resistor, RPOK, to VDD/external power supply.

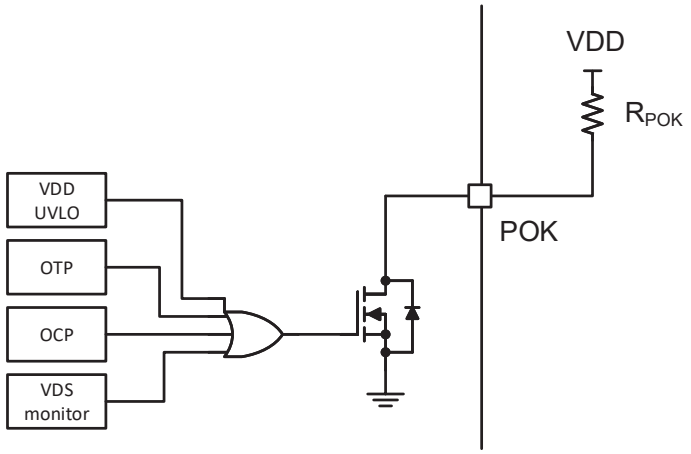


Figure 7. POK Block Diagram

POK is internally pulled low under the following conditions:

- VDD voltage is below UVLO voltage at any time.
- EN disabled and VDS_OK is false (indicates a short from VIN to VOUT. The device is prevented from powering up. The device is allowed to power up once VOUT < VDS_OK.).
- Over current
- Over Temperature

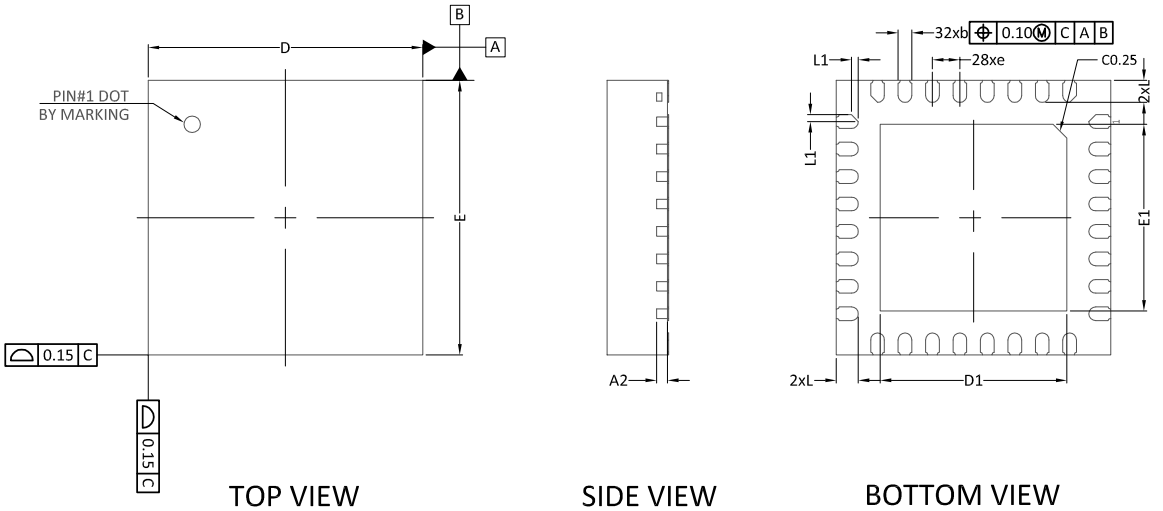
When multiple AOZ17517QI are paralleled together, the POK pin should be connected together to synchronize hiccup timing and prevent cascading faults.

Thermal Monitor (TMON) and Thermal Shut Down Protection (TSD)

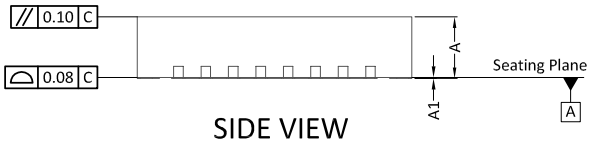
TMON is a voltage output proportional to controller's die temperature and provides a signal proportional to the die temperature on the TMON pin. TMON has a voltage of 450mV at 25°C and temperature gain of 10mV/°C.

Thermal shutdown protects device from excessive temperature. The power switch is turned off when the die temperature reaches thermal shutdown threshold of 150°C. There is a 25°C hysteresis. The power switch is allowed to turn on again if die temperature drops below approximately 125°C. If EN is high, the device will turn on when the junction temperate drops below the threshold.

Package Dimensions, QFN5x5-32L



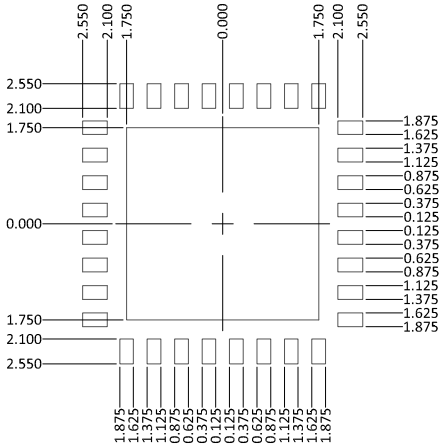
TOP VIEW SIDE VIEW BOTTOM VIEW



SIDE VIEW

SYMBOLS	DIM. IN MM			DIM. IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.000	1.100	1.200	0.039	0.043	0.047
A1	0.000	---	0.050	0.000	---	0.002
A2	0.203 REF			0.008 REF		
D	4.900	5.000	5.100	0.193	0.197	0.201
D1	3.350	3.400	3.450	0.132	0.134	0.136
E	4.950	5.000	5.050	0.195	0.197	0.199
E1	3.300	3.400	3.500	0.130	0.134	0.138
L	0.350	0.400	0.450	0.014	0.016	0.018
L1	0.075	0.125	0.175	0.003	0.005	0.007
b	0.200	0.250	0.300	0.008	0.010	0.012
e	0.500 BSC			0.020 BSC		

RECOMMENDED LAND PATTERN



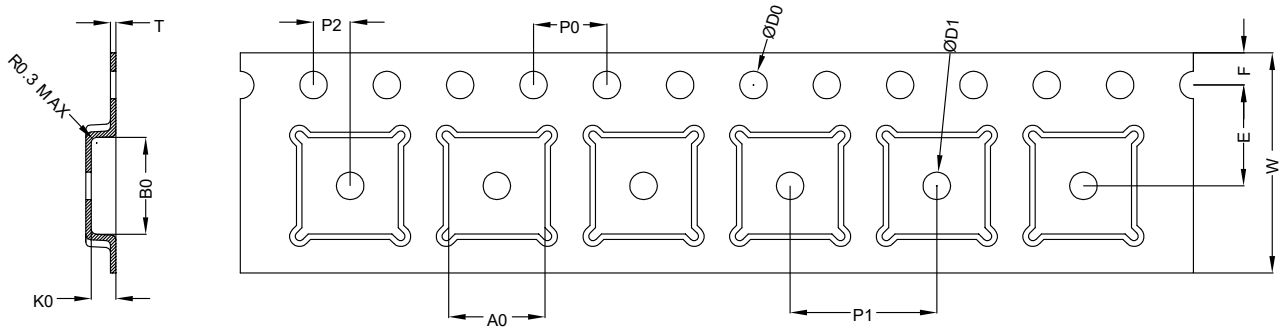
UNIT: mm

NOTE:

1. CONTROLLED DIMENSIONS ARE IN MILLIMETERS. DIMENSIONS IN INCHES ARE CONVERTED AS REFERENCE ONLY.

Tape and Reel Dimensions, QFN5x5-32L

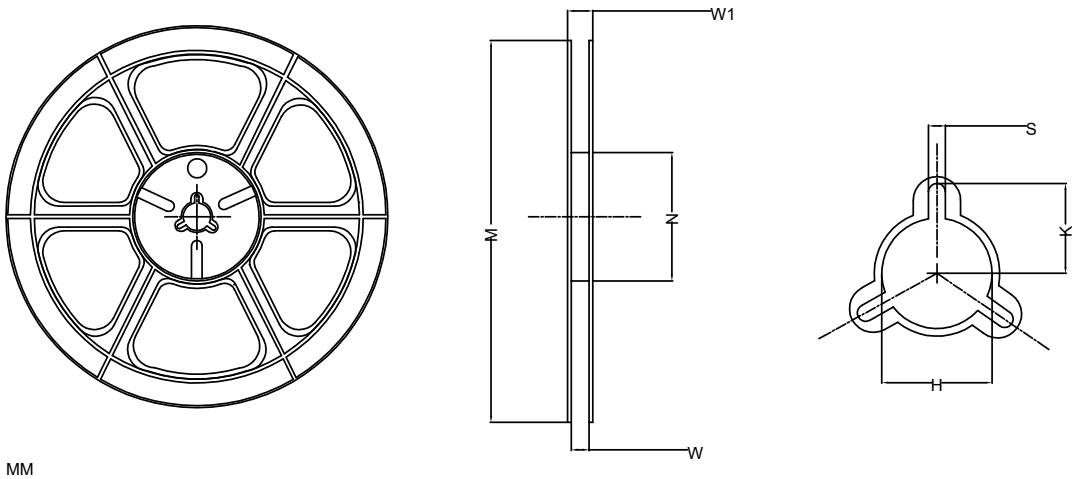
Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	W	E	F	P0	P1	P2	T
QFN5x5	5.25 ±0.10	5.25 ±0.10	1.35 ±0.10	1.50 +0.10 -0.00	1.50 MIN	12.00 +0.30 -0.10	5.50 ±0.05	1.75 ±0.10	4.00 ±0.10	8.00 ±0.10	2.00 ±0.05	0.30 ±0.05

Reel



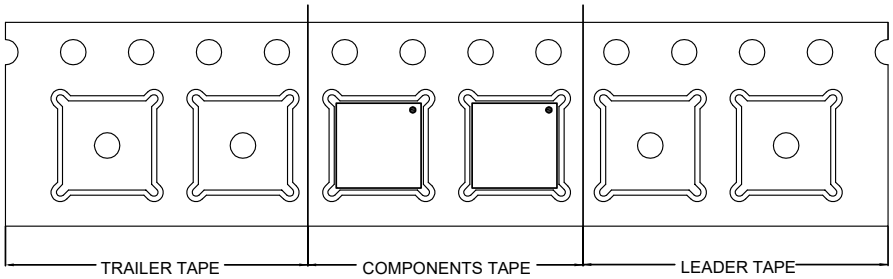
UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S
12 mm	Ø330	Ø330 ±0.50	Ø97.00 ±0.10	13.0 ±0.30	17.40 ±1.00	Ø13.0 +0.5 -0.2	10.6	2.00 ±0.50

Carrier Tape

Leader / Trailer & Orientation

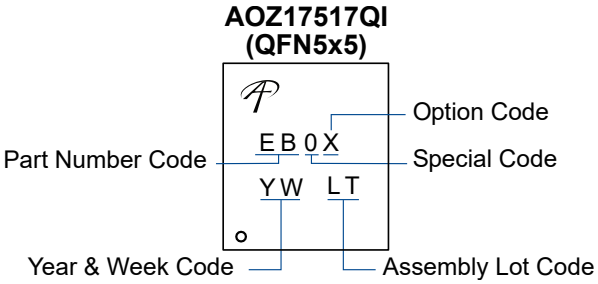
SPECIAL



Unit Per Reel: 3000pcs

TRAILER TAPE 300mm MIN. | COMPONENTS TAPE ORIENTATION IN POCKET | LEADER TAPE 500mm MIN.

Part Marking



Part Number	Fault Recovery	Marking Code
AOZ17517QI-01	Auto-Restart	EB01
AOZ17517QI-02	Latch-Off	EB02

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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.