AOZ1341

Dual Channel USB Switch

General Description

The AOZ1341 is a member of Alpha and Omega Semiconductor's dual channel power distribution switch family intended for applications where heavy capacitive loads and short-circuits are likely to be encountered. This device incorporates 70 mΩ N-channel MOSFET power switches for power-distribution systems that require multiple power switches in a single package. Each switch is controlled by a logic enable input. Gate drive is provided by an internal charge pump designed to control the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

The AOZ1341 is available in an Exposed Pad MSOP-8 or an SO8 8-pin package and is rated over the -40 °C to +85 °C ambient temperature range.

Features

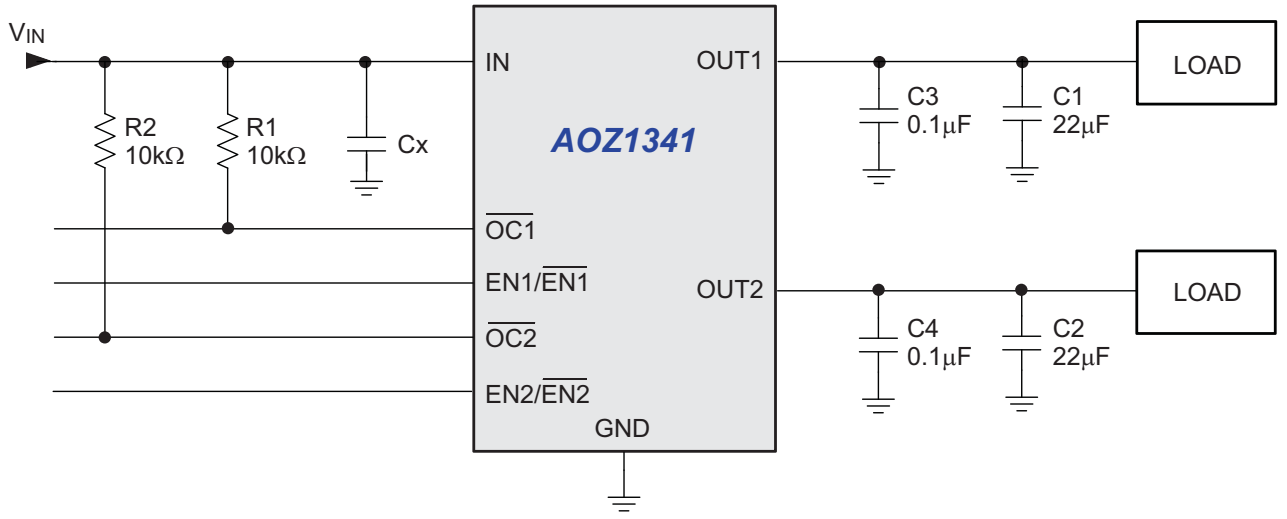
- Typical 70 mΩ (NFET)
- 1 A maximum continuous current
- V_{IN} Range: 2.7 V to 5.5 V
- Open Drain Fault Flag
- Fault Flag deglitched (blanking time)
- Discharge switch for shutdown
- Thermal shutdown
- Reverse current blocking
- Packages: Exposed Pad MSOP-8 and SO-8

Applications

- Notebook Computers
- Desktop Computers

Green Product

Typical Application

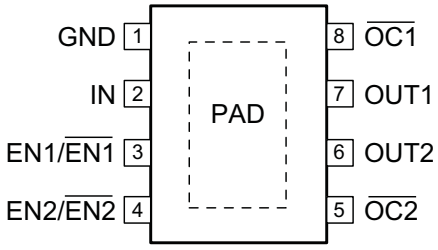


Ordering Information

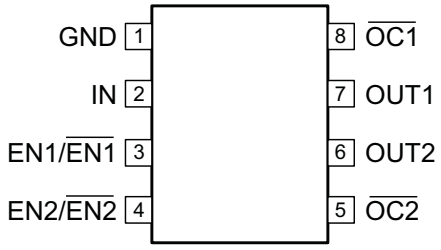
Part Number	Maximum Continuous Current	Typical Short-circuit Current Limit	Enable Setting	Package	Environmental
AOZ1341AI	1 A	1.5 A	Active Low	SO-8	Green Product RoHS Compliant
AOZ1341AI-1			Active High		
AOZ1341EI			Active Low	Exposed Pad MSOP-8	
AOZ1341EI-1			Active High		

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/web/quality/rohs_compliant.jsp for additional information.

Pin Configuration



Exposed Pad MSOP-8
(Top View)



SO-8
(Top View)

Pin Description

Pin Name	Pin Number	Pin Function
GND	1	Ground
IN	2	Input voltage
EN1/$\overline{EN1}$	3	Enable input, logic high/logic low turns on power switch IN-OUT1
EN2/$\overline{EN2}$	4	Enable input, logic high/logic low turns on power switch IN-OUT2
$\overline{OC2}$	5	Overcurrent, open-drain output, active low, IN-OUT2
OUT2	6	Power-switch output, IN-OUT2
OUT1	7	Power-switch output, IN-OUT1
$\overline{OC1}$	8	Overcurrent, open-drain output, active low, IN-OUT1

Absolute Maximum Ratings

Exceeding the Absolute Maximum Ratings may damage the device.

Parameter	Rating
Input Voltage (V_{IN})	6 V
Enable Voltage (V_{EN})	6 V
Storage Temperature (T_S)	-55 °C to +150 °C
Maximum Continuous Current	1 A
ESD Rating(1)	2 kV

Note:

1. Devices are inherently ESD sensitive, handling precautions are required. Human body model is a 100 pF capacitor discharging through a 1.5 kΩ resistor.

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Recommended Operating Conditions.

Parameter	Rating
Input Voltage (V_{IN})	+2.7 V to +5.5 V
Junction Temperature (T_J)	-40 °C to +125 °C
Package Thermal Resistance	
Exposed Pad MSOP-8 (Θ_{JA})	60 °C/W
SO-8 (Θ_{JA})	115 °C/W

Electrical Characteristics

T_A = 25 °C, V_{IN} = 5.5 V, V_{EN} = 0 V, unless otherwise specified.

Symbol	Parameter	Conditions(3)		Min.	Typ.	Max.	Units
POWER SWITCH							
$R_{DS(ON)}$	Switch On-Resistance	V_{IN} = 5.5 V, I_O = 1 A			70	135	mΩ
t_r	Rise Time, Output	V_{IN} = 5.5 V	C_L = 1 µF, R_L = 5 Ω		0.6	1.5	ms
		V_{IN} = 2.7 V			0.4	1	
t_f	Fall time, output	V_{IN} = 5.5 V		0.05		0.5	ms
		V_{IN} = 2.7 V		0.05		0.5	
	FET Leakage Current	Out connect to ground, 2.7 V ≤ V_{IN} ≤ 5.5 V, $V_{(\overline{ENx})}$ = V_{IN} or $V_{(ENx)}$ = 0 V	-40 °C ≤ T_J ≤ 125 °C(2)		1		µA
ENABLE INPUT $\overline{EN}$							
V_{IH}	High-level Input Voltage	2.7 V ≤ V_{IN} ≤ 5.5 V		2.0			V
V_{IL}	Low-level Input Voltage	2.7 V ≤ V_{IN} ≤ 5.5 V				0.8	V
I_I	Input Current			-0.5		0.5	µA
t_{on}	Turn-on Time	C_L = 100 µF, R_L = 5 Ω				3	ms
t_{off}	Turn-off Time	C_L = 100 µF, R_L = 5 Ω				10	
CURRENT LIMIT							
I_{OS}	Short-circuit Output Current (per Channel)	$V_{(IN)}$ = 2.7 V to 5.5 V, OUT connected to GND, device enable into short-circuit		1.1	1.5	1.9	A
I_{OC_TRIP}	Overcurrent Trip Threshold (per Channel)	$V_{(IN)}$ = 5 V, current ramp (≤ 100 A/s) on OUT		1.0	1.6	2.0	A
SUPPLY CURRENT							
	Supply Current, Low-level Output	No load on OUT, 2.7 V ≤ V_{IN} ≤ 5.5 V, $V_{(\overline{ENx})}$ = V_{IN} or $V_{(ENx)}$ = 0 V	T_J = 25°C		0.5	1	µA
			-40 °C ≤ T_J ≤ 125 °C(2)		0.5	5	
	Supply current, High-level Output	No load on OUT, $V_{(\overline{ENx})}$ = 0 V or $V_{(ENx)}$ = V_{IN}	T_J = 25 °C		65	81	µA
			-40 °C ≤ T_J ≤ 125 °C(2)		65	90	
	Reverse Leakage Current	$V_{(OUTx)}$ = 5.5 V, IN = ground			0.2		µA

Electrical Characteristics (Continued)

T_A = 25 °C, V_{IN} = 5.5 V, V_{EN} = 0 V, unless otherwise specified.

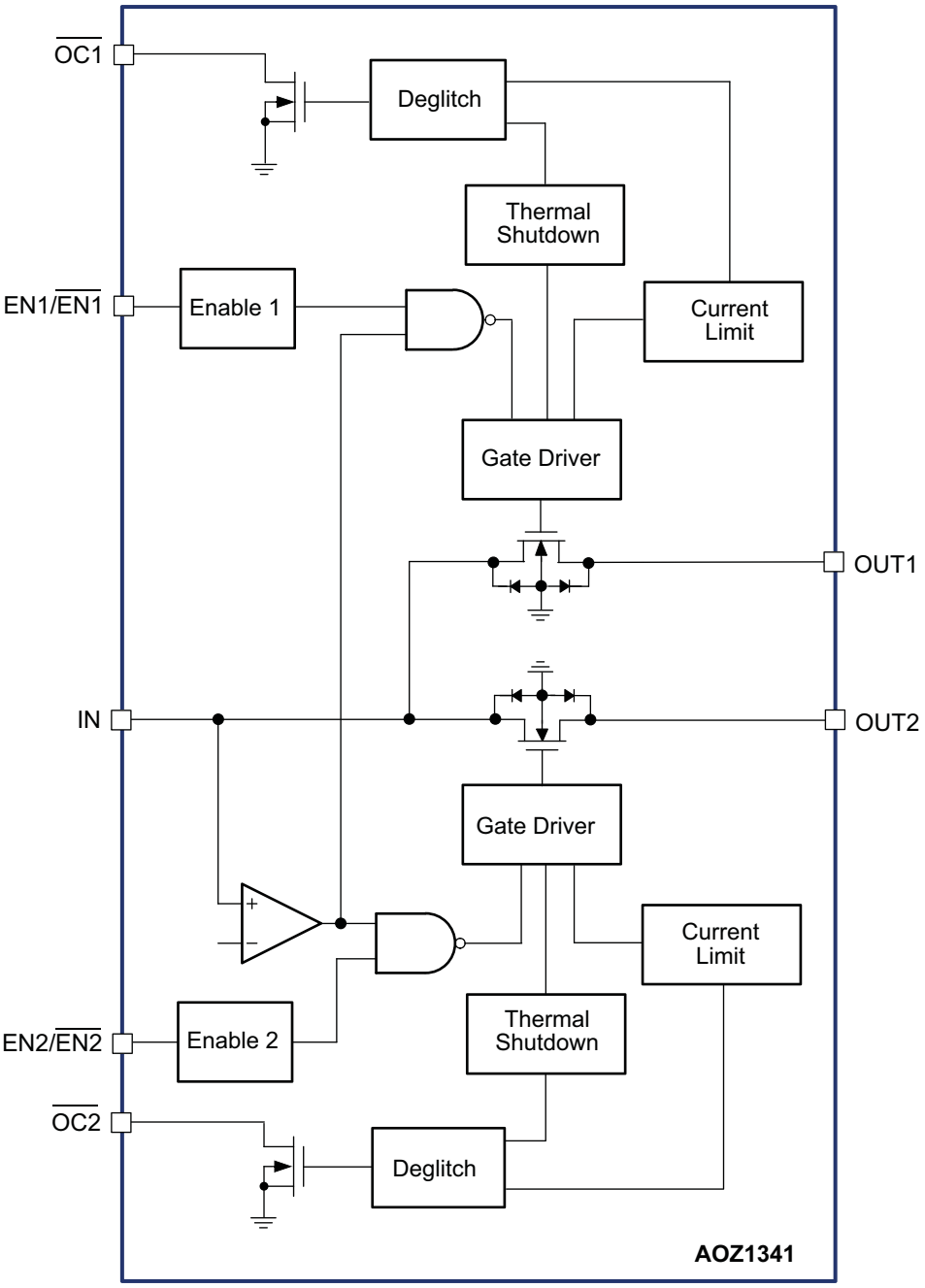
Symbol	Parameter	Conditions[3]	Min.	Typ.	Max.	Units
UNDERVOLTAGE LOCKOUT						
	Low-level voltage, IN		2.0		2.5	V
	Hysteresis, IN			200		mV
OVERCURRENT $\overline{OC1}$ AND $\overline{OC2}$						
	Output Low Voltage $V_{OL(OCx)}$	$I_{O(OCx)}$ = 5 mA			0.4	V
	Off-state Current	$V_{O(OCx)}$ = 5 V or 3.3 V			1	µA
	OC_L Deglitch	OCx assertion or deassertion	4	8	15	ms
THERMAL SHUTDOWN						
	Thermal Shutdown Threshold		135			°C
	Recovery from Thermal Shutdown		105			°C
	Hysteresis			30		°C

Note:

2. Parameters are guaranteed by design only and not production tested.

3. Pulse testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

Functional Block Diagram



Functional Characteristics

Figure 1. Turn-Off Delay and Fall Time with 1μF Load (Active Low)

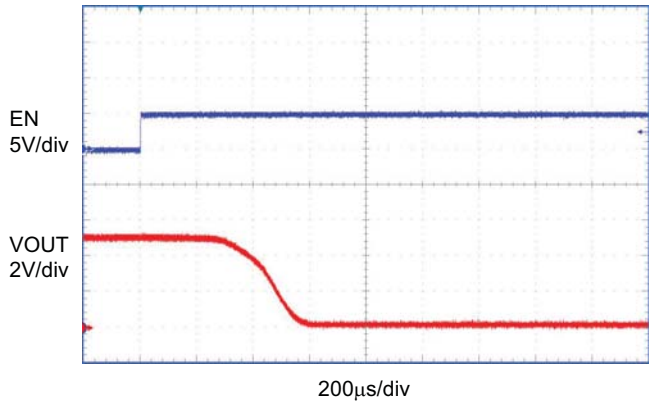


Figure 2. Turn-On Delay and Rise Time with 1μF Load (Active Low)

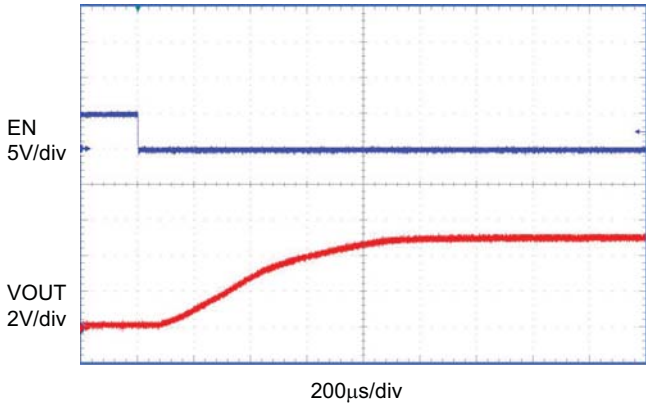


Figure 3. Turn-Off Delay and Fall Time with 100μF Load (Active Low)

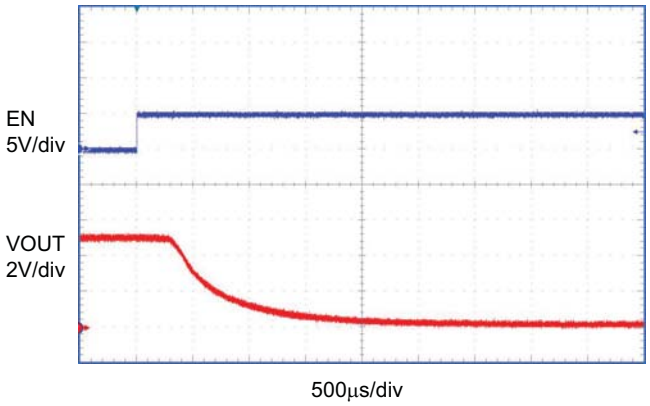


Figure 4. Turn-On Delay and Rise Time with 100μF Load (Active Low)

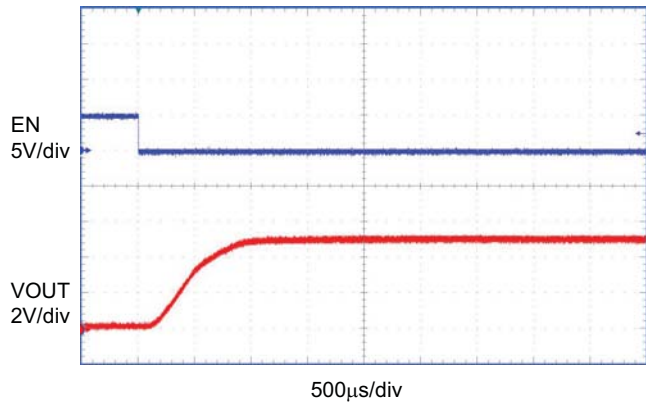


Figure 5. Short-circuit Current, Device Enable to Short

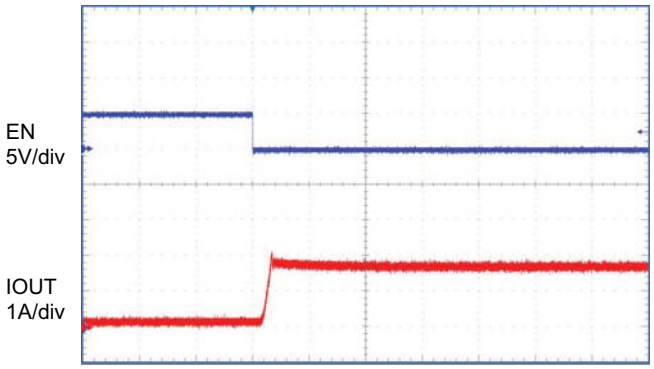
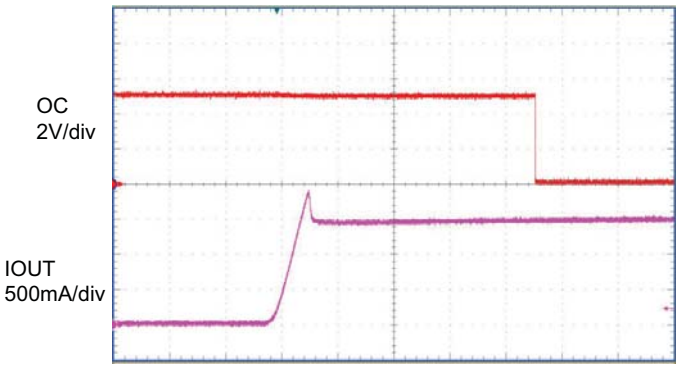


Figure 6. 0.6Ω Load Connected to Vout



Functional Characteristics (Continued)

Figure 7. Inrush Current with Different Load Capacitance

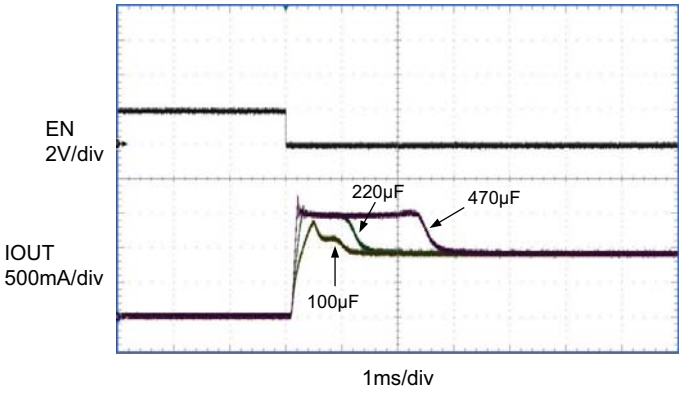
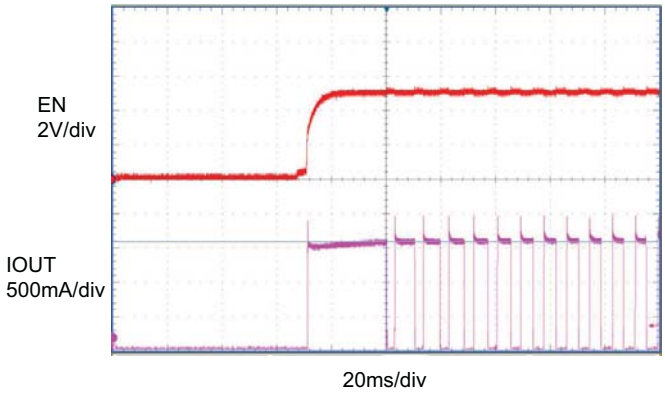


Figure 8. Short Circuit Current Limit



Typical Characteristics

Figure 9. Supply Current, Output Enabled vs. Junction Temperature

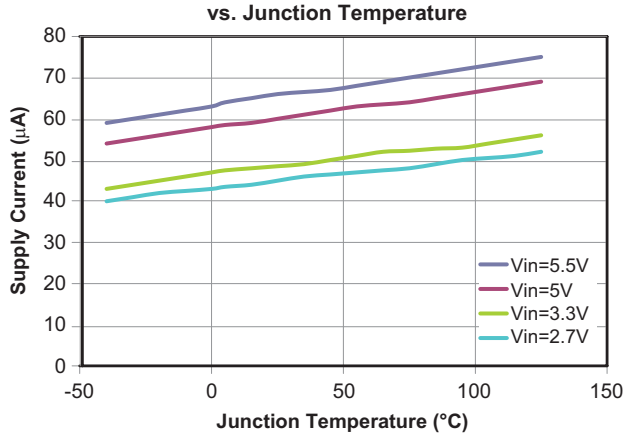


Figure 10. Supply Current, Output Disabled vs. Junction Temperature

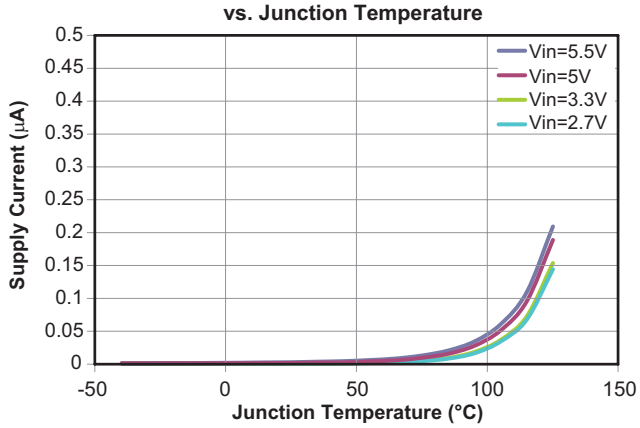


Figure 11. Rds(on) vs. Ambient Temperature

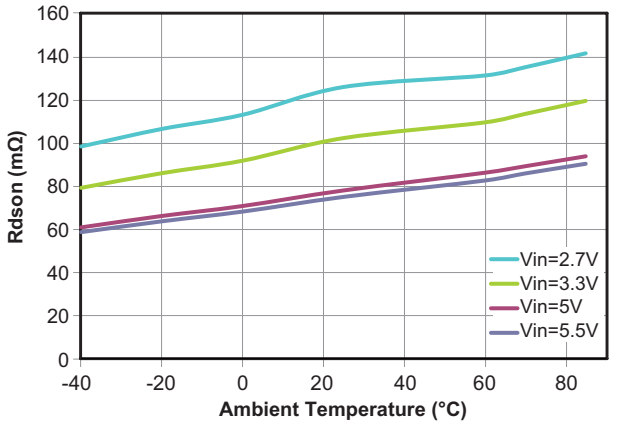
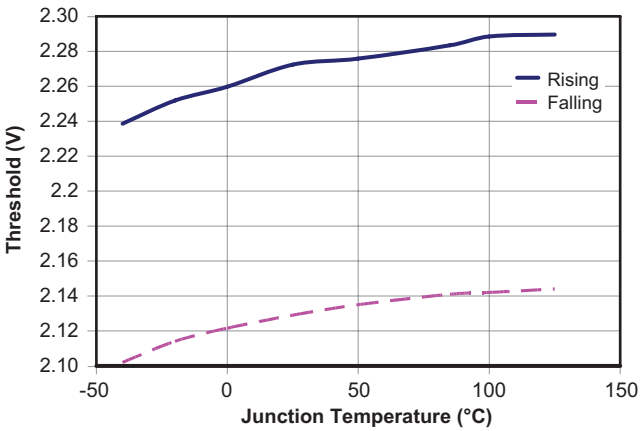


Figure 12. UVLO Threshold vs. Junction Temperature



Typical Characteristics (Continued)

Figure 13. OCP Trip Current vs. Input Voltage

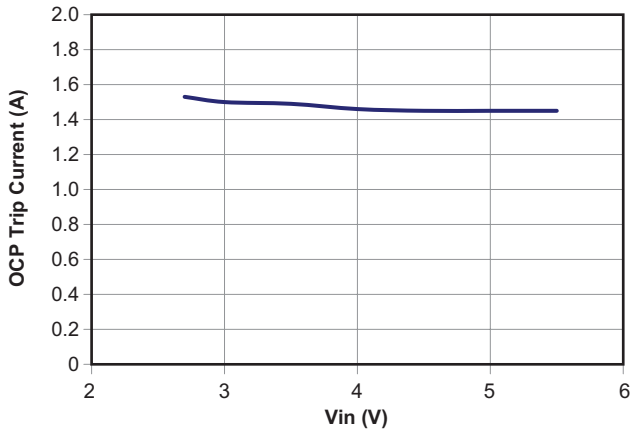


Figure 14. Turn On Time vs Input Voltage

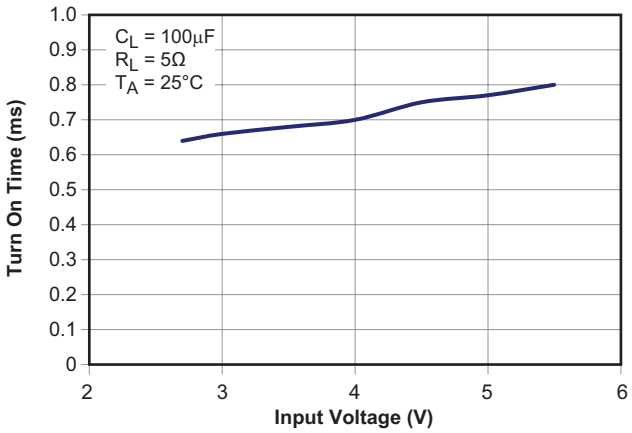


Figure 15. Turn Off Time vs Input Voltage

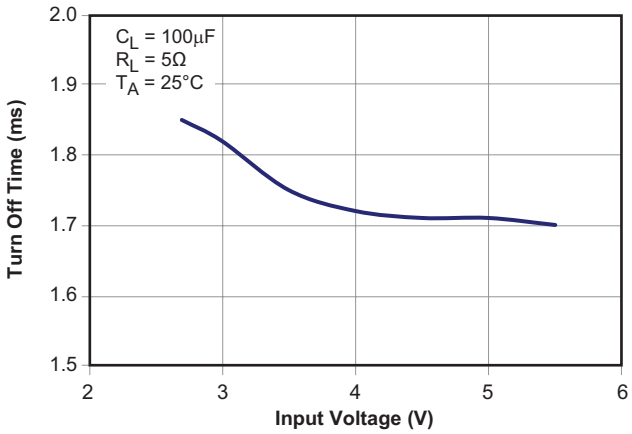


Figure 16. Rise Time vs Input Voltage

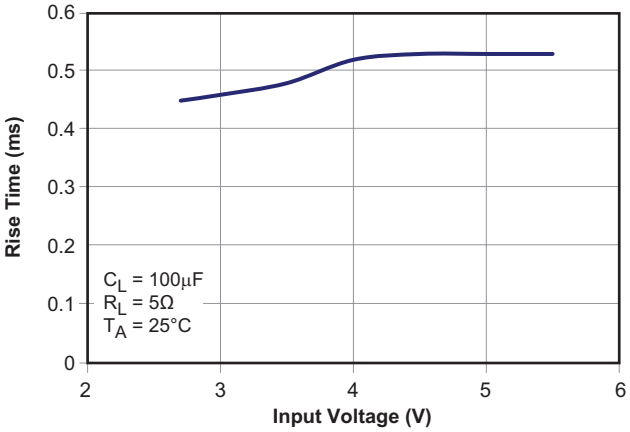
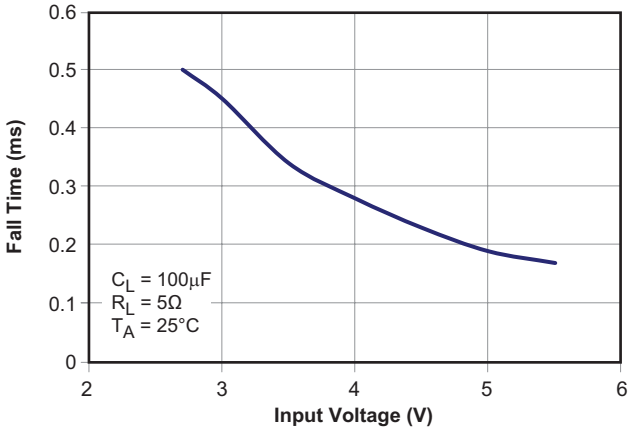


Figure 17. Fall Time vs Input Voltage



Detailed Description

The AOZ1341 is a member of Alpha and Omega Semiconductor's dual channel power distribution switch family intended for applications where heavy capacitive loads and short-circuits are likely to be encountered. This device incorporates 70 mΩ N-channel MOSFET power switches for power-distribution systems that require multiple power switches in a single package. Each switch is controlled by a logic enable input. Gate drive is provided by an internal charge pump designed to control the power-switch rise and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

Power Switch

The power switch is a N-channel MOSFET with a low on-state resistance capable of delivering 1 A of continuous current. Configured as a high-side switch, the MOSFET will go into high impedance when disabled. Thus, preventing current flow from OUT to IN and IN to OUT.

Charge Pump

An internal charge pump supplies power to the circuits and provides the necessary voltage to drive the gate of the MOSFET beyond the source. The charge pump is capable of operating down to a low voltage of 2.7 Volts.

Driver

The driver controls the voltage on the gate to the power MOSFET switch. This is used to limit the large current surges when the switch is being turned On and Off. Proprietary circuitry controls the rise and fall time of the output voltages.

Enable

The logic enable disables the power switch, charge pump, gate driver, logic device, and other circuitry to reduce the supply current. When the enable receives a logic high the supply current is reduced to approximately 1 μA. The enable input is compatible with both TTL and CMOS logic levels.

Over-current

The over-current open drain output is asserted (active low) when an over-current condition occurs. The output will remain asserted until the over-current condition is removed. A 15 ms deglitch circuit prevents the over-current from false triggering.

Thermal Shut-down Protection

When the output load exceeds the current-limit threshold the device limits the output current to a safe level by switching into a constant-current mode, pulling the overcurrent (OC) logic output low.

During current limit conditions the increasing power dissipation in the chip causing the die temperature to rise. When the die temperature reaches a specified level the thermal shutdown circuitry will shutdown the device. The thermal shutdown will cycle repeatedly until the short circuit condition is resolved.

Applications Information

Input Capacitor Selection

The input capacitor prevents large voltage transients from appearing at the input, and provides the instantaneous current needed each time the switch turns on and also to limit input voltage drop. The input capacitor t also prevents high-frequency noise on the power line from passing through the output of the power side. The choice of the input capacitor is based on its ripple current and voltage ratings rather than its capacitor value. The input capacitor should be located as close to the VIN pin as possible. A 0.1 μF ceramic cap is recommended but higher capacitor values will further reduce the voltage drop at the input.

Output Capacitor Selection

The output capacitor acts in a similar way. A small 0.1 μF capacitor prevents high-frequency noise from going into the system. Also, the output capacitor has to supply enough current for a large load that it may encounter during system transients. This bulk capacitor must be large enough to supply fast transient load in order to prevent the output voltage from dropping.

Power Dissipation Calculation

Calculate the power dissipation for normal load condition using the following equation:

$$P_D = R_{ON} \times (I_{OUT})^2$$

The worst case power dissipation occurs when the load current hits the current limit due to over-current or short circuit faults. The power dissipation under these conditions can be calculated using the following equation:

$$P_D = (V_{IN} - V_{OUT}) \times I_{LIMIT}$$

Layout Guidelines

Proper PCB layout is important for improving the thermal and overall performance of the AOZ1341. To optimize the switch response time to output short-circuit conditions keep all traces as short as possible to reduce the effect of unwanted parasitic inductance.

Place the input and output bypass capacitors as close as possible to the IN and OUT pins. The input and output PCB traces should be as wide as possible for the given PCB space.

Use a ground plane to enhance the power dissipation capability of the device.

USB Power Distribution Application

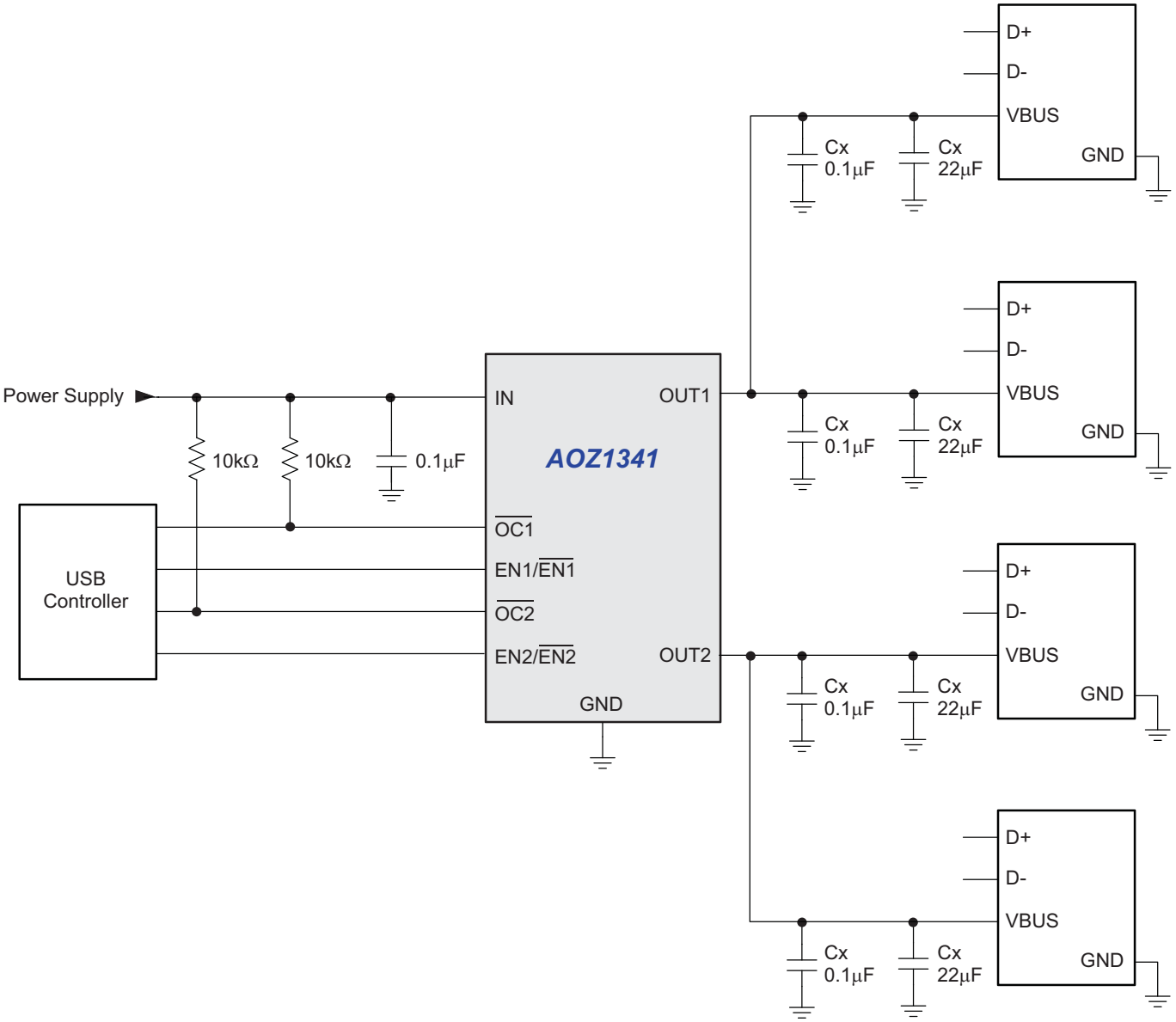
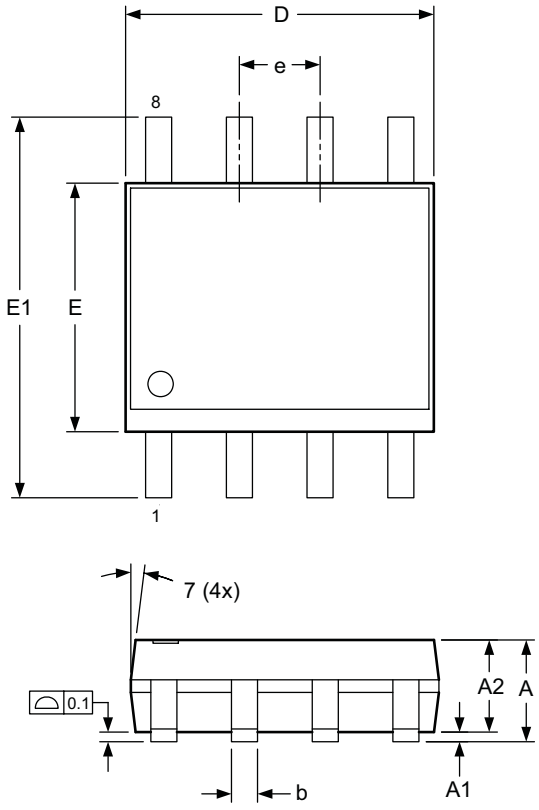
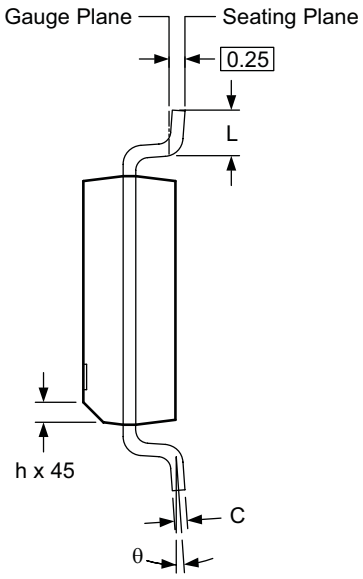


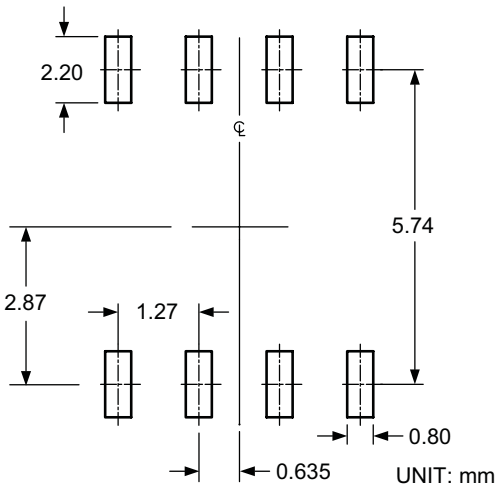
Figure 18. Typical Four-Port USB Host/Self-Powered Hub Applications Circuitry

Package Dimensions, SO-8





RECOMMENDED LAND PATTERN



Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	1.35	1.65	1.75
A1	0.10	—	0.25
A2	1.25	1.50	1.65
b	0.31	—	0.51
c	0.17	—	0.25
D	4.80	4.90	5.00
E	3.80	3.90	4.00
e	1.27 BSC		
E1	5.80	6.00	6.20
h	0.25	—	0.50
L	0.40	—	1.27
θ	0°	—	8°

Dimensions in inches

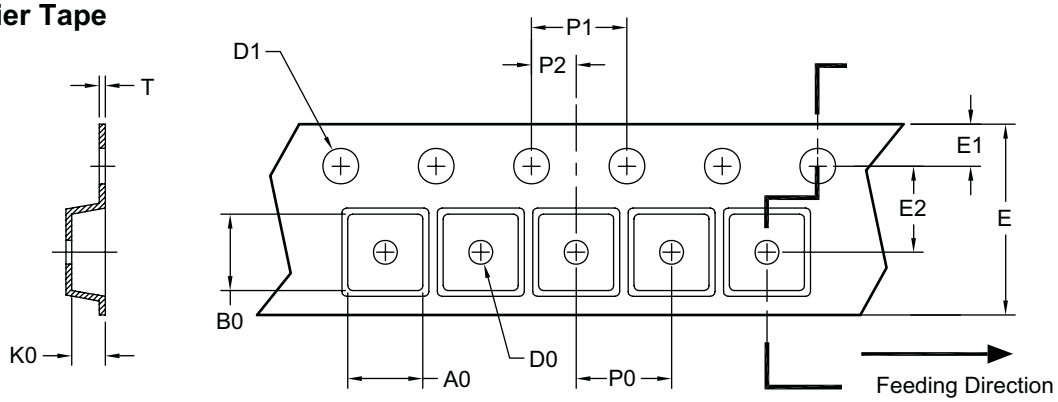
Symbols	Min.	Nom.	Max.
A	0.053	0.065	0.069
A1	0.004	—	0.010
A2	0.049	0.059	0.065
b	0.012	—	0.020
c	0.007	—	0.010
D	0.189	0.193	0.197
E	0.150	0.154	0.157
e	0.050 BSC		
E1	0.228	0.236	0.244
h	0.010	—	0.020
L	0.016	—	0.050
θ	0°	—	8°

Notes:

1. All dimensions are in millimeters.
2. Dimensions are inclusive of plating
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 6 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

Tape and Reel Dimensions, SO-8

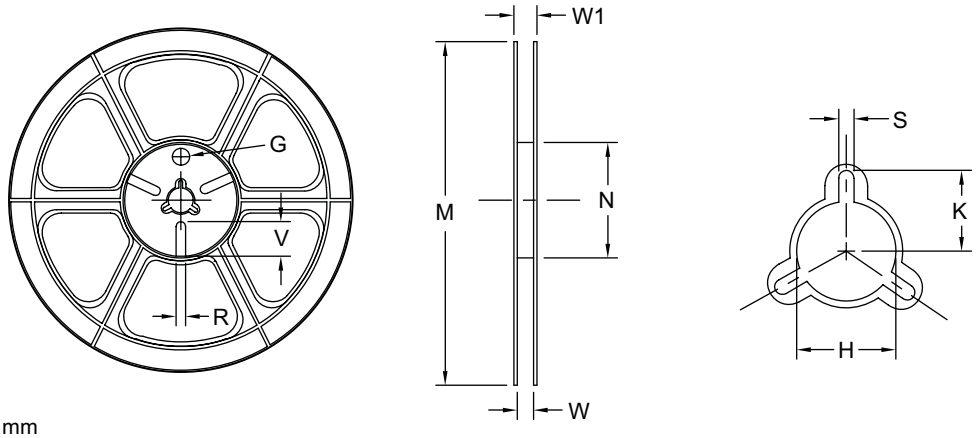
Carrier Tape



UNIT: mm

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
SO-8 (12mm)	6.40 ±0.10	5.20 ±0.10	2.10 ±0.10	1.60 ±0.10	1.50 ±0.10	12.00 ±0.10	1.75 ±0.10	5.50 ±0.10	8.00 ±0.10	4.00 ±0.10	2.00 ±0.10	0.25 ±0.10

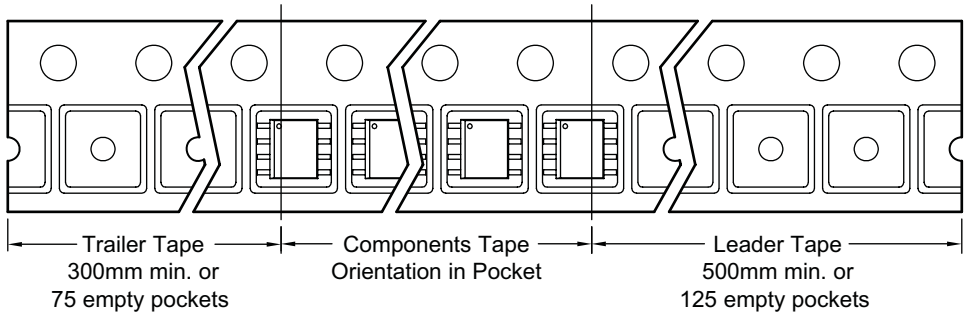
Reel



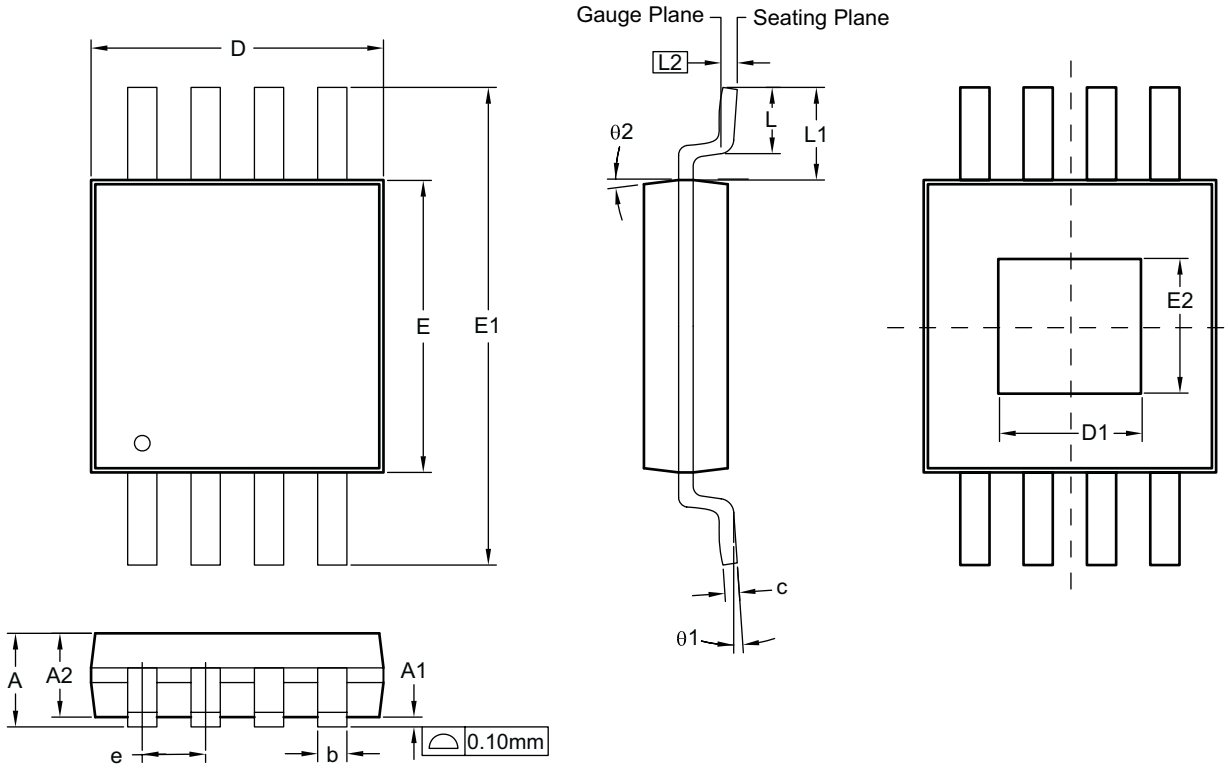
UNIT: mm

Tape Size	Reel Size	M	N	W	W1	H	K	S	G	R	V
12mm	ø330	ø330.00 ±0.50	ø97.00 ±0.10	13.00 ±0.30	17.40 ±1.00	ø13.00 +0.50/-0.20	10.60	2.00 ±0.50	—	—	—

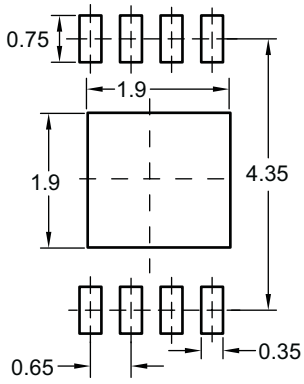
Leader/Trailer and Orientation



Package Dimensions, Exposed Pad MSOP-8



RECOMMENDED LAND PATTERN



Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	0.81	1.02	1.12
A1	0.05	—	0.15
A2	0.76	0.86	0.97
b	0.25	0.30	0.40
c	0.13	0.15	0.23
D	2.90	3.00	3.10
D1	1.55	—	1.8
e	0.65 TYP.		
E	2.90	3.00	3.10
E1	4.70	4.90	5.10
E2	1.3	—	1.8
L	0.40	0.55	0.70
L1	0.90	0.95	1.00
L2	0.25 BSC		
θ1	0°	—	6°
θ2	—	12°	—

Dimensions in inches

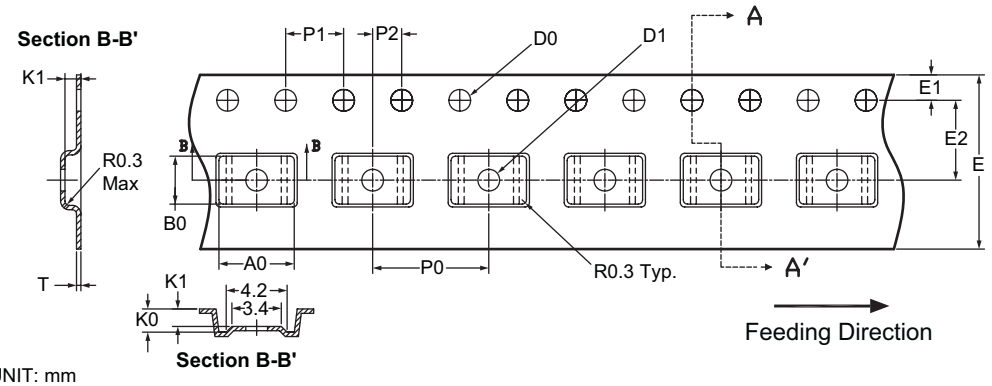
Symbols	Min.	Nom.	Max.
A	0.032	0.040	0.044
A1	0.002	—	0.006
A2	0.030	0.034	0.038
b	0.010	0.012	0.016
c	0.005	0.006	0.010
D	0.116	0.118	0.120
D1	0.06	—	0.07
e	0.026 TYP.		
E	0.116	0.118	0.120
E1	0.185	0.192	0.20
E2	0.05	—	0.07
L	0.016	0.022	0.028
L1	0.035	0.037	0.039
L2	0.010 BSC		
θ1	0°	—	6°
θ2	—	12°	—

Notes:

1. All dimensions are in millimeters.
2. Dimensions are inclusive of plating.
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 6 mils each.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

Tape and Reel Dimensions, Exposed Pad MSO8-P

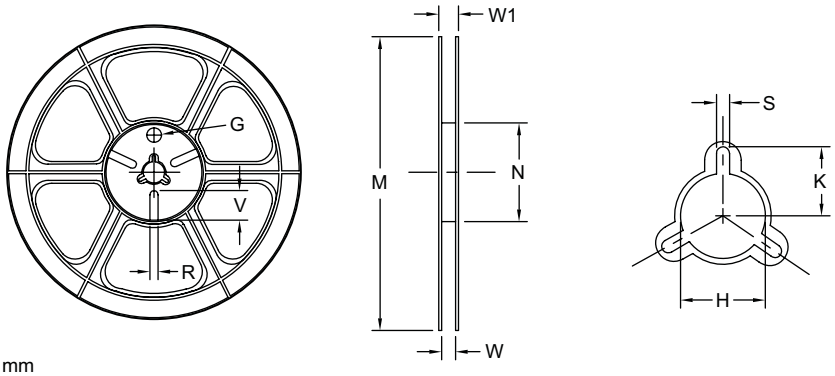
Carrier Tape



UNIT: mm

Package	T	B0	A0	K1	K0	D0	D1	E	E1	E2	P0	P1	P2
MSOP-8	0.30 ±0.05	3.30 ±0.10	5.20 ±0.10	1.20 ±0.10	1.60 ±0.10	ø1.50 +0.1/-0.0	ø1.50 Min.	12.0 ±0.3	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.05	2.00 ±0.05

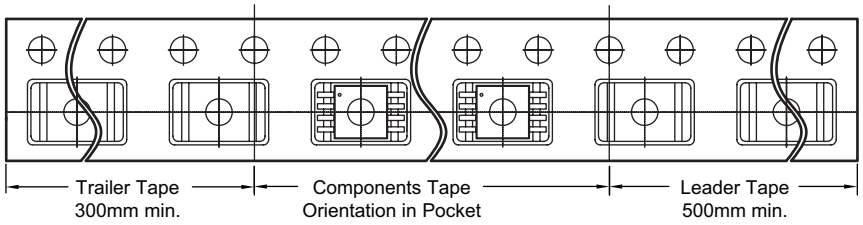
Reel



UNIT: mm

Tape Size	Reel Size	M	N	W	W1	H	K	S	G	R	V
12mm	ø330	ø330.00 ±0.50	ø97.00 ±0.10	13.00 ±0.30	17.40 ±1.00	ø13.00 +0.50/-0.20	10.60	2.00 ±0.50	—	—	—

Leader/Trailer and Orientation

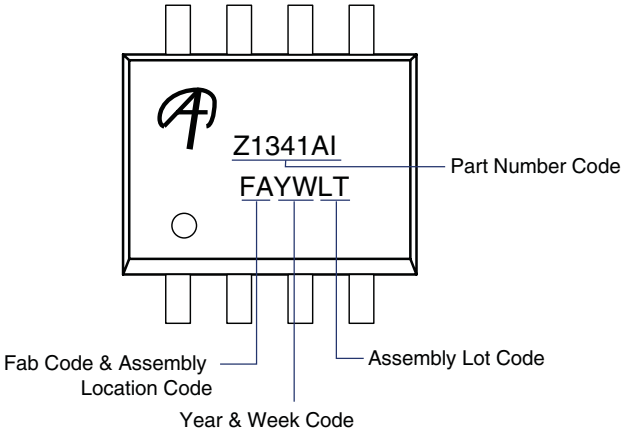


Notes:

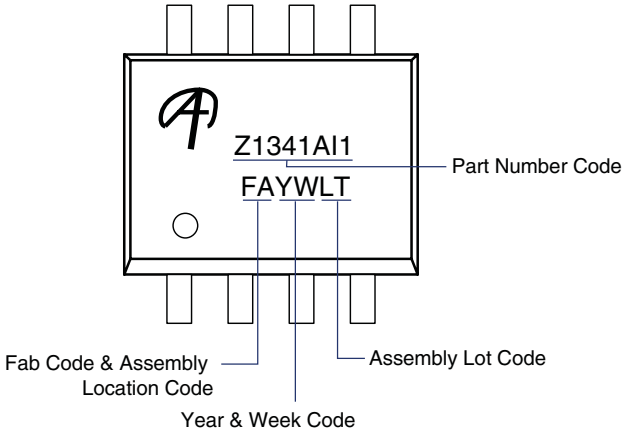
1. 10 sprocket hole pich cumulative tolerance 0.2.
2. Camber not to exceed 1mm in 100mm.
3. A0 and B0 measured on a plane 0.3mm above the bottom of the pocket.
4. K0 measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
5. Pocket position relative to sprocket hole measured as tue position of pocket, not pocket hole.
6. All dimensions in mm.

Part Marking

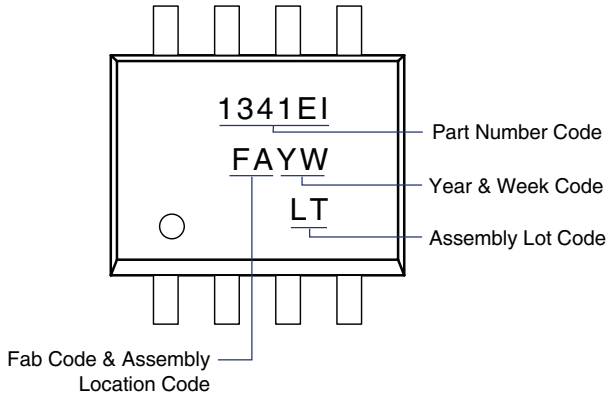
AOZ1341AI
(SO-8)



AOZ1341AI-1
(SO-8)



AOZ1341EI
(Exposed Pad MSOP-8)



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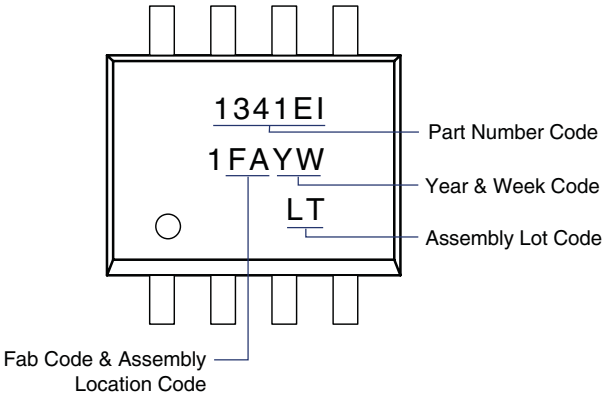

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