

## General Description

The AOZ1081 is a high efficiency, simple to use, 1.8A buck regulator for White LED. The AOZ1081 works from a 4.5V to 16V input voltage range, and provides up to 1.8A of continuous output current with an output voltage adjustable down to 0.25V.

The AOZ1081 comes in an SO-8 package and is rated over a -40°C to +85°C ambient temperature range.

## Features

- 4.5V to 16V operating input voltage range
- 100 mΩ internal PFET switch for high efficiency: up to 95%
- Internal Schottky Diode
- Internal soft start
- 0.25V internal reference with ±5% accuracy over temperature
- 1.8A continuous output current
- Fixed 1MHz PWM operation
- Cycle-by-cycle current limit
- Short-circuit protection
- Under voltage lockout
- Output over voltage protection
- Thermal shutdown
- Small size SO-8 package

## Applications

- Buck regulator for white LEDs
- Landscape lighting
- Flashlights
- Battery powered backlight applications



## Typical Application

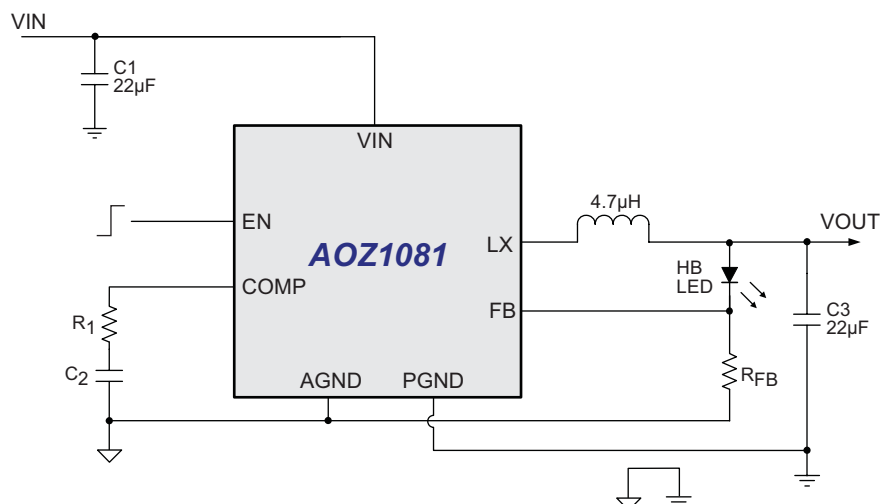


Figure 1.

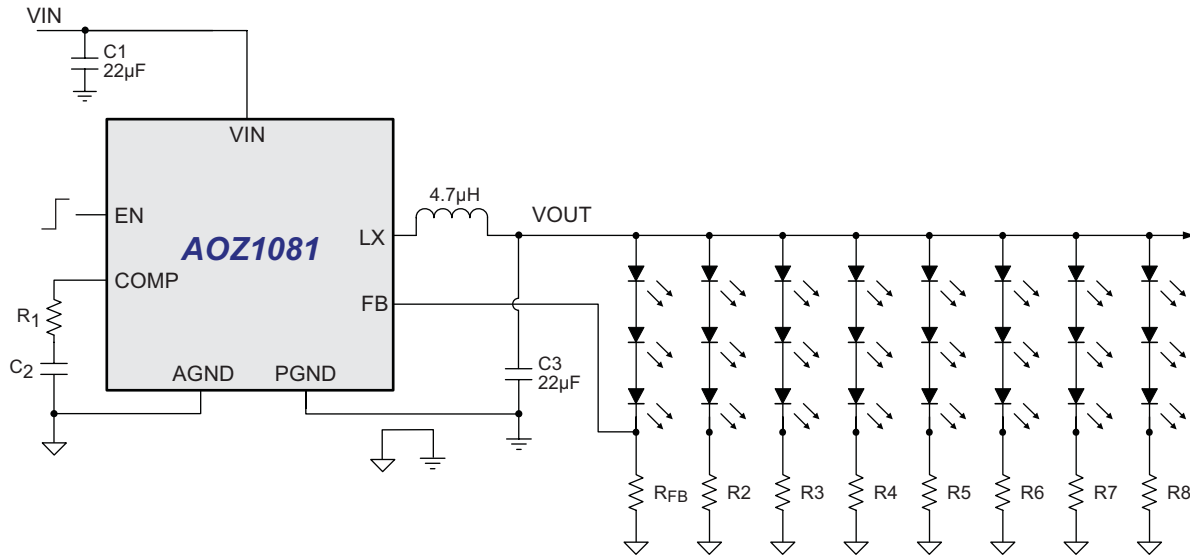


Figure 2.

### Ordering Information

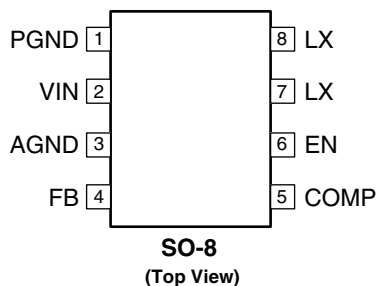
| Part Number | Ambient Temperature Range | Package | Environmental |
|-------------|---------------------------|---------|---------------|
| AOZ1081AI   | -40°C to +85°C            | SO-8    | RoHS          |



All AOS products are offered in packages with Pb-free plating and compliant to RoHS standards.

Please visit [www.aosmd.com/web/quality/rohs\\_compliant.jsp](http://www.aosmd.com/web/quality/rohs_compliant.jsp) for additional information.

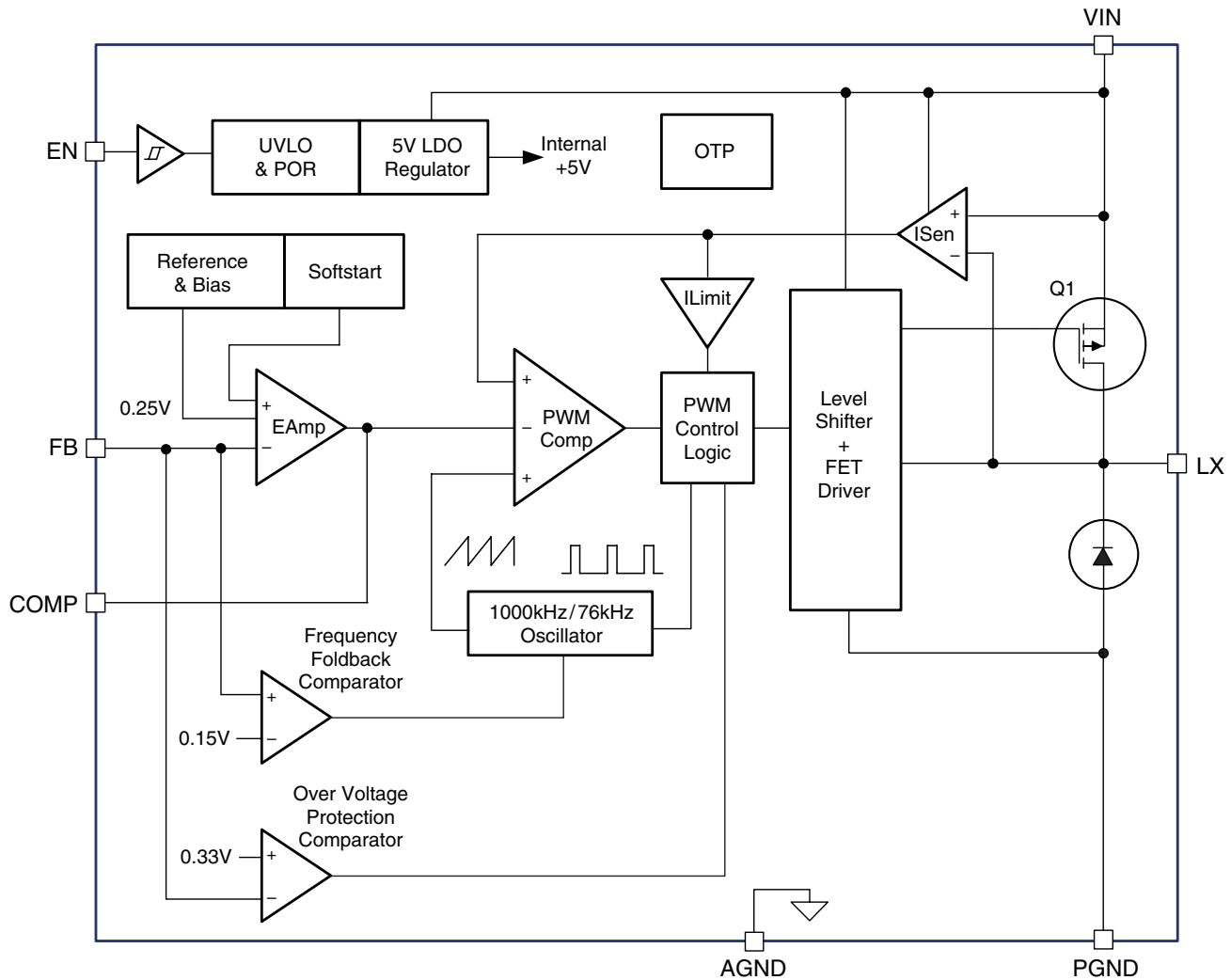
## Pin Configuration



## Pin Description

| Pin Number | Pin Name | Pin Function   |
|------------|----------|--|
| 1          | PGND     | Power ground. Electrically needs to be connected to AGND.  |
| 2          | VIN      | Supply voltage input. When $V_{IN}$ rises above the UVLO threshold the device starts up.   |
| 3          | AGND     | Reference connection for controller section. Also used as thermal connection for controller section. Electrically needs to be connected to PGND. |
| 4          | FB       | LED Current Feedback Input. The FB voltage is regulated at 250mV in normal operation. The FB sense resistor sets the nominal LED current         |
| 5          | COMP     | External loop compensation pin.  |
| 6          | EN       | The enable pin is active high. Connect EN pin to $V_{IN}$ if not used. Do not leave the EN pin floating.   |
| 7,8        | LX       | PWM output connection to inductor. Thermal connection for output stage.  |

## Block Diagram



### Absolute Maximum Ratings

Exceeding the Absolute Maximum Ratings may damage the device.

| Parameter                      | Rating                 |
|--------------------------------|------------------------|
| Supply Voltage ( $V_{IN}$ )    | 18V                    |
| LX to AGND                     | -0.7V to $V_{IN}+0.3V$ |
| EN to AGND                     | -0.3V to $V_{IN}+0.3V$ |
| FB to AGND                     | -0.3V to 6V            |
| COMP to AGND                   | -0.3V to 6V            |
| PGND to AGND                   | -0.3V to +0.3V         |
| Junction Temperature ( $T_J$ ) | +150°C                 |
| Storage Temperature ( $T_S$ )  | -65°C to +150°C        |
| ESD Rating <sup>(1)</sup>      | 2kV                    |

**Note:**

1. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5kΩ in series with 100pF.

### Recommend Operating Ratings

The device is not guaranteed to operate beyond the Maximum Operating Ratings.

| Parameter  | Rating            |
|--|-------------------|
| Supply Voltage ( $V_{IN}$ )                                      | 4.5V to 16V       |
| Output Voltage Range   | 0.25V to $V_{IN}$ |
| Ambient Temperature ( $T_A$ )                                    | -40°C to +85°C    |
| Package Thermal Resistance SO-8 ( $\Theta_{JA}$ ) <sup>(2)</sup> | 87°C/W            |

**Note:**

2. The value of  $\Theta_{JA}$  is measured with the device mounted on 1-in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A = 25^\circ\text{C}$ . The value in any given application depends on the user's specific board design.

## Electrical Characteristics

$T_A = 25^\circ\text{C}$ ,  $V_{IN} = V_{EN} = 12\text{V}$ ,  $V_{OUT} = 3.3\text{V}$  unless otherwise specified<sup>(3)</sup>

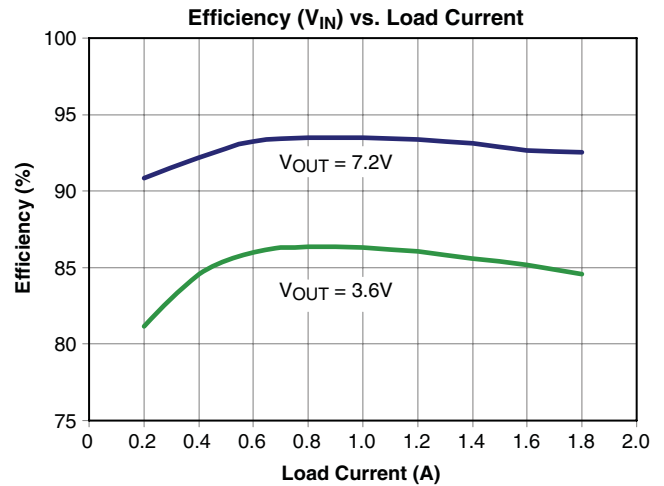
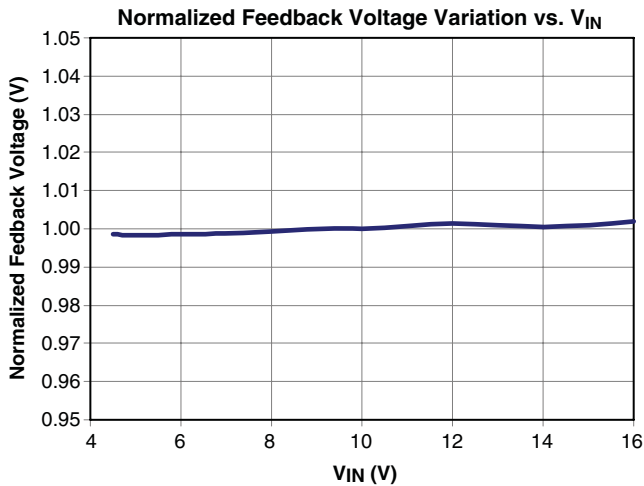
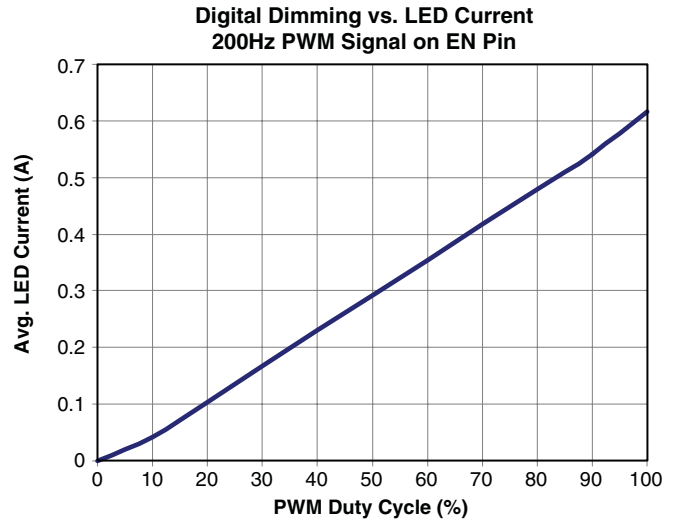
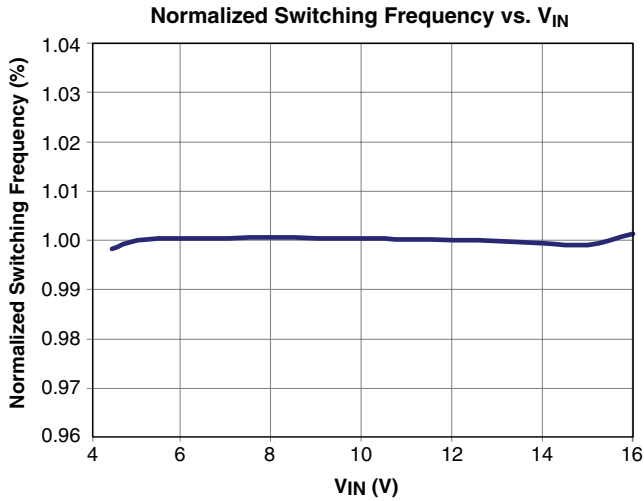
| Symbol              | Parameter                                | Conditions  | Min.          | Typ.                     | Max.          | Units            |
|---------------------|--|---|---------------|--------------------------|---------------|------------------|
| $V_{IN}$            | Supply Voltage                           |   | <b>4.5</b>    |                          | <b>16</b>     | V                |
| $V_{UVLO}$          | Input Under-Voltage Lockout Threshold    | $V_{IN}$ Rising<br>$V_{IN}$ Falling                               |               | <b>4.0</b><br><b>3.7</b> |               | V                |
| $I_{IN}$            | Supply Current (Quiescent)               | $I_{OUT} = 0$ , $V_{COMP} = 0.1\text{V}$ , $V_{EN} > 1.2\text{V}$ |               | 2                        | <b>3</b>      | mA               |
| $I_{OFF}$           | Shutdown Supply Current                  | $V_{EN} = 0\text{V}$  |               | 1                        | <b>10</b>     | $\mu\text{A}$    |
| $V_{FB}$            | Feedback Voltage                         |   | <b>0.2375</b> | 0.25                     | <b>0.2625</b> | V                |
|                     | Load Regulation                          |   |               | 0.5                      |               | %                |
|                     | Line Regulation                          |   |               | 0.5                      |               | %                |
| $I_{FB}$            | Feedback Voltage Input Current           |   |               |                          | 200           | nA               |
| $V_{EN}$            | EN Input Threshold                       | Off Threshold<br>On Threshold                                     | <b>2.0</b>    |                          | <b>0.6</b>    | V                |
| $V_{HYS}$           | EN Input Hysteresis                      |   |               | 100                      |               | mV               |
| <b>MODULATOR</b>    |  |   |               |                          |               |                  |
| $f_O$               | Frequency                                |   | <b>850</b>    | 1000                     | <b>1150</b>   | kHz              |
| $D_{MAX}$           | Maximum Duty Cycle                       |   | 100           |                          |               | %                |
| $D_{MIN}$           | Minimum Duty Cycle                       |   |               |                          | 12            | %                |
|                     | Error Amplifier Voltage Gain             |   |               | 500                      |               | V/V              |
|                     | Error Amplifier Transconductance         |   |               | 200                      |               | $\mu\text{A/V}$  |
| <b>PROTECTION</b>   |  |   |               |                          |               |                  |
| $I_{LIM}$           | Current Limit                            |   | 2.5           |                          | 4.0           | A                |
| $V_{PR}$            | Output Over-Voltage Protection Threshold | Off Threshold<br>On Threshold                                     |               | 330<br>240               |               | mV               |
| $T_J$               | Over-Temperature Shutdown Limit          |   |               | 150                      |               | $^\circ\text{C}$ |
| $t_{SS}$            | Soft Start Interval                      |   |               | 400                      |               | $\mu\text{s}$    |
| <b>OUTPUT STAGE</b> |  |   |               |                          |               |                  |
|                     | High-Side Switch On-Resistance           | $V_{IN} = 12\text{V}$<br>$V_{IN} = 5\text{V}$                     |               | 97<br>166                | 130<br>200    | $\text{m}\Omega$ |

**Note:**

3. Specification in **BOLD** indicate an ambient temperature range of  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ . These specifications are guaranteed by design.

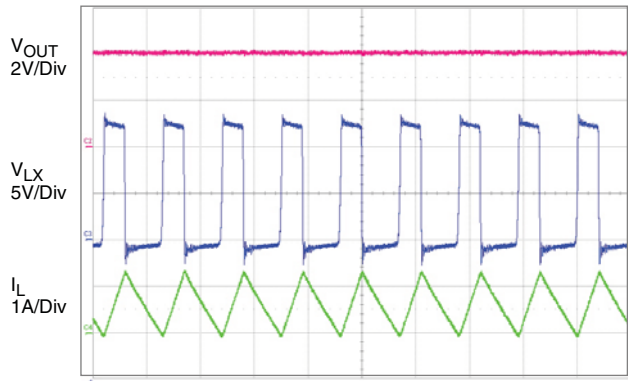
## Typical Performance Characteristics

Circuit of Figure 1.  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = V_{EN} = 12\text{V}$ ,  $V_{OUT} = 3.3\text{V}$  unless otherwise specified.

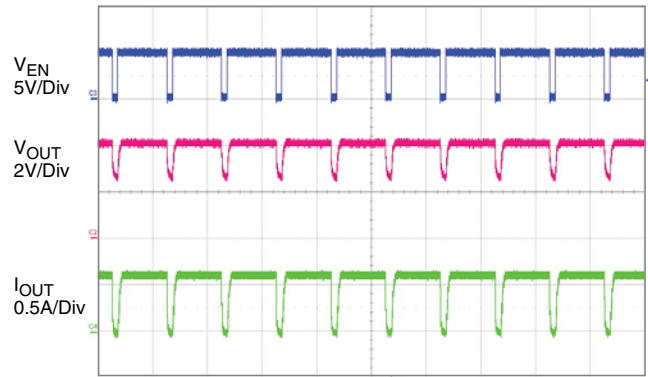


Typical Performance Characteristics (Continued)

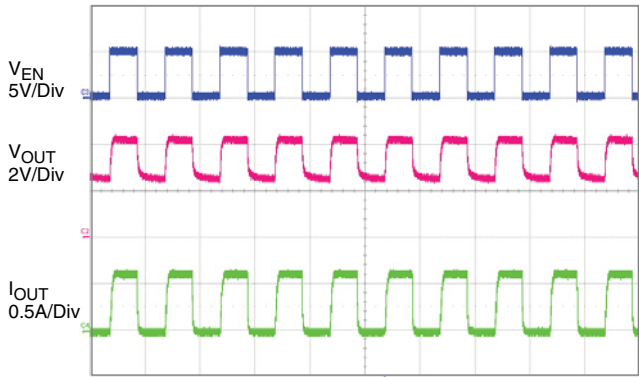
Typical Switching Waveform



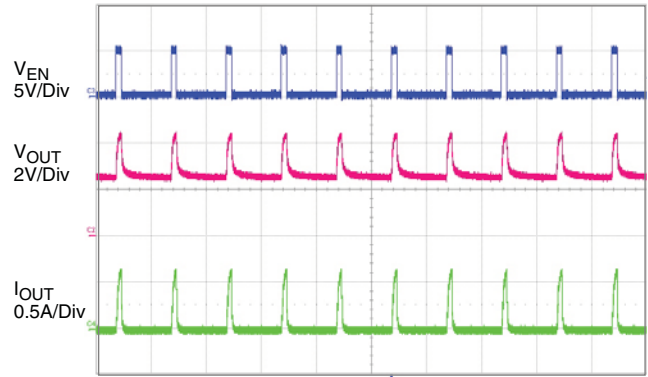
PWM Dimming at 200Hz (90% Duty Cycle)



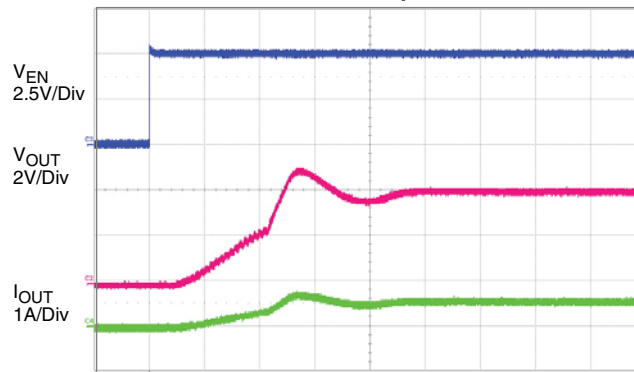
PWM Dimming at 200Hz (90% Duty Cycle)



PWM Dimming at 200Hz (90% Duty Cycle)



Start Up



## Detailed Description

The AOZ1081 is a current-mode step down regulator with integrated high side PMOS switch and a low side freewheeling Schottky diode. It operates from a 4.5V to 16V input voltage range and supplies up to 1.8A of load current. The duty cycle can be adjusted from 12% to 100% allowing a wide range of output voltage. Features include enable control, Power-On Reset, input under voltage lockout, fixed internal soft-start and thermal shut down.

The AOZ1081 is available in SO-8 package.

### Enable and Soft Start

The AOZ1081 has internal soft start feature to limit in-rush current and ensure the output voltage ramps up smoothly to regulation voltage. A soft start process begins when the input voltage rises to 4.5V and voltage on EN pin is HIGH. In soft start process, the output voltage is ramped to regulation voltage in typically 400 $\mu$ s. The 400 $\mu$ s soft start time is set internally.

The EN pin of the AOZ1081 is active HIGH. Connect the EN pin to  $V_{IN}$  if enable function is not used. Pull it to ground will disable the AOZ1081. Do not leave it open. The voltage on EN pin must be above 2.0 V to enable the AOZ1081. When voltage on EN pin falls below 0.6V, the AOZ1081 is disabled. If an application circuit requires the AOZ1081 to be disabled, an open drain or open collector circuit should be used to interface to EN pin.

### PWM Dimming

The AOZ1081 allows dimming up to 200Hz PWM signal at the EN pin. By forcing a PWM digital waveform to the EN pin, the system will go into a digital dimming state. The output switch will be off when PWM waveform is logic low and it will be on when PWM waveform is logic high. The duty cycle range is 10% to 100%.

### Steady-State Operation

Under steady-state conditions, the converter operates in fixed frequency and Continuous-Conduction Mode (CCM).

The AOZ1081 integrates an internal P-MOSFET as the high-side switch. Inductor current is sensed by amplifying the voltage drop across the drain to source of the high side power MOSFET. Output voltage is divided down by the external voltage divider at the FB pin. The difference of the FB pin voltage and reference is amplified by the internal transconductance error amplifier. The error voltage, which shows on the COMP pin, is compared against

the current signal, which is sum of inductor current signal and ramp compensation signal, at PWM comparator input. If the current signal is less than the error voltage, the internal high-side switch is on. The inductor current flows from the input through the inductor to the output. When the current signal exceeds the error voltage, the high-side switch is off. The inductor current is freewheeling through the internal Schottky diode to output.

The AOZ1081 uses a P-Channel MOSFET as the high side switch. It saves the bootstrap capacitor normally seen in a circuit which is using an NMOS switch. It allows 100% turn-on of the upper switch to achieve linear regulation mode of operation. The minimum voltage drop from  $V_{IN}$  to  $V_O$  is the load current times DC resistance of MOSFET + DC resistance of buck inductor. It can be calculated by equation below:

$$V_{O\_MAX} = V_{IN} - I_O \times (R_{DS(ON)} + R_{inductor})$$

where,

$V_{O\_MAX}$  is the maximum output voltage;

$V_{IN}$  is the input voltage from 4.5V to 16V;

$I_O$  is the output current from 0A to 1.8A;

$R_{DS(ON)}$  is the on resistance of internal MOSFET, the value is between 97m $\Omega$  and 200m $\Omega$  depending on input voltage and junction temperature; and

$R_{inductor}$  is the inductor DC resistance;

### Switching Frequency

The AOZ1081 switching frequency is fixed and set by an internal oscillator. The actual switching frequency could range from 850kHz to 1.15MHz due to device variation.

### Protection Features

The AOZ1081 has multiple protection features to prevent system circuit damage under abnormal conditions.

#### Over Current Protection (OCP)

The sensed inductor current signal is also used for over current protection. Since the AOZ1081 employs peak current mode control, the COMP pin voltage is proportional to the peak inductor current. The COMP pin voltage is limited to be between 0.4V and 2.5V internally. The peak inductor current is automatically limited cycle by cycle.

The cycle by cycle current limit threshold is set between 2.5A and 4A. When the load current reaches the current limit threshold, the cycle by cycle current limit circuit turns



off the high side switch immediately to terminate the current duty cycle. The inductor current stop rising. The cycle by cycle current limit protection directly limits inductor peak current. The average inductor current is also limited due to the limitation on peak inductor current. When cycle by cycle current limit circuit is triggered, the output voltage drops as the duty cycle decreasing.

The AOZ1081 has internal short circuit protection to protect itself from catastrophic failure under output short circuit conditions. The FB pin voltage is proportional to the output voltage. Whenever FB pin voltage is below 0.15V, the short circuit protection circuit is triggered. As a result, the converter is shut down and hiccups at a frequency equals to 1/8 of normal switching frequency. The converter will start up via a soft start once the short circuit condition disappears. In short circuit protection mode, the inductor average current is greatly reduced because of the low hiccup frequency.

### Output Over Voltage Protection (OVP)

The AOZ1081 monitors the feedback voltage: when the feedback voltage is higher than 330mV, it immediate turns-off the PMOS to protect the output voltage overshoot at fault condition. When feedback voltage is lower than 240mV, the PMOS is allowed to turn on in the next cycle.

### Power-On Reset (POR)

A power-on reset circuit monitors the input voltage. When the input voltage exceeds 4V, the converter starts operation. When input voltage falls below 3.7V, the converter will stop switching.

### Thermal Protection

An internal temperature sensor monitors the junction temperature. It shuts down the internal control circuit and high side PMOS if the junction temperature exceeds 150°C.

## Application Information

The basic AOZ1081 application circuit is shown in Figure 1 and 2. Component selection is explained below.

### Setting the Maximum LED Current

The AOZ1081 features a programmable LED current using a resistor  $R_{FB}$  at the end of the primary chain of LEDs.

$$I_{LEDMAX} = \frac{250mV}{R_{FB}}$$

## Input Capacitor

The input capacitor (C1 in Figure 1) must be connected to the  $V_{IN}$  pin and PGND pin of the AOZ1081 to maintain steady input voltage and filter out the pulsing input current. A small decoupling capacitor ( $C_d$  in Figure 1), usually 1 $\mu$ F, should be connected to the  $V_{IN}$  pin and AGND pin for stable operation of the AOZ1081. The voltage rating of input capacitor must be greater than maximum input voltage plus ripple voltage.

The input ripple voltage can be approximated by equation below:

$$\Delta V_{IN} = \frac{I_O}{f \times C_{IN}} \times \left(1 - \frac{V_O}{V_{IN}}\right) \times \frac{V_O}{V_{IN}}$$

Since the input current is discontinuous in a buck converter, the current stress on the input capacitor is another concern when selecting the capacitor. For a buck circuit, the RMS value of input capacitor current can be calculated by:

$$I_{CIN\_RMS} = I_O \times \sqrt{\frac{V_O}{V_{IN}} \left(1 - \frac{V_O}{V_{IN}}\right)}$$

if let  $m$  equal the conversion ratio:

$$\frac{V_O}{V_{IN}} = m$$

The relationship between the input capacitor RMS current and voltage conversion ratio is calculated and shown in Figure 2. It can be seen that when  $V_O$  is half of  $V_{IN}$ ,  $C_{IN}$  is under the worst current stress. The worst current stress on  $C_{IN}$  is  $0.5 \times I_O$ .

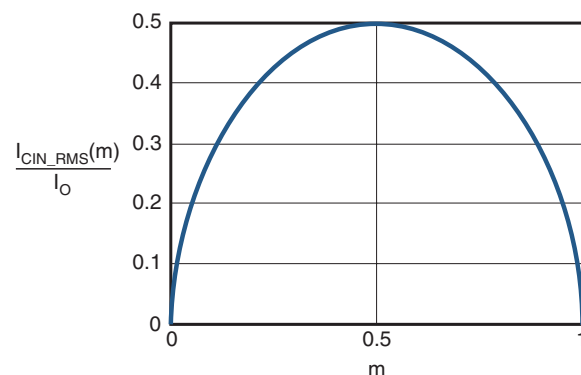


Figure 2.  $I_{CIN}$  vs. Voltage Conversion Ratio

For reliable operation and best performance, the input capacitors must have current rating higher than  $I_{CIN\_RMS}$  at worst operating conditions. Ceramic capacitors are preferred for input capacitors because of their low ESR and high ripple current rating. Depending on the application circuits, other low ESR tantalum capacitor or aluminum electrolytic capacitor may also be used. When selecting ceramic capacitors, X5R or X7R type dielectric ceramic capacitors are preferred for their better temperature and voltage characteristics. Note that the ripple current rating from capacitor manufactures is based on certain amount of life time. Further de-rating may be necessary for practical design requirement.

### Inductor

The inductor is used to supply constant current to output when it is driven by a switching voltage. For given input and output voltage, inductance and switching frequency together decide the inductor ripple current, which is:

$$\Delta I_L = \frac{V_O}{f \times L} \times \left(1 - \frac{V_O}{V_{IN}}\right)$$

The peak inductor current is:

$$I_{Lpeak} = I_O + \frac{\Delta I_L}{2}$$

High inductance gives low inductor ripple current but requires larger size inductor to avoid saturation. Low ripple current reduces inductor core losses. It also reduces RMS current through inductor and switches, which results in less conduction loss. Usually, peak to peak ripple current on inductor is designed to be 20% to 30% of output current.

When selecting the inductor, make sure it is able to handle the peak current without saturation even at the highest operating temperature.

The inductor takes the highest current in a buck circuit. The conduction loss on inductor needs to be checked for thermal and efficiency requirements.

Surface mount inductors in different shape and styles are available from Coilcraft, Elytone and Murata. Shielded inductors are small and radiate less EMI noise. But they cost more than unshielded inductors. The choice depends on EMI requirement, price and size.

### Output Capacitor

The output capacitor is selected based on the DC output voltage rating, output ripple voltage specification and ripple current rating.

The selected output capacitor must have a higher rated voltage specification than the maximum desired output voltage including ripple. De-rating needs to be considered for long term reliability.

Output ripple voltage specification is another important factor for selecting the output capacitor. In a buck converter circuit, output ripple voltage is determined by inductor value, switching frequency, output capacitor value and ESR. It can be calculated by the equation below:

$$\Delta V_O = \Delta I_L \times \left(ESR_{CO} + \frac{1}{8 \times f \times C_O}\right)$$

where;

$C_O$  is output capacitor value, and

$ESR_{CO}$  is the Equivalent Series Resistor of output capacitor.

When low ESR ceramic capacitor is used as output capacitor, the impedance of the capacitor at the switching frequency dominates. Output ripple is mainly caused by capacitor value and inductor ripple current. The output ripple voltage calculation can be simplified to:

$$\Delta V_O = \Delta I_L \times \frac{1}{8 \times f \times C_O}$$

If the impedance of ESR at switching frequency dominates, the output ripple voltage is mainly decided by capacitor ESR and inductor ripple current. The output ripple voltage calculation can be further simplified to:

$$\Delta V_O = \Delta I_L \times ESR_{CO}$$

For lower output ripple voltage across the entire operating temperature range, X5R or X7R dielectric type of ceramic, or other low ESR tantalum are recommended to be used as output capacitors.

In a buck converter, output capacitor current is continuous. The RMS current of output capacitor is decided by the peak to peak inductor ripple current. It can be calculated by:

$$I_{CO\_RMS} = \frac{\Delta I_L}{\sqrt{12}}$$

Usually, the ripple current rating of the output capacitor is a smaller issue because of the low current stress. When the buck inductor is selected to be very small and inductor ripple current is high, output capacitor could be overstressed.

## Loop Compensation

The AOZ1081 employs peak current mode control for easy use and fast transient response. Peak current mode control eliminates the double pole effect of the output L&C filter. It greatly simplifies the compensation loop design.

With peak current mode control, the buck power stage can be simplified to be a one-pole and one-zero system in frequency domain. The pole is dominant pole and can be calculated by:

$$f_{p1} = \frac{1}{2\pi \times C_O \times R_L}$$

The zero is a ESR zero due to output capacitor and its ESR. It is can be calculated by:

$$f_{z1} = \frac{1}{2\pi \times C_O \times ESR_{CO}}$$

where;

$C_O$  is the output filter capacitor,

$R_L$  is load resistor value, and

$ESR_{CO}$  is the equivalent series resistance of output capacitor.

The compensation design is actually to shape the converter close loop transfer function to get desired gain and phase. Several different types of compensation network can be used for AOZ1081. For most cases, a series capacitor and resistor network connected to the COMP pin sets the pole-zero and is adequate for a stable high-bandwidth control loop.

In the AOZ1081, FB pin and COMP pin are the inverting input and the output of internal transconductance error amplifier. A series R and C compensation network connected to COMP provides one pole and one zero. The pole is:

$$f_{p2} = \frac{G_{EA}}{2\pi \times C_C \times G_{VEA}}$$

where;

$G_{EA}$  is the error amplifier transconductance, which is  $200 \times 10^{-6}$  A/V,

$G_{VEA}$  is the error amplifier voltage gain, which is 500 V/V, and

$C_C$  is compensation capacitor.

The zero given by the external compensation network, capacitor  $C_C$  (C5 in Figure 1) and resistor  $R_C$  (R1 in Figure 1), is located at:

$$f_{z2} = \frac{1}{2\pi \times C_C \times R_C}$$

To design the compensation circuit, a target crossover frequency  $f_C$  for close loop must be selected. The system crossover frequency is where control loop has unity gain. The crossover frequency is also called the converter bandwidth. Generally a higher bandwidth means faster response to load transient. However, the bandwidth should not be too high due to system stability concern. When designing the compensation loop, converter stability under all line and load condition must be considered.

Usually, it is recommended to set the bandwidth to be less than 1/10 of switching frequency. The AOZ1081 operates at a fixed switching frequency range from 750kHz to 1.15MHz. It is recommended to choose a crossover frequency less than 75kHz.

$$f_C = 75kHz$$

The strategy for choosing  $R_C$  and  $C_C$  is to set the cross over frequency with  $R_C$  and set the compensator zero with  $C_C$ . Using selected crossover frequency,  $f_C$ , to calculate  $R_C$ :

$$R_C = f_C \times \frac{V_O}{V_{FB}} \times \frac{2\pi \times C_O}{G_{EA} \times G_{CS}}$$

where;

$f_C$  is desired crossover frequency,

$V_{FB}$  is 0.25V,

$G_{EA}$  is the error amplifier transconductance, which is  $200 \times 10^{-6}$  A/V, and

$G_{CS}$  is the current sense circuit transconductance, which is 5.64 A/V.

The compensation capacitor  $C_C$  and resistor  $R_C$  together make a zero. This zero is put somewhere close to the dominate pole  $f_{p1}$  but lower than 1/5 of selected crossover frequency.  $C_C$  can be selected by:

$$C_C = \frac{1.5}{2\pi \times R_C \times f_{p1}}$$

The equation above can also be simplified to:

$$C_C = \frac{C_O \times R_L}{R_C}$$

## Thermal Management and Layout Consideration

In the AOZ1081 buck regulator circuit, high pulsing current flows through two circuit loops. The first loop starts from the input capacitors, to the  $V_{IN}$  pin, to the LX pins, to the filter inductor, to the output capacitor and load, and then return to the input capacitor through ground. Current flows in the first loop when the high side switch is on. The second loop starts from inductor, to the output capacitors and load, to the PGND pin of the AOZ1081, to the LX pins of the AOZ1081. Current flows in the second loop when the low side diode is on.

In PCB layout, minimizing the two loops area reduces the noise of this circuit and improves efficiency. A ground plane is recommended to connect input capacitor, output capacitor, and PGND pin of the AOZ1081.

In the AOZ1081 buck regulator circuit, the two major power dissipating components are the AOZ1081 and output inductor. The total power dissipation of converter circuit can be measured by input power minus output power.

$$P_{total\_loss} = V_{IN} \times I_{IN} - V_O \times I_O$$

The power dissipation of inductor can be approximately calculated by output current and DCR of inductor.

$$P_{inductor\_loss} = I_O^2 \times R_{inductor} \times 1.1$$

The actual AOZ1081 junction temperature can be calculated with power dissipation in the AOZ1081 and thermal impedance from junction to ambient.

$$T_{junction} = (P_{total\_loss} - P_{inductor\_loss}) \times \Theta + T_{ambient}$$

The maximum junction temperature of AOZ1081 is 150°C, which limits the maximum load current capability. Please see the thermal de-rating curves for the maximum load current of the AOZ1081 under different ambient temperature.

The thermal performance of the AOZ1081 is strongly affected by the PCB layout. Extra care should be taken by users during design process to ensure that the IC will operate under the recommended environmental conditions.

Several layout tips are listed below for the best electric and thermal performance. Figure 3 on the next page illustrates a single layer PCB layout example as reference.

1. Do not use thermal relief connection to the  $V_{IN}$  and the PGND pin. Pour a maximized copper area to the PGND pin and the  $V_{IN}$  pin to help thermal dissipation.
2. Input capacitor should be connected to the  $V_{IN}$  pin and the PGND pin as close as possible.
3. A ground plane is preferred. If a ground plane is not used, separate PGND from AGND and connect them only at one point to avoid the PGND pin noise coupling to the AGND pin. In this case, a decoupling capacitor should be connected between  $V_{IN}$  pin and AGND pin.
4. Make the current trace from LX pins to L to Co to the PGND as short as possible.
5. Pour copper plane on all unused board area and connect it to stable DC nodes, like  $V_{IN}$ , GND or  $V_{OUT}$ .
6. The two LX pins are connected to internal PFET drain. They are low resistance thermal conduction path and most noisy switching node. Connected a copper plane to LX pin to help thermal dissipation. This copper plane should not be too larger otherwise switching noise may be coupled to other part of circuit.
7. Keep sensitive signal trace such as trace connected with FB pin and COMP pin far away from the LX pins.

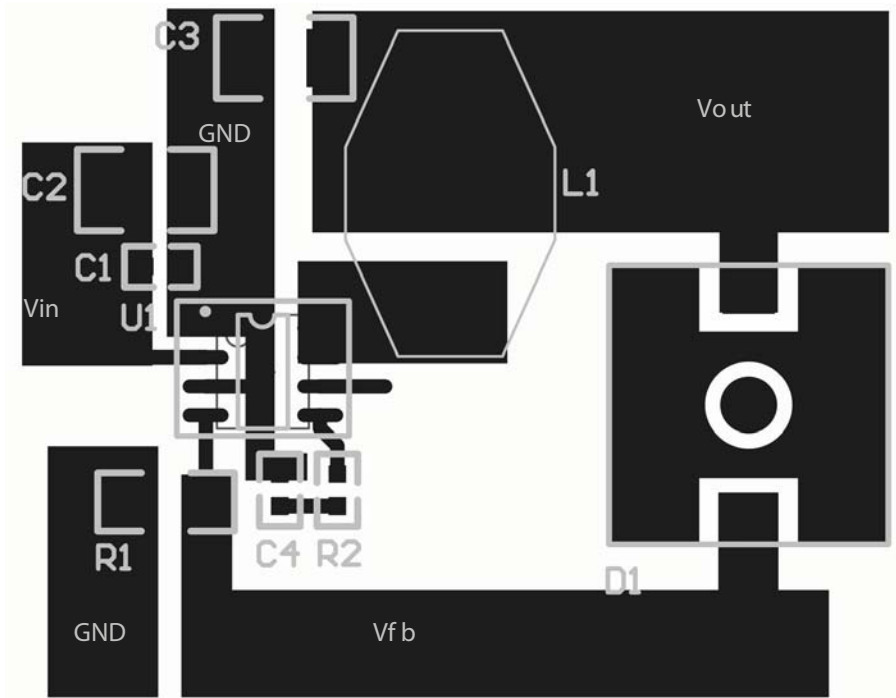
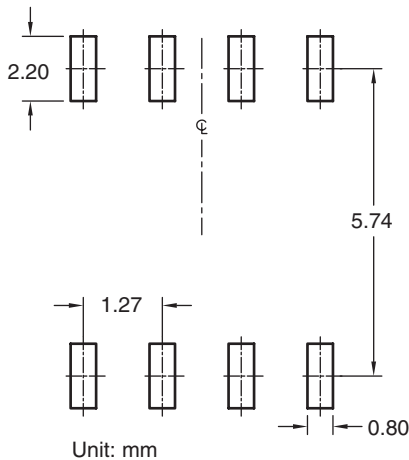
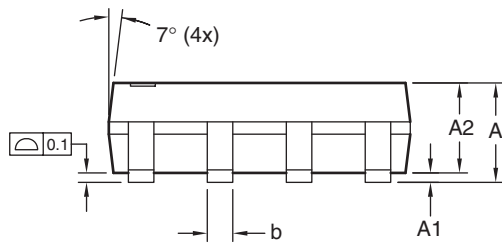
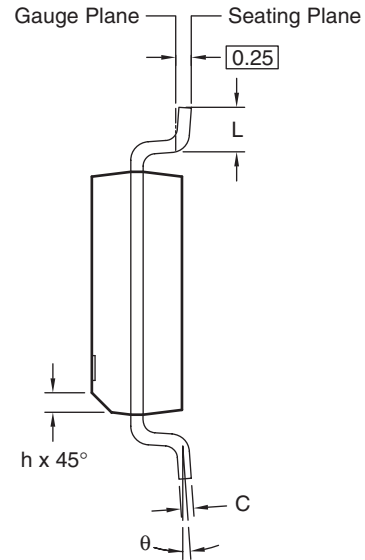
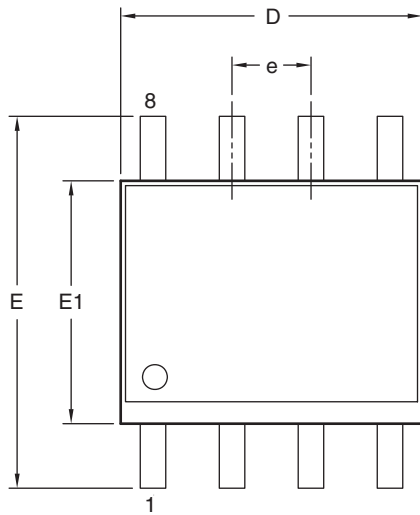


Figure 3. AOZ1081 PCB Layout

### Package Dimensions, SO-8



Dimensions in millimeters

| Symbols | Min.     | Nom. | Max. |
|---------|----------|------|------|
| A       | 1.35     | 1.65 | 1.75 |
| A1      | 0.10     | —    | 0.25 |
| A2      | 1.25     | 1.50 | 1.65 |
| b       | 0.31     | —    | 0.51 |
| c       | 0.17     | —    | 0.25 |
| D       | 4.80     | 4.90 | 5.00 |
| E1      | 3.80     | 3.90 | 4.00 |
| e       | 1.27 BSC |      |      |
| E       | 5.80     | 6.00 | 6.20 |
| h       | 0.25     | —    | 0.50 |
| L       | 0.40     | —    | 1.27 |
| θ       | 0°       | —    | 8°   |

Dimensions in inches

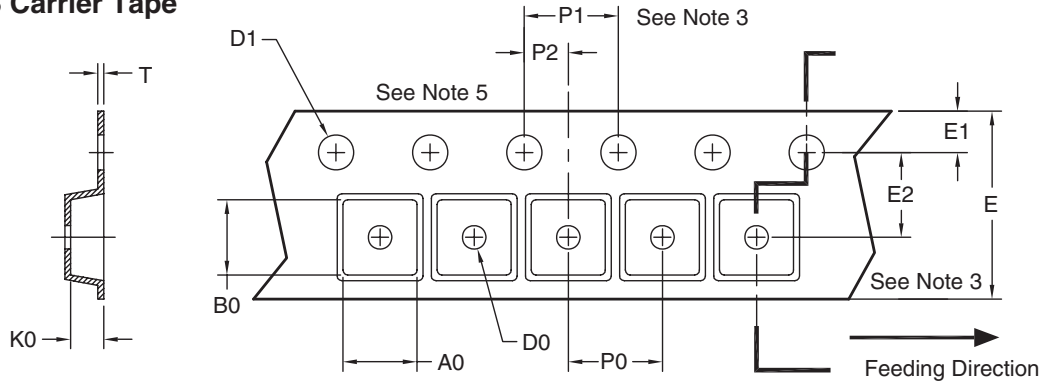
| Symbols | Min.      | Nom.  | Max.  |
|---------|-----------|-------|-------|
| A       | 0.053     | 0.065 | 0.069 |
| A1      | 0.004     | —     | 0.010 |
| A2      | 0.049     | 0.059 | 0.065 |
| b       | 0.012     | —     | 0.020 |
| c       | 0.007     | —     | 0.010 |
| D       | 0.189     | 0.193 | 0.197 |
| E1      | 0.150     | 0.154 | 0.157 |
| e       | 0.050 BSC |       |       |
| E       | 0.228     | 0.236 | 0.244 |
| h       | 0.010     | —     | 0.020 |
| L       | 0.016     | —     | 0.050 |
| θ       | 0°        | —     | 8°    |

**Notes:**

1. All dimensions are in millimeters.
2. Dimensions are inclusive of plating
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 6 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

## Tape and Reel Dimensions, SO-8

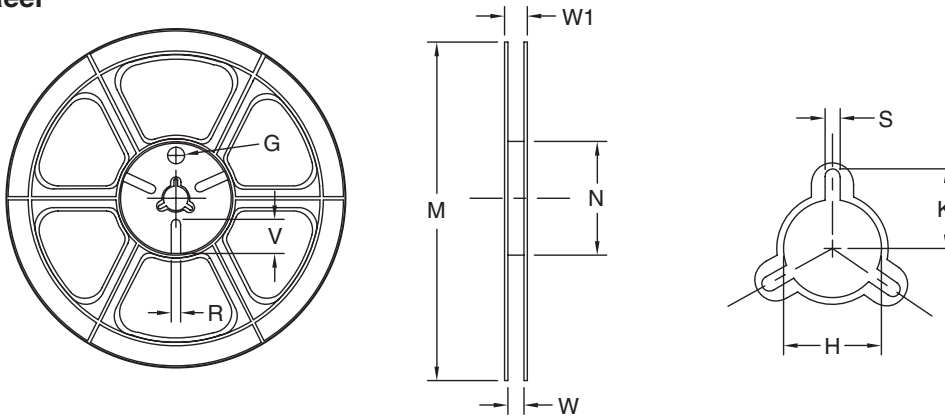
### SO-8 Carrier Tape



Unit: mm

| Package        | A0            | B0            | K0            | D0            | D1            | E              | E1            | E2            | P0            | P1            | P2            | T             |
|----------------|---------------|---------------|---------------|---------------|---------------|----------------|---------------|---------------|---------------|---------------|---------------|---------------|
| SO-8<br>(12mm) | 6.40<br>±0.10 | 5.20<br>±0.10 | 2.10<br>±0.10 | 1.60<br>±0.10 | 1.50<br>±0.10 | 12.00<br>±0.10 | 1.75<br>±0.10 | 5.50<br>±0.10 | 8.00<br>±0.10 | 4.00<br>±0.10 | 2.00<br>±0.10 | 0.25<br>±0.10 |

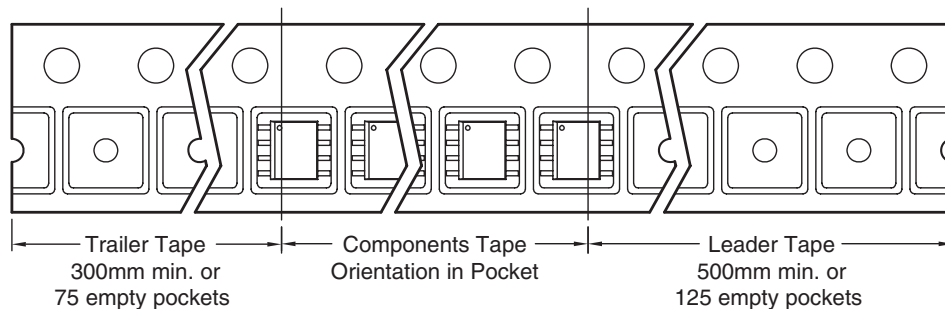
### SO-8 Reel



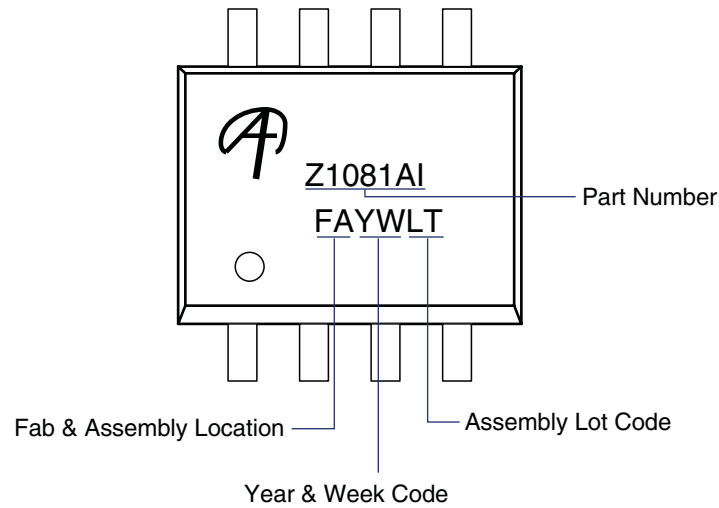
| Tape Size | Reel Size | M                | N               | W              | W1             | H                     | K     | S             | G | R | V |
|-----------|-----------|------------------|-----------------|----------------|----------------|-----------------------|-------|---------------|---|---|---|
| 12mm      | ø330      | ø330.00<br>±0.50 | ø97.00<br>±0.10 | 13.00<br>±0.30 | 17.40<br>±1.00 | ø13.00<br>+0.50/-0.20 | 10.60 | 2.00<br>±0.50 | — | — | — |

### SO-8 Tape

Leader/Trailer & Orientation



## Package Marking



### LIFE SUPPORT POLICY

ALPHA & OMEGA SEMICONDUCTOR PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.