ALPHA & OMEGA SEMICONDUCTOR

AON6984

30V Dual Asymmetric N-Channel MOSFET

General Description

- Trench Power αMOS Technology
- Low $R_{DS(ON)}$
- Low Gate Charge
- High Current Capability
- RoHS and Halogen-Free Compliant

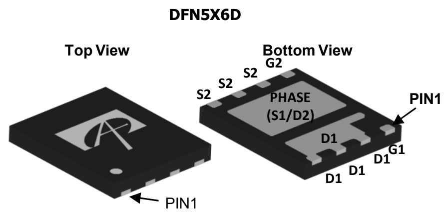
Applications

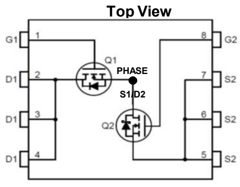
- DC/DC Converters in Computing
- Isolated DC/DC Converters in Telecom and Industrial

Product Summary

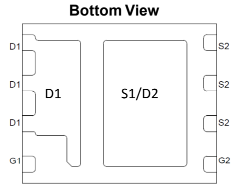
	Q1	Q2
V_{DS}	30V	30V
I_D (at V_{GS}=10V)	50A	82A
$R_{DS(ON)}$ (at V_{GS}=10V)	< 5.2mΩ	< 2.8mΩ
$R_{DS(ON)}$ (at V_{GS}=4.5V)	< 8.4mΩ	< 3.45mΩ

100% UIS Tested
100% Rg Tested





Q2: SRFET™
Soft Recovery MOSFET:
Integrated Schottky Diode



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AON6984	DFN 5x6D	Tape & Reel	3000

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Max Q1	Max Q2	Units
Drain-Source Voltage		V_{DS}	30	30	V
Gate-Source Voltage		V_{GS}	±20	±12	V
Continuous Drain Current	T_C=25°C	I_D	50	82	A
	T_C=100°C		31	54	
Pulsed Drain Current [C]		I_{DM}	100	180	
Continuous Drain Current	T_A=25°C	I_{DSM}	19	26	A
	T_A=70°C		15	21	
Avalanche Current [C]		I_{AS}	38	72	A
Avalanche energy	L=0.01mH [C]	E_{AS}	7	26	mJ
V_{DS} Spike	10µs	V_{SPIKE}	36	36	V
Power Dissipation [B]	T_C=25°C	P_D	21	31	W
	T_C=100°C		8	13	
Power Dissipation [A]	T_A=25°C	P_{DSM}	3.1	3.1	W
	T_A=70°C		2	2	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150		°C

Thermal Characteristics

Parameter		Symbol	Typ Q1	Typ Q2	Max Q1	Max Q2	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	30	30	40	40	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		50	50	65	65	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	4.6	3.1	6	4	°C/W

Q1 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV_{DSS}	Drain-Source Breakdown Voltage	ID=250µA, VGS=0V		30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V				1	µA
			T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V				±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=$V_{GS,}$ I_D=250µA		1.4	1.8	2.2	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=20A			4.3	5.2	mΩ
			T_J=125°C		6.3	7.6	
		V_{GS}=4.5V, I_D=20A			6.8	8.4	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=20A			67		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V			0.71	1	V
I_S	Maximum Body-Diode Continuous Current					20	A
DYNAMIC PARAMETERS							
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz			810		pF
C_{oss}	Output Capacitance				335		pF
C_{rss}	Reverse Transfer Capacitance				39		pF
R_g	Gate resistance	f=1MHz		0.6	1.2	1.8	Ω
SWITCHING PARAMETERS							
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=20A			12.8		nC
Q_g(4.5V)	Total Gate Charge				6		nC
Q_{gs}	Gate Source Charge				2		nC
Q_{gd}	Gate Drain Charge				2.3		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=0.75Ω, R_{GEN}=3Ω			6.5		ns
t_r	Turn-On Rise Time				16.5		ns
$t_{D(off)}$	Turn-Off DelayTime				17		ns
t_f	Turn-Off Fall Time				2.5		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, dI/dt=500A/µs			11		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=20A, dI/dt=500A/µs			19		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on R $_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Single pulse width limited by junction temperature $T_{J(MAX)}$=150° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. The maximum current rating is package limited.
H. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

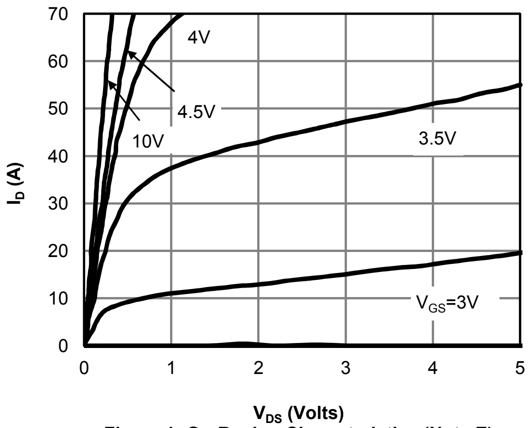


Figure 1: On-Region Characteristics (Note E)

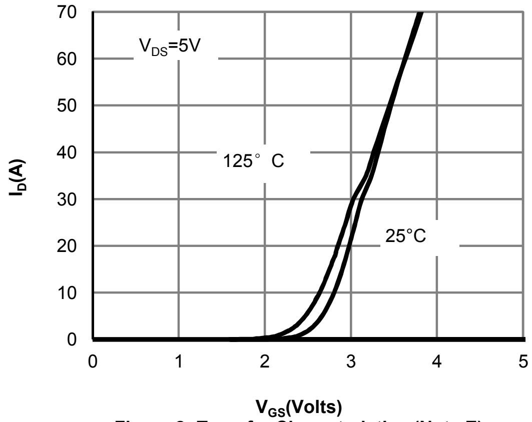


Figure 2: Transfer Characteristics (Note E)

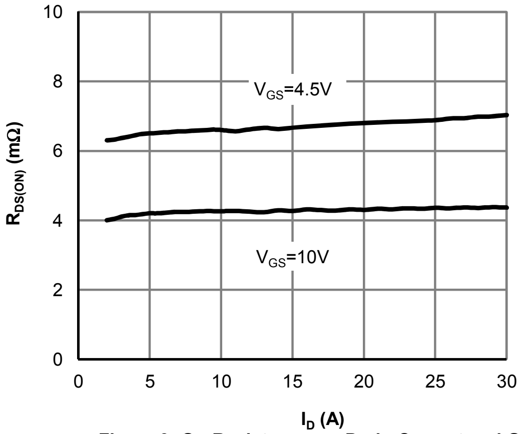


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

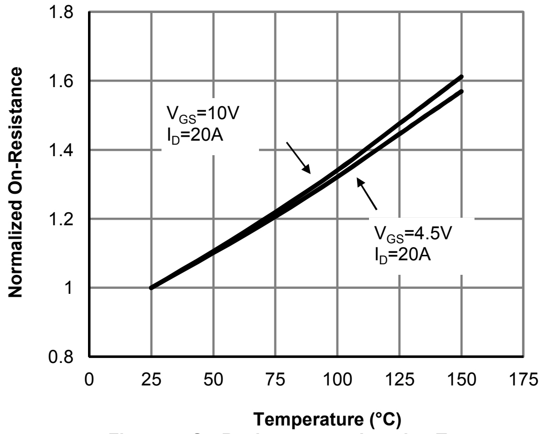


Figure 4: On-Resistance vs. Junction Temperature (Note E)

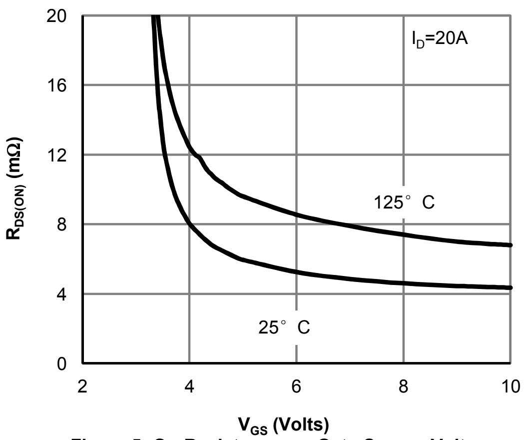


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

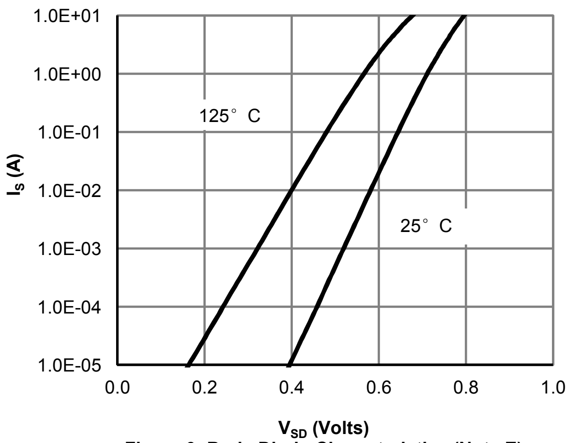


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

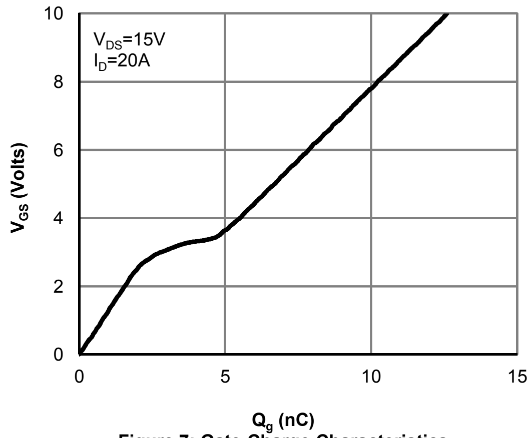


Figure 7: Gate-Charge Characteristics

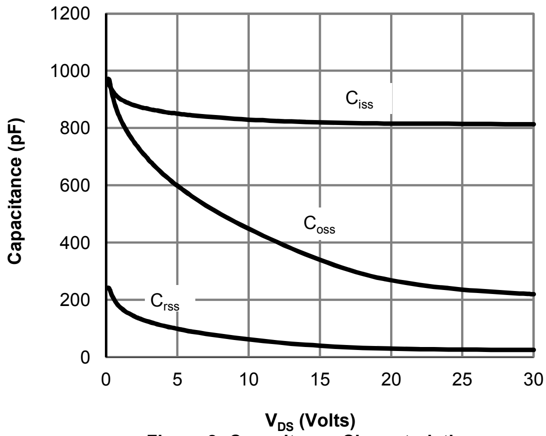
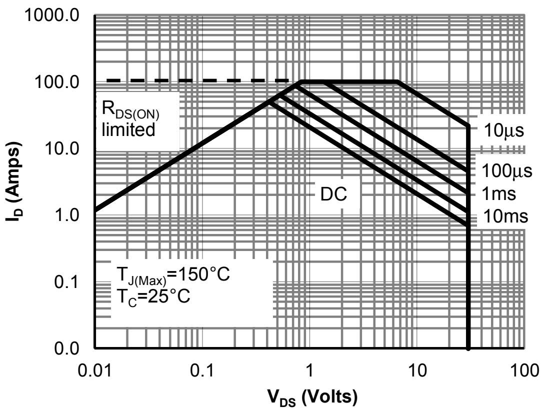


Figure 8: Capacitance Characteristics



V_{GS}> or equal to 4.5V
Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

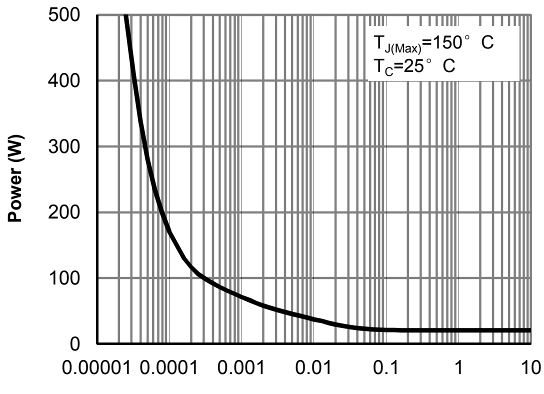


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

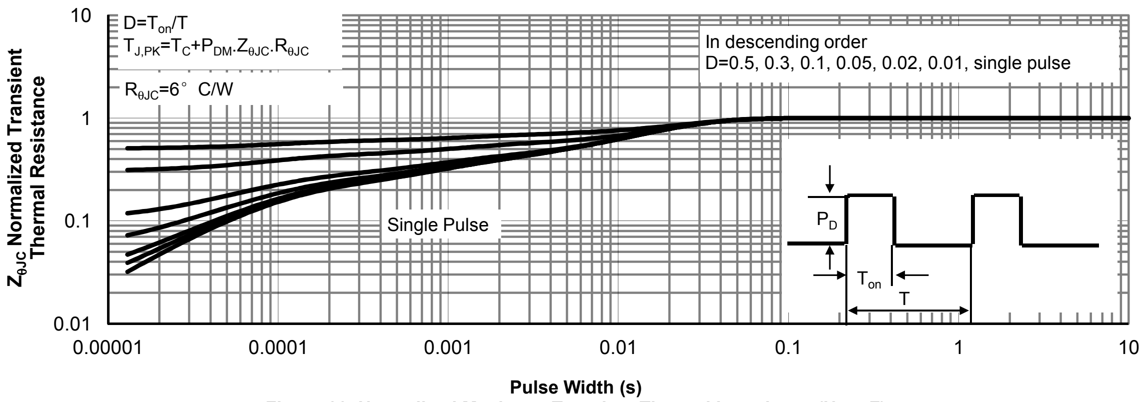


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

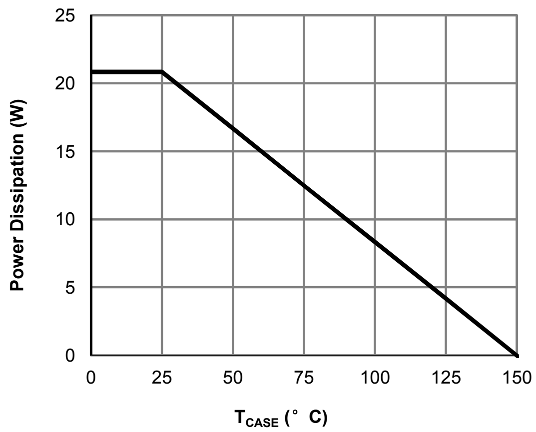


Figure 12: Power De-rating (Note F)

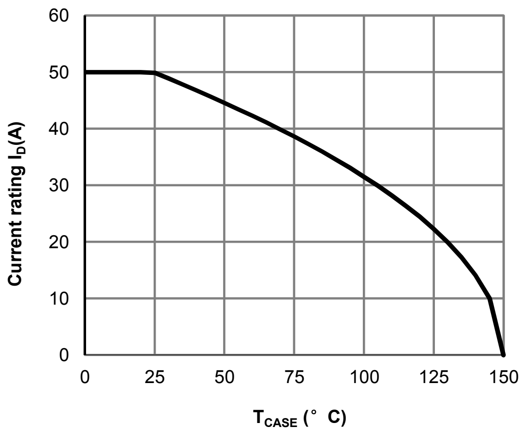


Figure 13: Current De-rating (Note F)

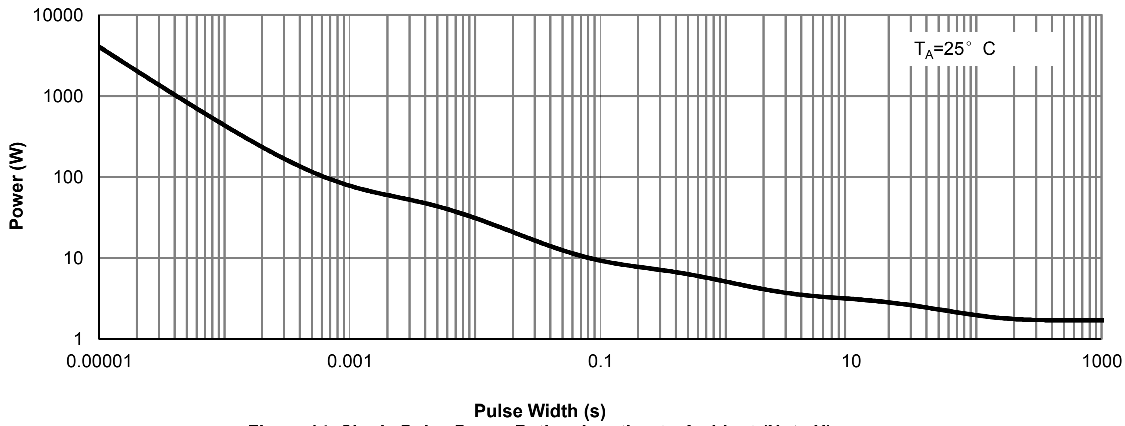


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

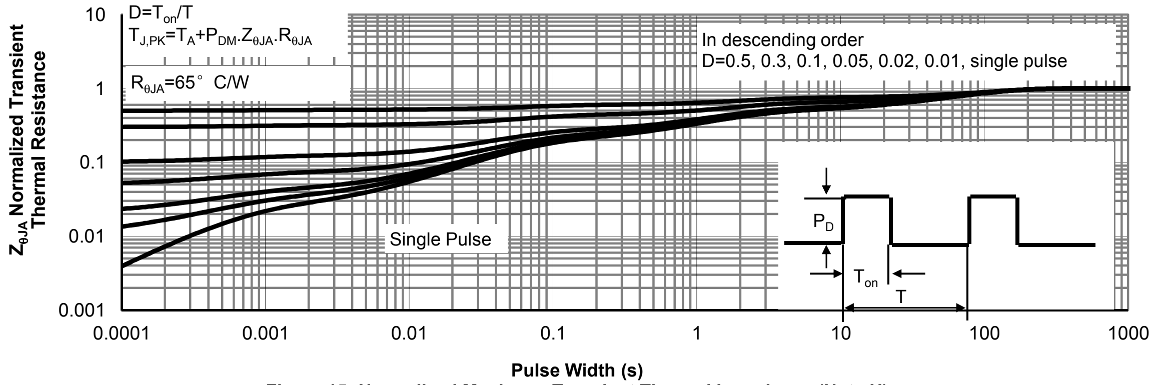


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

Q2 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	ID=10mA, VGS=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			0.5	mA
		T_J=55°C			100	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±12V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=$V_{GS,}$ I_D=250µA	1.1	1.5	1.9	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=20A		2.3	2.8	mΩ
		T_J=125°C		3.4	4.1	
		V_{GS}=4.5V, I_D=20A		2.8	3.45	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=20A		167		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.5	0.7	V
I_S	Maximum Body-Diode Continuous Current				30	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		2120		pF
C_{oss}	Output Capacitance			700		pF
C_{rss}	Reverse Transfer Capacitance			69		pF
R_g	Gate resistance	f=1MHz	0.9	1.8	2.7	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=20A		37		nC
Q_g(4.5V)	Total Gate Charge			16.8		nC
Q_{gs}	Gate Source Charge			5		nC
Q_{gd}	Gate Drain Charge			4.9		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=0.75Ω, R_{GEN}=3Ω		7		ns
t_r	Turn-On Rise Time			3.5		ns
$t_{D(off)}$	Turn-Off DelayTime			36		ns
t_f	Turn-Off Fall Time			6		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, dI/dt=500A/µs		15.5		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=20A, dI/dt=500A/µs		33		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on R $_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Single pulse width limited by junction temperature $T_{J(MAX)}$=150° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. The maximum current rating is package limited.
H. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

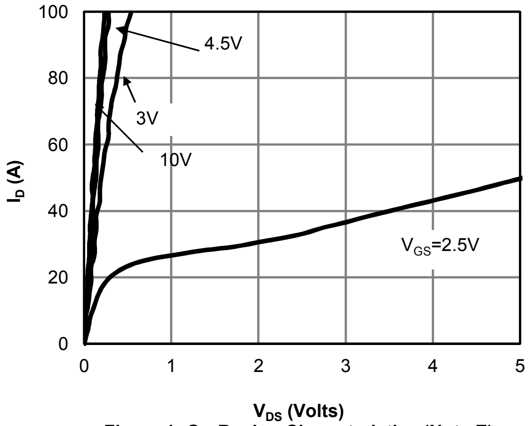


Figure 1: On-Region Characteristics (Note E)

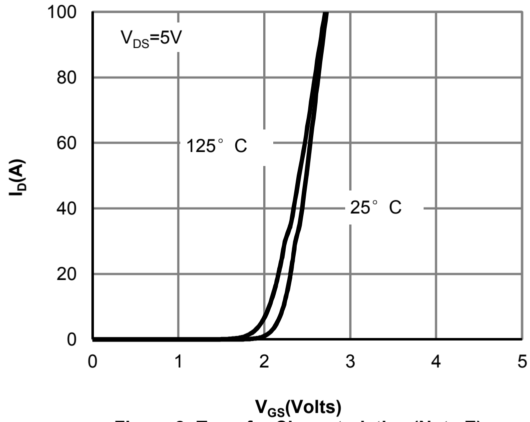


Figure 2: Transfer Characteristics (Note E)

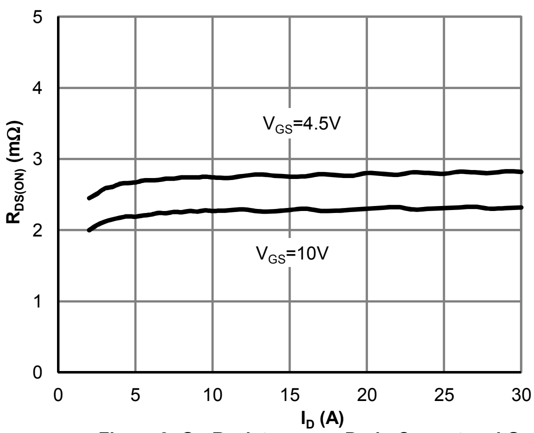


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

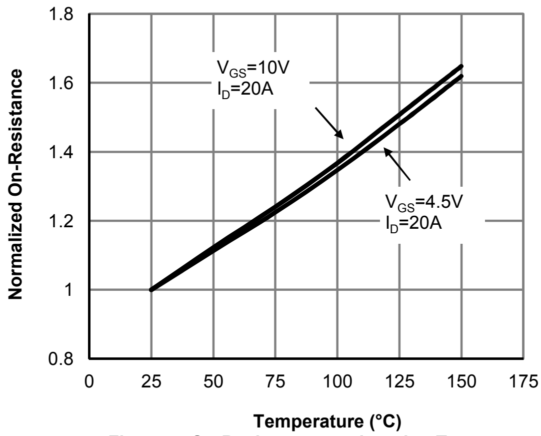


Figure 4: On-Resistance vs. Junction Temperature (Note E)

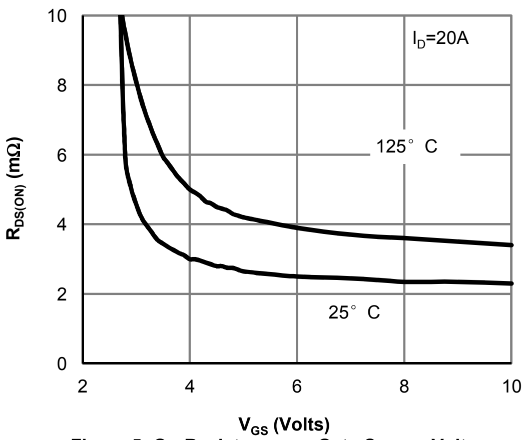


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

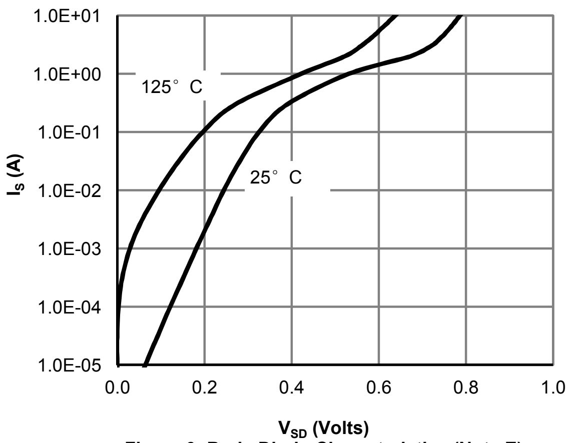


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

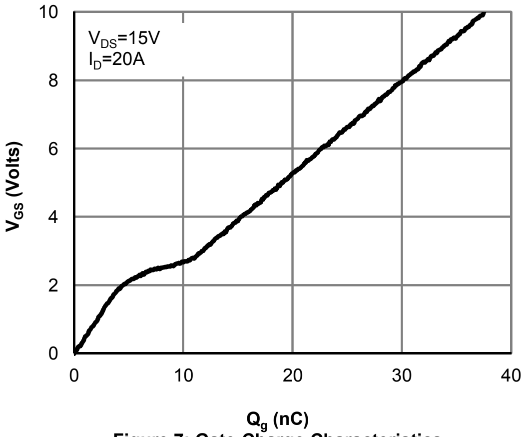


Figure 7: Gate-Charge Characteristics

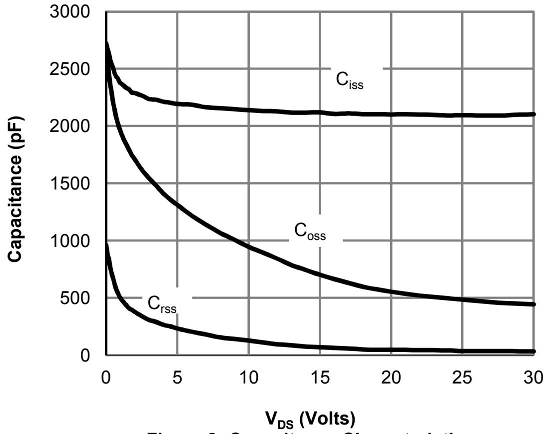
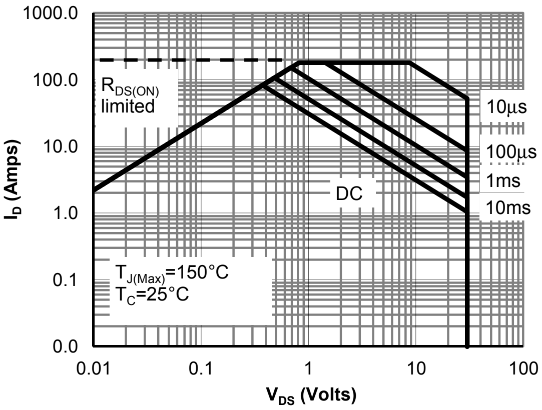


Figure 8: Capacitance Characteristics



V_{GS}> or equal to 4.5V

Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

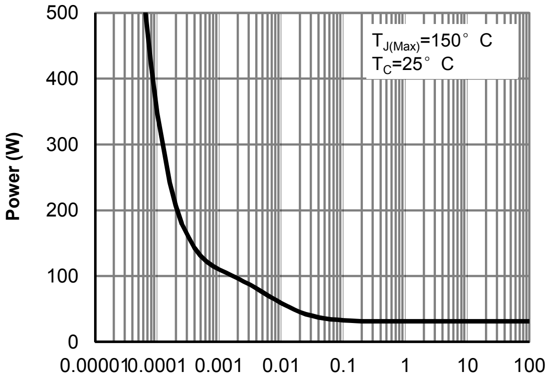


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

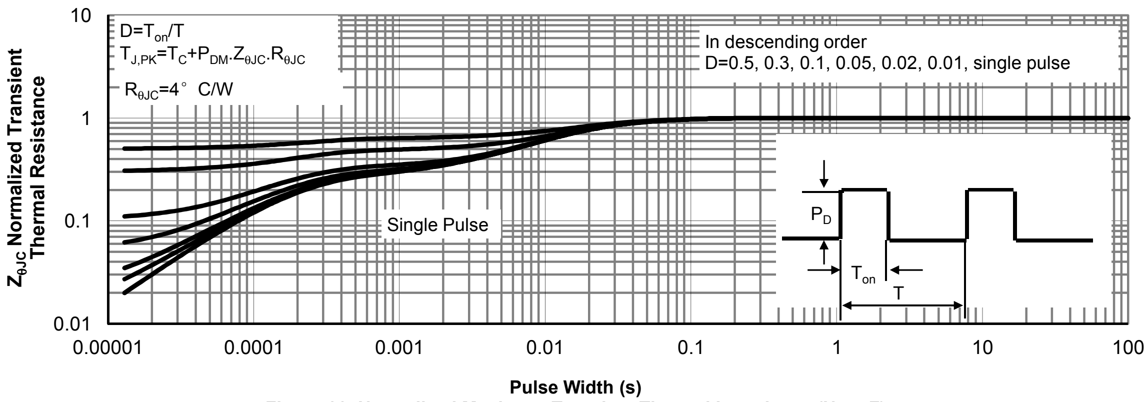


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

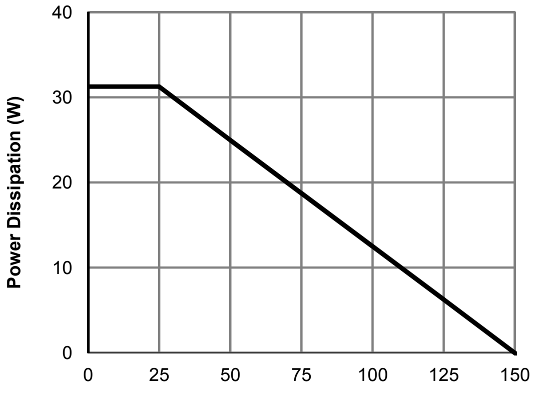
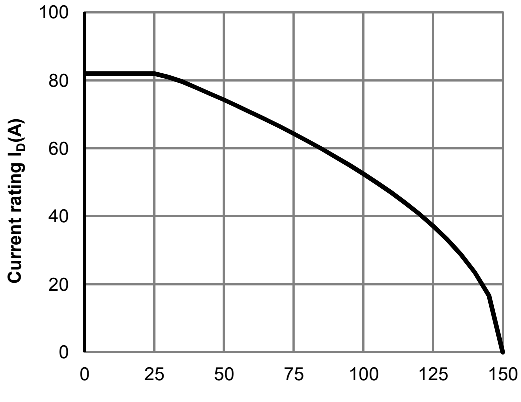


Figure 12: Power De-rating (Note F)



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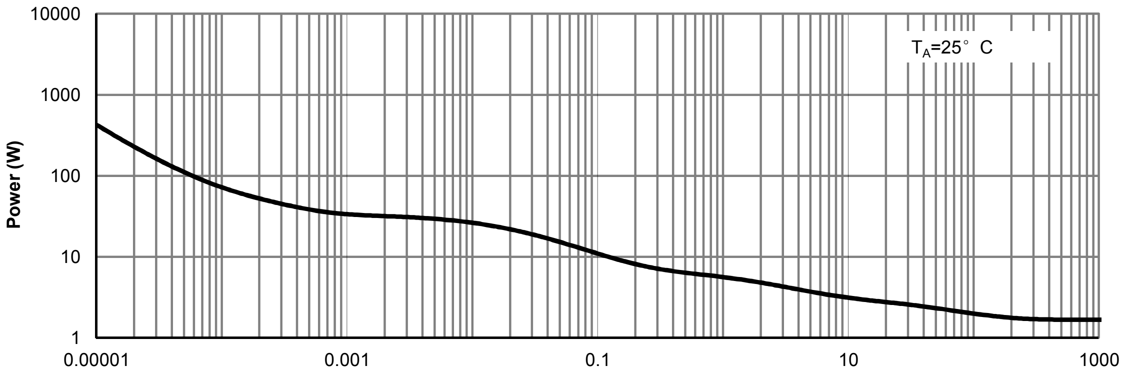


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

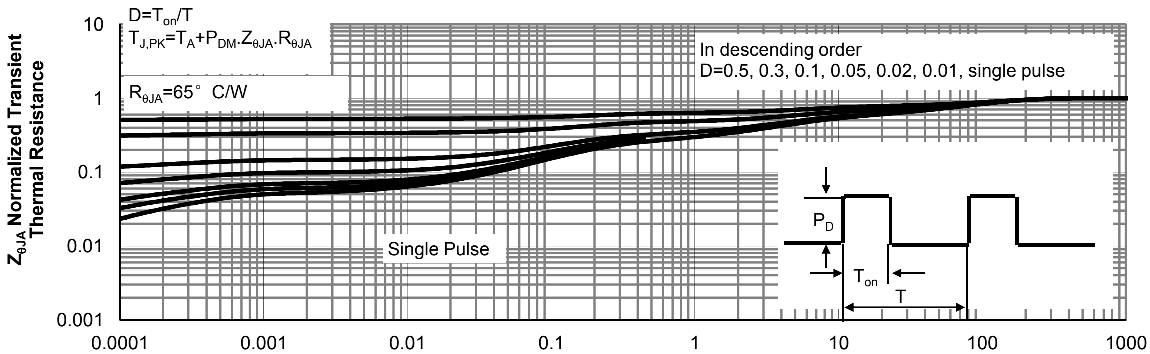
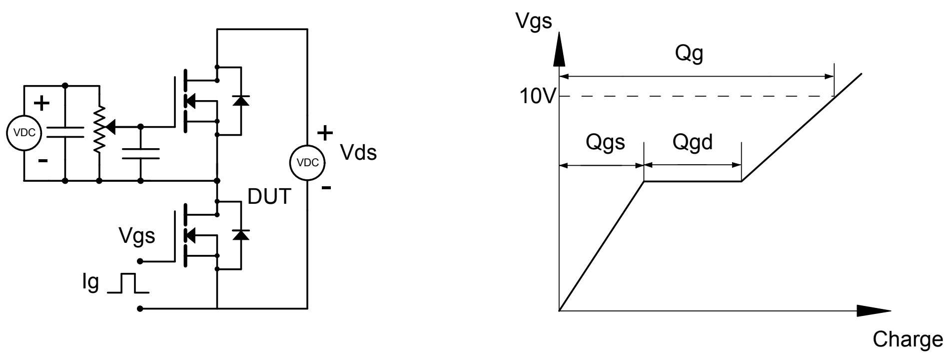
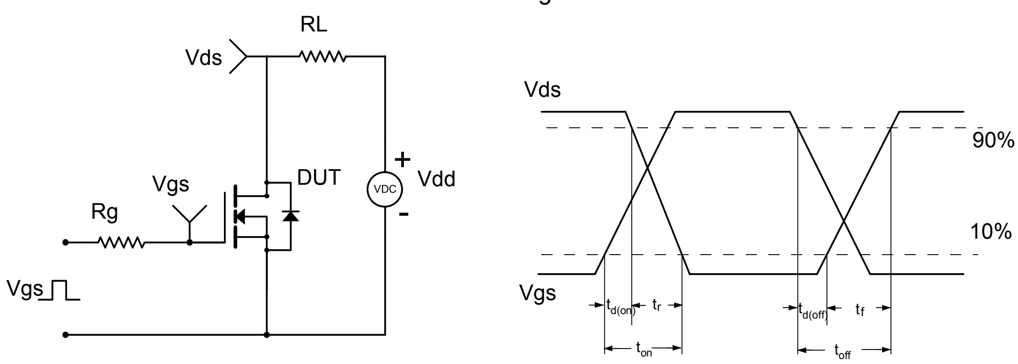


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

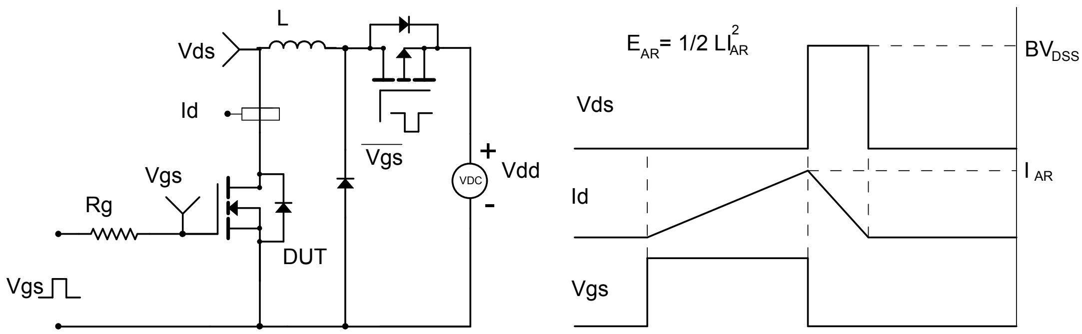
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms