



ALPHA & OMEGA
SEMICONDUCTOR

AOD4504
200V N-Channel MOSFET

General Description

The AOD4504 combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is ideal for boost converters and synchronous rectifiers for consumer, telecom, industrial power supplies and LED backlighting.

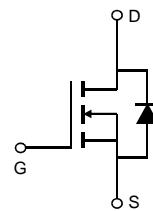
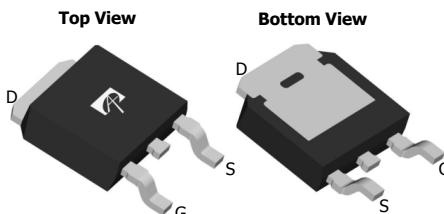
Product Summary

V_{DS}	200V
I_D (at $V_{GS}=10V$)	6A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 400m Ω

100% UIS Tested
100% R_g Tested



TO252
DPAK



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	200	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^A	I_D	6	A
$T_C=100^\circ\text{C}$		4.5	
Pulsed Drain Current ^C	I_{DM}	10	
Continuous Drain Current ^A	I_{DSM}	1.5	A
$T_A=70^\circ\text{C}$		1	
Avalanche Current ^C	I_{AS}	3	A
Avalanche energy $L=3.9\text{mH}$ ^C	E_{AS}	18	mJ
Power Dissipation ^B	P_D	42.5	W
$T_C=100^\circ\text{C}$		21	
Power Dissipation ^A	P_{DSM}	2.5	W
$T_A=70^\circ\text{C}$		1.6	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	°C

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A $t \leq 10\text{s}$	$R_{\theta JA}$	15	20	°C/W
Maximum Junction-to-Ambient ^{A,D} Steady-State		41	50	°C/W
Maximum Junction-to-Case	$R_{\theta JC}$	2.9	3.5	°C/W

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	200			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=200\text{V}, V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1 5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}, V_{GS}=\pm20\text{V}$			±100	nA
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1.7	2.8	3.7	V
$I_{\text{D(ON)}}$	On state drain current	$V_{GS}=10\text{V}, V_{DS}=5\text{V}$	10			A
$R_{\text{DS(ON)}}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}, I_D=3\text{A}$ $T_J=125^\circ\text{C}$	333 666	400 800		$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}, I_D=3\text{A}$	7			S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}, V_{GS}=0\text{V}$	0.75	1		V
I_S	Maximum Body-Diode Continuous Current				6	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=100\text{V}, f=1\text{MHz}$		328		pF
C_{oss}	Output Capacitance			20.5		pF
C_{rss}	Reverse Transfer Capacitance			8		pF
R_g	Gate resistance	$V_{GS}=0\text{V}, V_{DS}=0\text{V}, f=1\text{MHz}$	1	2	3	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}, V_{DS}=100\text{V}, I_D=3\text{A}$		82	115	nC
$Q_g(4.5\text{V})$	Total Gate Charge			44	53	nC
Q_{gs}	Gate Source Charge			16		nC
Q_{gd}	Gate Drain Charge			30		nC
$t_{\text{D(on)}}$	Turn-On Delay Time	$V_{GS}=10\text{V}, V_{DS}=100\text{V}, R_L=33.3\Omega, R_{\text{GEN}}=3\Omega$		6		ns
t_r	Turn-On Rise Time			3.5		ns
$t_{\text{D(off)}}$	Turn-Off Delay Time			18		ns
t_f	Turn-Off Fall Time			3		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=3\text{A}, dI/dt=500\text{A}/\mu\text{s}$		35		ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=3\text{A}, dI/dt=500\text{A}/\mu\text{s}$		150		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{ C}$. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150° C . The value in any given application depends on the user's specific board design, and the maximum temperature of 175° C may be used if the PCB allows it.

B. The power dissipation P_D is based on $T_{J(\text{MAX})}=175^\circ\text{ C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(\text{MAX})}=175^\circ\text{ C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^\circ\text{ C}$.

D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

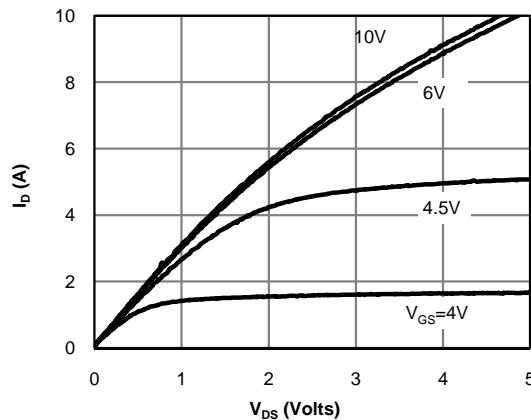
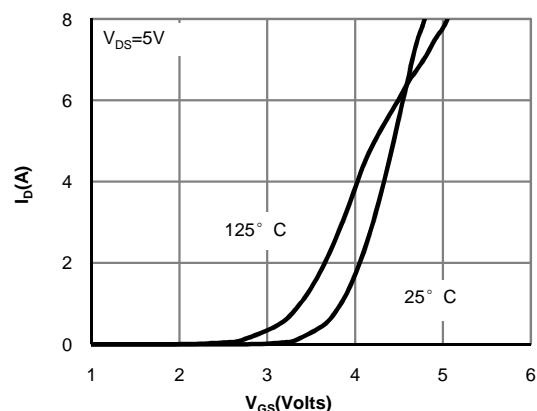
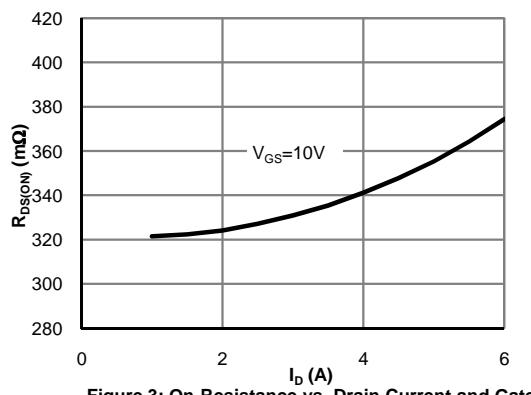
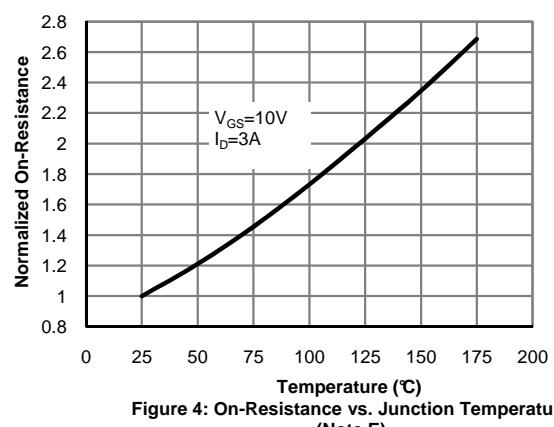
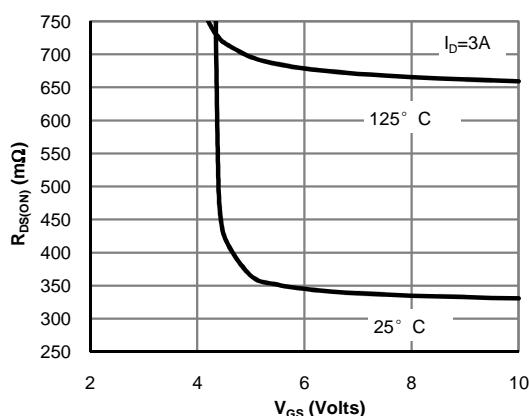
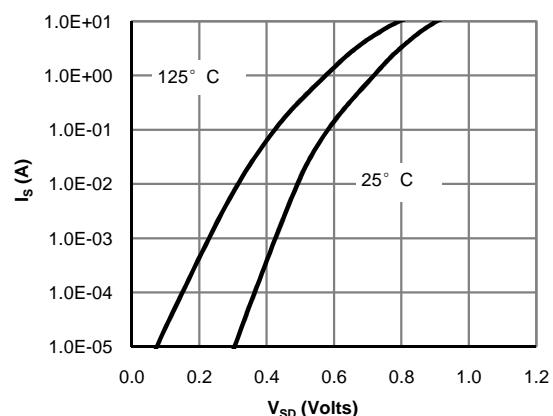
E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

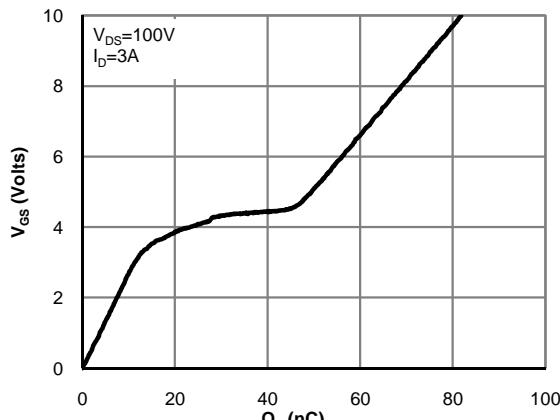
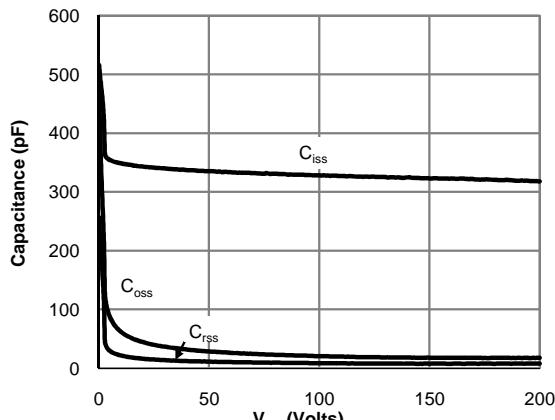
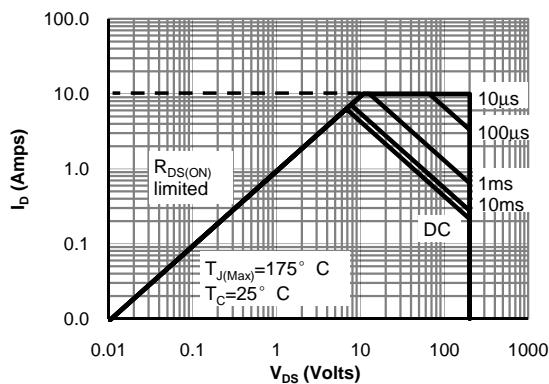
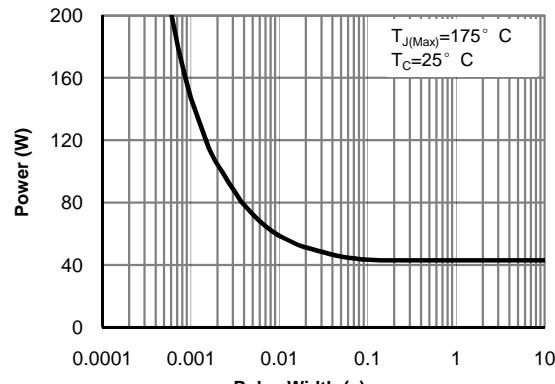
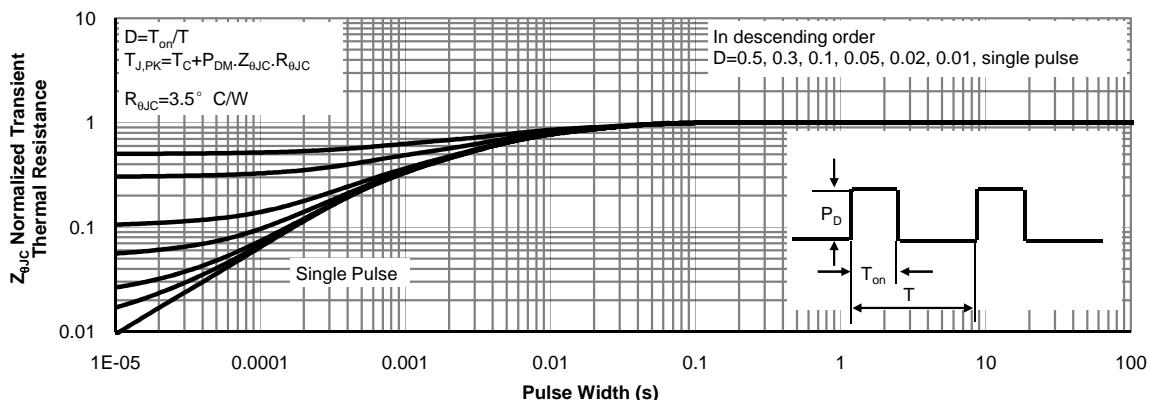
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(\text{MAX})}=175^\circ\text{ C}$. The SOA curve provides a single pulse rating.

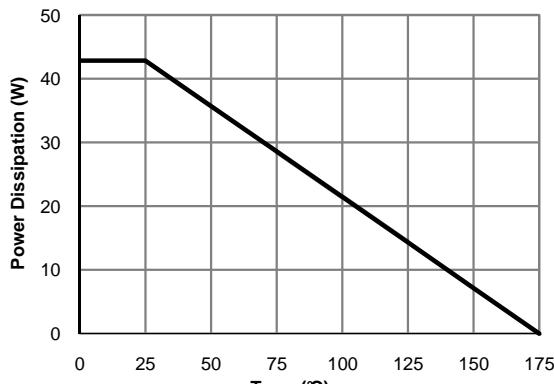
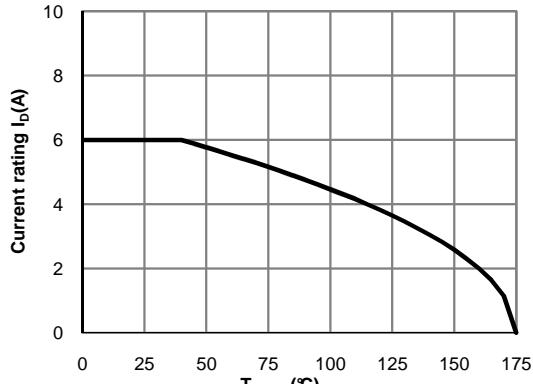
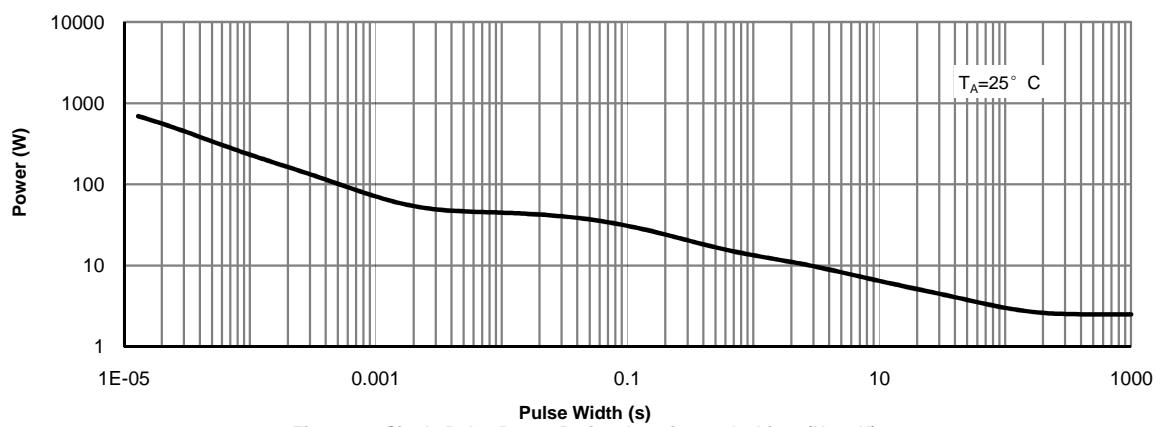
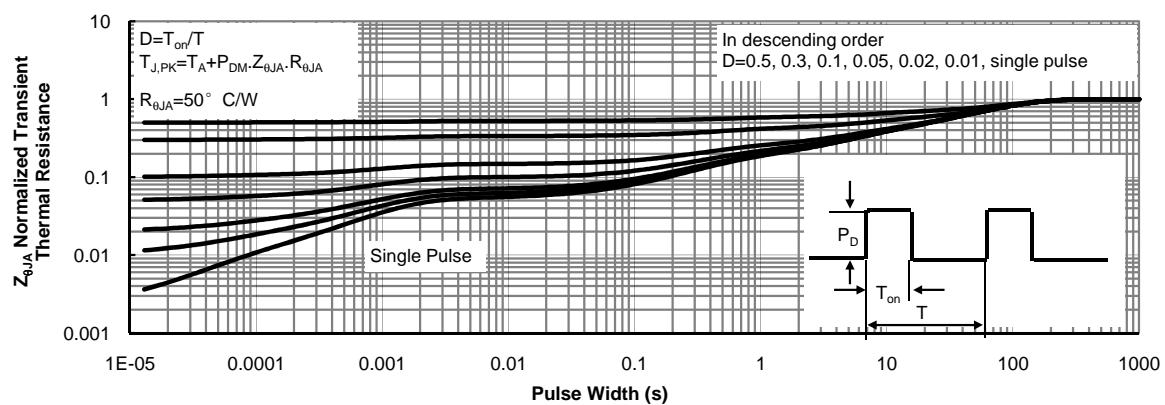
G. The maximum current rating is package limited.

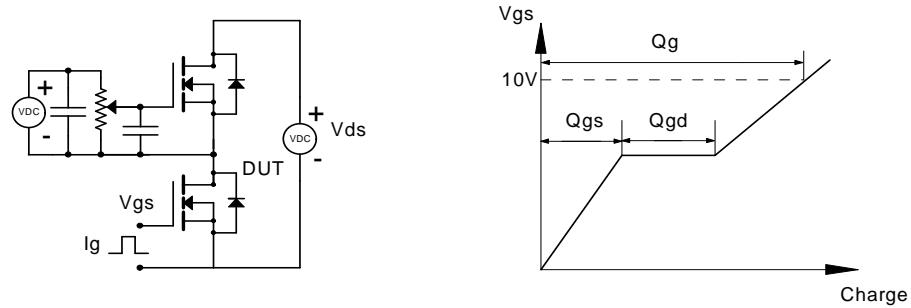
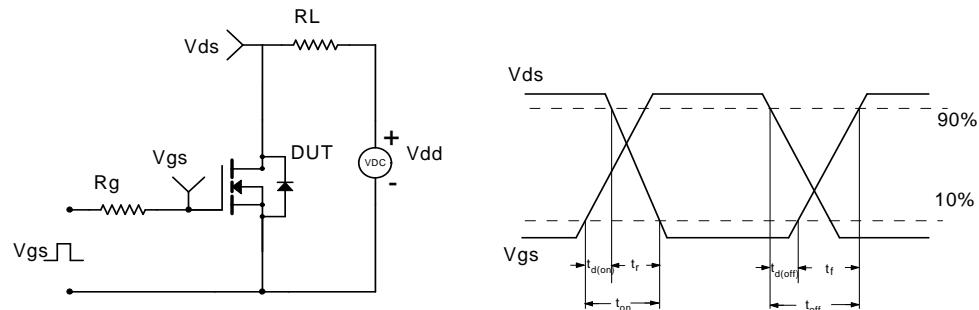
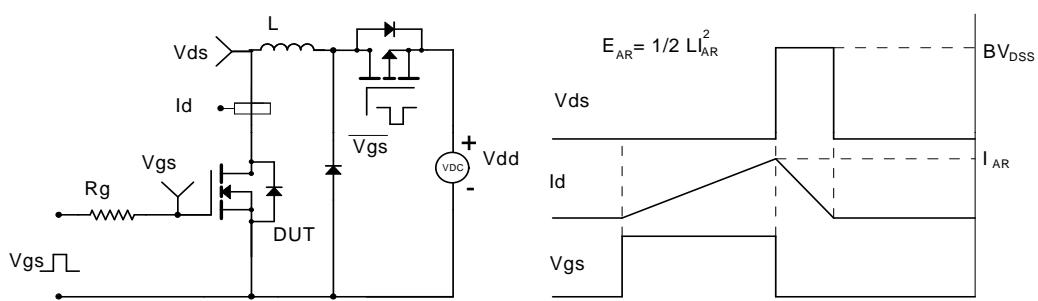
H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{ C}$.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

Fig 1: On-Region Characteristics (Note E)

Figure 2: Transfer Characteristics (Note E)

Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

Figure 4: On-Resistance vs. Junction Temperature (Note E)

Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

Figure 7: Gate-Charge Characteristics

Figure 8: Capacitance Characteristics

Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

Figure 12: Power De-rating (Note F)

Figure 13: Current De-rating (Note F)

Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

Gate Charge Test Circuit & Waveform

Resistive Switching Test Circuit & Waveforms

Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

Diode Recovery Test Circuit & Waveforms
