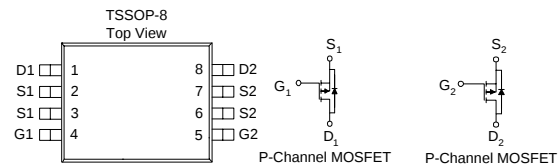


P-Channel 20-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe TSSOP-8 saves board space
- Fast switching speed
- High performance trench technology

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (OHM)	I_D (A)
-20	0.050 @ $V_{GS} = -4.5V$	-4.0
	0.060 @ $V_{GS} = -2.5V$	-3.6
	0.075 @ $V_{GS} = -1.8V$	-3.2



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ UNLESS OTHERWISE NOTED)			
Parameter		Symbol	Maximum Units
Drain-Source Voltage		V_{DS}	-20 V
Gate-Source Voltage		V_{GS}	± 8
Continuous Drain Current ^a	$T_A = 25^\circ C$	I_D	-4.0
	$T_A = 70^\circ C$		-3.2
Pulsed Drain Current ^b		I_{DM}	-10 A
Continuous Source Current (Diode Conduction) ^a		I_S	± 1.6 A
Power Dissipation ^a	$T_A = 25^\circ C$	P_D	1.15
	$T_A = 70^\circ C$		0.7
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150 $^\circ C$

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typ	Max	
Maximum Junction-to-Ambient ^a	$t \leq 10$ sec	R_{thJA}	93	110	$^\circ C/W$
	Steady State		130	150	

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

SPECIFICATIONS (T _A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 uA	-0.40			
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = +/-12 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -16 V, V _{GS} = 0 V			-1	uA
		V _{DS} = -16 V, V _{GS} = 0 V, T _J = 55°C			-10	
On-State Drain Current ^A	I _{D(on)}	V _{DS} = -5 V, V _{GS} = -10 V	-3			A
Drain-Source On-Resistance ^A	r _{DS(on)}	V _{GS} = -4.5 V, I _D = -4.0 A			0.050	Ω
		V _{GS} = -2.5 V, I _D = -3.6 A			0.060	
		V _{GS} = -1.8 V, I _D = -3.2 A			0.075	
Forward Tranconductance ^A	g _{fs}	V _{DS} = -5 V, I _D = -4.0 A		3		S
Diode Forward Voltage	V _{SD}	I _S = -1.6 A, V _{GS} = 0 V		-0.70		V
Dynamic ^b						
Total Gate Charge	Q _g	V _{DS} = -5 V, V _{GS} = -4.5 V, I _D = -4.0 A		12.2		nC
Gate-Source Charge	Q _{gs}			1.1		
Gate-Drain Charge	Q _{gd}			1.5		
Turn-On Delay Time	t _{d(on)}	V _{DD} = -5 V, R _L = 5 OHM, V _{GEN} = -4.5 V, R _G = 6 OHM		6.5		ns
Rise Time	t _r			20		
Turn-Off Delay Time	t _{d(off)}			31		
Fall-Time	t _f			21		

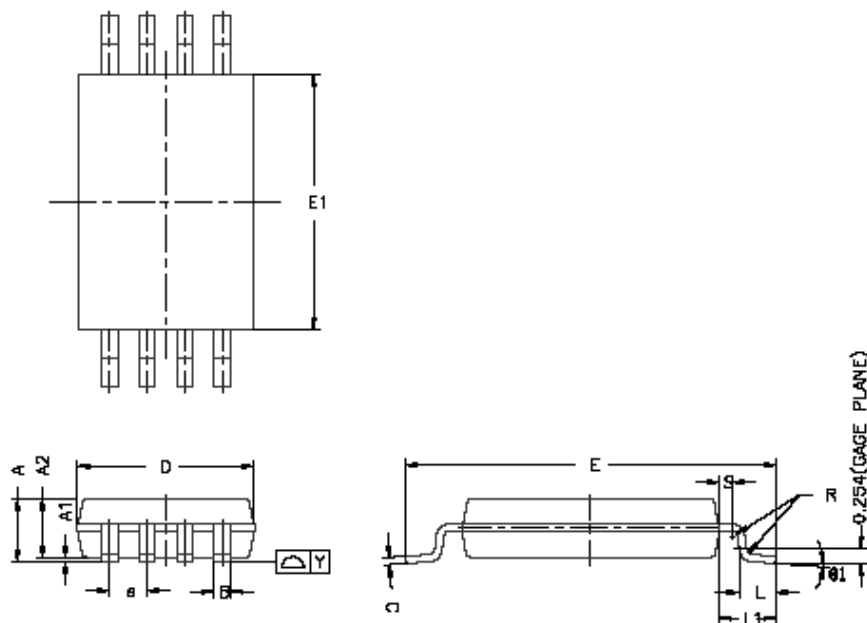
Notes

- Pulse test: $PW \leq 300\mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

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Package Information

TSSOP-8: 8LEAD



DIM.	MILLIMETERS		
	MIN.	NDM.	MAX.
A	1.05	1.10	1.20
A(1)	0.05	0.10	0.15
A(2)	0.99	1.02	1.05
B	0.19	0.25	0.30
C	---	0.127	---
D	2.90	3.00	3.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
a	0.635SC		
L	0.45	0.60	0.75
L1	0.90	1.00	1.10
Y	---	---	0.10
Ø1	Ø	Ø	Ø
R	0.09	---	---
S	0.20	---	---