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A New High Performance Current-Mode Controller Teams Up with Current Sensing Power MOSFETs

By
Jade Alberkrack
Warren Schultz
Motorola, SPS

ABSTRACT

A new current-mode control IC that interfaces directly with current sensing power MOSFETs is described. Its second generation architecture is shown to provide a variety of advantages in current-mode power supplies. The most notable of these advantages is a "lossless" current sensing capability that is provided when used with current sensing MOSFETs.

Included in the discussion are subtle factors to watch out for in practical designs, and an applications example.

INTRODUCTION

Current-mode control is well known for the dynamic performance advantages that it brings to switching power supplies. In response to these advantages, two generations of integrated circuits have been developed. The first generation simplified component counts and made current-mode topologies economically competitive. Second generation products have focused on two additional types of improvements. One approach emphasizes high speeds in critical control loops. The other emphasizes CMOS like bias power requirements and compatibility with current sensing power MOSFETs.

Motorola's MC34129 fits into the second category. Its architecture provides very low bias power consumption, 300 kHz operation, and full compatibility with current sensing power MOSFETs. The latter advantage is particularly important since it allows more efficient current sensing. Instead of running amps through a power sense resistor, primary current is split into power and sense components by new power MOSFETs called SENSEFETs. The sense portion, typically milliamps, is run through a 1/4 watt sense resistor while the power component flows unimpeded to ground. Since power dissipation in the sense resistor is reduced by several orders of magnitude, the circuit technique is called lossless current sensing.

Fully taking advantage of lossless current sensing's benefits requires a control circuit topology which differs somewhat from first generation current-mode control IC's. The MC34129 fills the void with its second generation design.

MC34129 DESCRIPTION

In order to work well with SENSEFETs, current-mode control circuitry has to accept relatively low values of sense voltage. First generation current-mode control IC's will accept these voltages during regulation, but are often found lacking under short circuit conditions. Short circuit current limit thresholds usually exceed sense voltages that are practically attainable with SENSEFETs.

The MC34129 has an architecture which works quite well with SENSEFET output voltages, and provides a number of other features. An illustration of the circuit and a timing diagram are included in Figure 1. A block by block description follows from this figure.

Oscillator:

The oscillator is programmed for operating frequency and maximum duty cycle by components R_T and C_T. Capacitor C_T is charged from a 2.5 volt reference through resistor R_T to approximately 1.25 volts and discharged by an internal current sink to ground. During the discharge of C_T, an internal blanking pulse is generated that holds the NOR gate's lower input high. This arrangement causes the Drive Output (Pin 1) to be in a low state, thereby producing a controlled amount of dead time. Note that many values of R_T and C_T will give the same oscillator frequency but only one combination will yield a specific deadtime at a given frequency.

For many noise sensitive applications, it is desirable to frequency lock one or more switching regulators to an external clock. This can be accomplished by applying a clock signal to the Sync/Inhibit Input. For reliable locking, R_T and C_T should be set for approximately 10% less than the external clock frequency. Operation is illustrated by timing waveforms in Figure 1. The external clock's rising edge terminates charging of C_T and forces Pin 1 low. As long as the clock is high, Pin 1 remains low. At the clock's falling edge C_T begins charging again, Pin 1 is enabled, and the cycle repeats.

By tailoring the clock waveform, accurate duty cycle clamping of the Drive Output can be achieved. The Sync/Inhibit Input may also be used as a means for system shutdown by applying a dc voltage that is within the range of 2 volts to V_{CC}.

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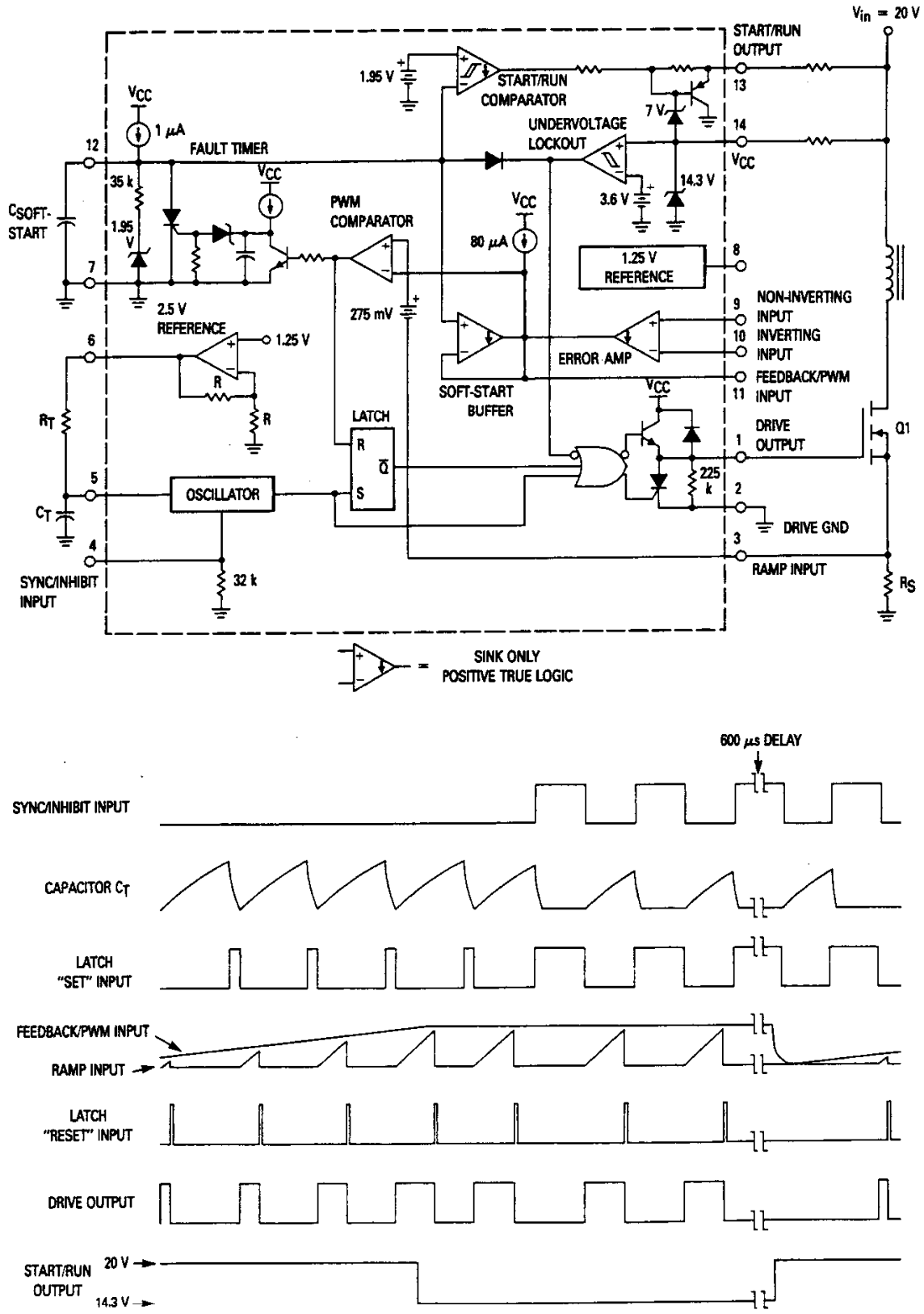

Figure 1. Block Diagram and Timing Waveforms

PWM Comparator and Latch:

The MC34129's PWM architecture is designed such that output switch conduction is initiated by the oscillator and terminated when peak inductor current reaches a threshold level. A unique arrangement establishes the threshold level with an Error Amp and Soft Start Buffer whose outputs are tied together at Pin 11. This arrangement controls peak inductor current on a cycle by cycle basis regardless of whether duty cycle is limited by the error signal, soft start, or an output fault. The PWM Comparator-Latch configuration that is used, ensures that only a single pulse appears at the Drive Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting a ground-referenced resistor R_S in series with the Sense terminal of a SENSEFET or Source of a conventional power MOSFET.

The Ramp Input adds 275 millivolts of offset to whatever sense voltage is developed by R_S. This guarantees that no output pulses will appear when Pin 11 is at its lowest state, and provides adequate margin to overcome the error amplifier's minimum output voltage.

Under normal operating conditions, peak inductor current $I_{(pk)}$ is controlled by the voltage at Pin 11 such that:

$$I_{pk} = \frac{V\ (Pin\ 11) - 275\ mV}{(R_S/K)}$$

In this equation K is the ratio of inductor current to sense current. For conventional sense resistors, K is 1, and for SENSEFET applications K is the ratio of Drain current to Sense current.

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the PWM comparator's inverting input (Pin 11) will assume the error amp's maximum output voltage. This voltage determines peak switch current, and is clamped internally to 1.95 volts. Compatibility with SENSEFETs is provided by a configuration that easily allows clamping to much lower levels. One method is shown in Figure 2. It uses an external divider and a diode to clamp Pin 11's maximum voltage, and thereby adjust peak fault current. A second diode uses negative input bias current from Pin 3 (typically 120 μA) to provide compensation for the diode drop at Pin 11. Maximum switch current can be calculated as follows:

$$I_{p(max)} = \left(\frac{1.25\ R1}{R1 + R2} - 0.275\right) \cdot K/R_S$$

Although this expression is straightforward, it is important to note that high frequency layout techniques are imperative.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit instability when its output is lightly loaded. This spike is due to power transformer interwinding capacitance, output rectifier recovery charge, and SENSEFET characteristics. The addition of an RC filter on the Ramp Input with a time constant that approximates the spike duration will usually eliminate the instability. A typical connection is shown in Figure 3.

Error Amp and Soft Start Buffer:

A fully compensated Error Amplifier with access to its output and both inputs is provided for maximum design flexibility. The Error Amplifier output is tied to the output of the Soft Start Buffer. These outputs are open collector (sink only) and feed the inverting input of the PWM Comparator. With this configuration, the amplifier that demands lower peak inductor current dominates control of the PWM loop.

The Soft Start Buffer is configured as a unity gain follower with its non-inverting input connected to Pin 12.

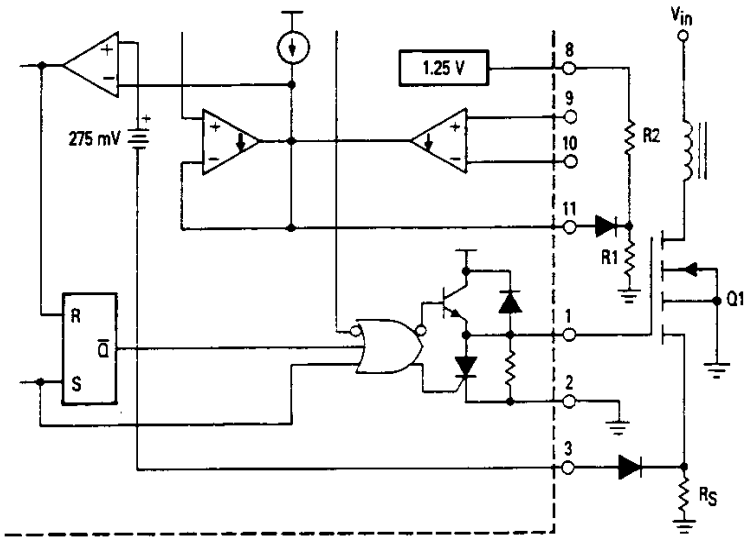

Figure 2. Fault Current Adjustment

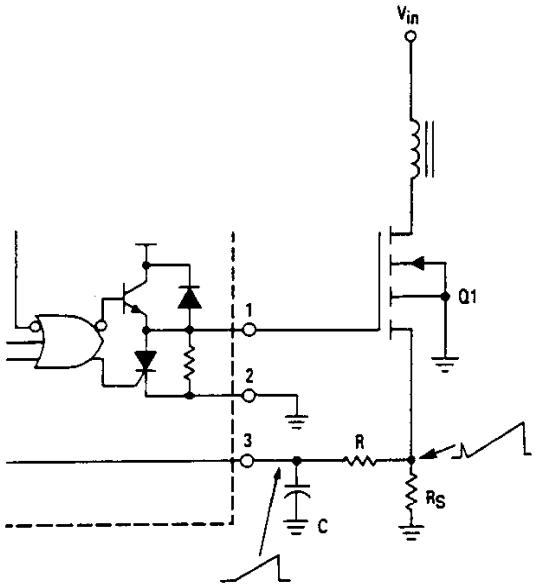

Figure 3. Ramp Filter

An internal 1 μA current source charges the soft-start capacitor ($C_{soft\text{-}start}$) to Pin 11's clamp voltage. The rate of change of peak inductor current during startup is programmed by the capacitor value selected.

Fault Timer:

This unique circuit prevents sustained operation in a lockout condition. Lockout can occur with conventional switching control IC's when operating from a power source with a high series impedance. If power required by the load is greater than power available from the source, input voltage will collapse and cause a lockout condition. The Fault Timer provides automatic recovery when this condition is detected. Under normal operating conditions the PWM Comparator will reset the Latch and discharge the Fault Timer's internal capacitor on a cycle-by-cycle basis. Under operating conditions where input power is insufficient for the load, Ramp Input Voltage (plus offset) will not reach the threshold established at Pin 11, and the PWM Comparator's output will remain low. If this condition persists for more than 600 μs, the Fault Timer will activate, discharging $C_{soft\text{-}start}$ and initiating a soft-start cycle. The power supply will operate in a skip cycle or hiccup mode until either the load, or source impedance, is reduced. When either occurs, normal operation resumes automatically.

Start/Run Comparator:

A bootstrap startup circuit is included to improve system efficiency when operating from a high input voltage. For this purpose, a Start/Run Comparator controls the state of an external transistor. A typical application is shown in Figure 4. While $C_{soft\text{-}start}$ is charging, startup bias is supplied to V_{CC} (Pin 14) from V_{in} through transistor Q2. When $C_{soft\text{-}start}$ reaches 1.95 volts, the Start/

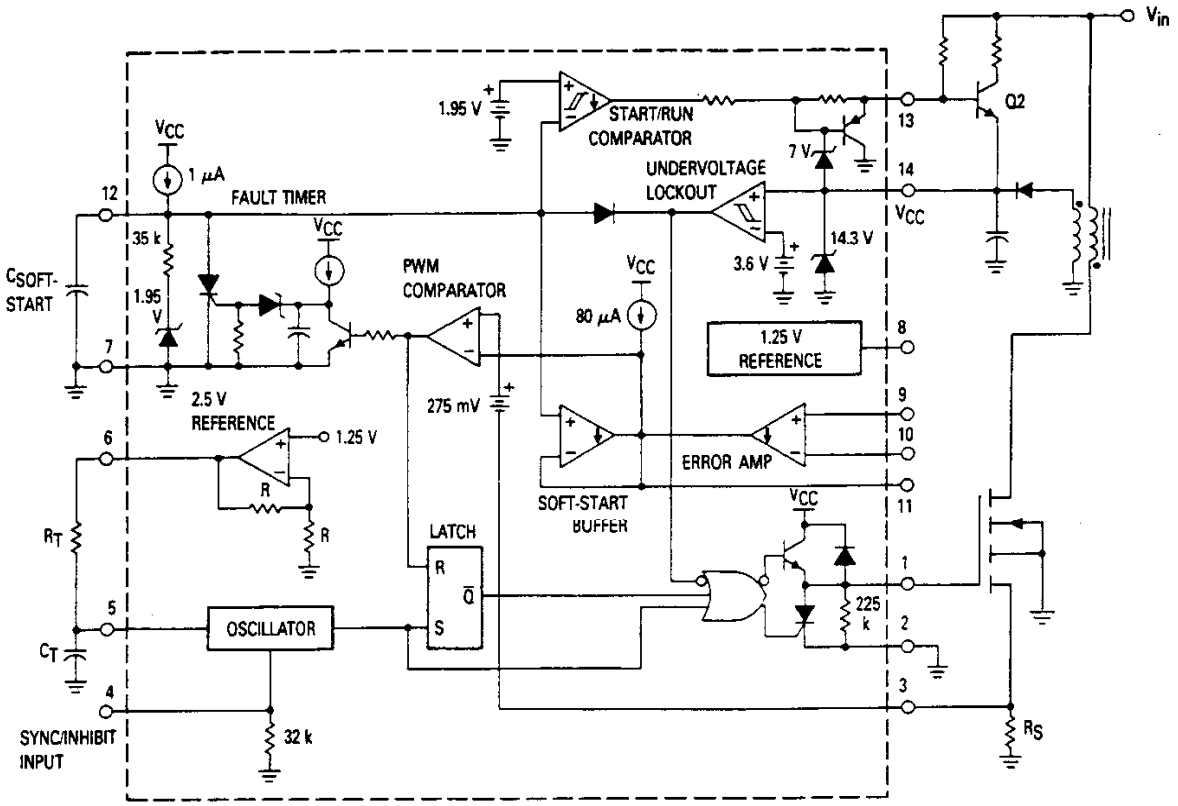

Figure 4. Bootstrap Bias

Run output switches low and turns off Q2. Operating bias is now derived from an auxiliary bootstrap winding, and drive power is efficiently converted down from V_{in}. A smooth switchover is facilitated by 350 mV of hysteresis in the Start/Run Comparator.

An important constraint is that start time must be long enough for the power supply to reach regulation. This ensures that there is sufficient bias voltage at the auxiliary winding for sustained operation. An adequate value of $C_{soft\text{-}start}$ can be determined from the following expression:

$$t_{start} = \frac{1.95\ V \cdot C_{soft\text{-}start}}{1\ \mu A} = 1.95\ C_{soft\text{-}start}\ \text{in}\ \mu F$$

In addition, use of the Start/Run feature implies that the error amplifier's maximum output voltage has not been clamped externally.

Drive Output and Drive Ground:

The MC34129 contains a single totem-pole output stage that is specifically designed for direct drive of power MOSFET's. It is capable of up to ±1 amps peak drive current and has a typical fall time of 30 ns with a 500 pF load. The totem-pole stage consists of an NPN transistor for turn-on drive and a high speed SCR for turn-off. The SCR design requires less average supply current (I_{CC}) than conventional switching control IC's that use all NPN totem-poles. The improvement comes during turn-off, where the SCR is able to use the power MOSFET's gate charge as regenerative on-bias. In contrast, a conventional all transistor design requires continuous base current. The improvement is large enough to allow bias from a series dropping resistor in many high input voltage applications.

An internal 225 kΩ pull-down resistor is included to shunt the Drive Output to ground when Undervoltage Lockout is active. In addition, a separate Drive Ground is provided in order to reduce the effects of switching transient noise imposed on the Ramp Input. This feature becomes particularly useful when ramp voltage is provided by a current sensing power MOSFET.

Undervoltage Lockout:

An Undervoltage Lockout comparator holds both Drive Output and $C_{soft\text{-}start}$ pins low when V_{CC} is less than 3.6 volts. This ensures that the MC34129 is fully functional before the output stage is enabled and a soft-start cycle begins. Built in hysteresis of 350 mV prevents erratic behavior as V_{CC} crosses the threshold voltage. In addition, a 14.3 volt zener is connected as a shunt regulator to protect the output transistor's gate from excessive drive voltage during system startup. An external 9.1 volt zener is required when driving low threshold MOSFET's as shown in Figure 5. The minimum operating voltage range is 4.2 volts to 12 volts.

References:

Two reference voltages are provided. the 1.25 volt bandgap reference at Pin 8 is trimmed to a ±2% tolerance

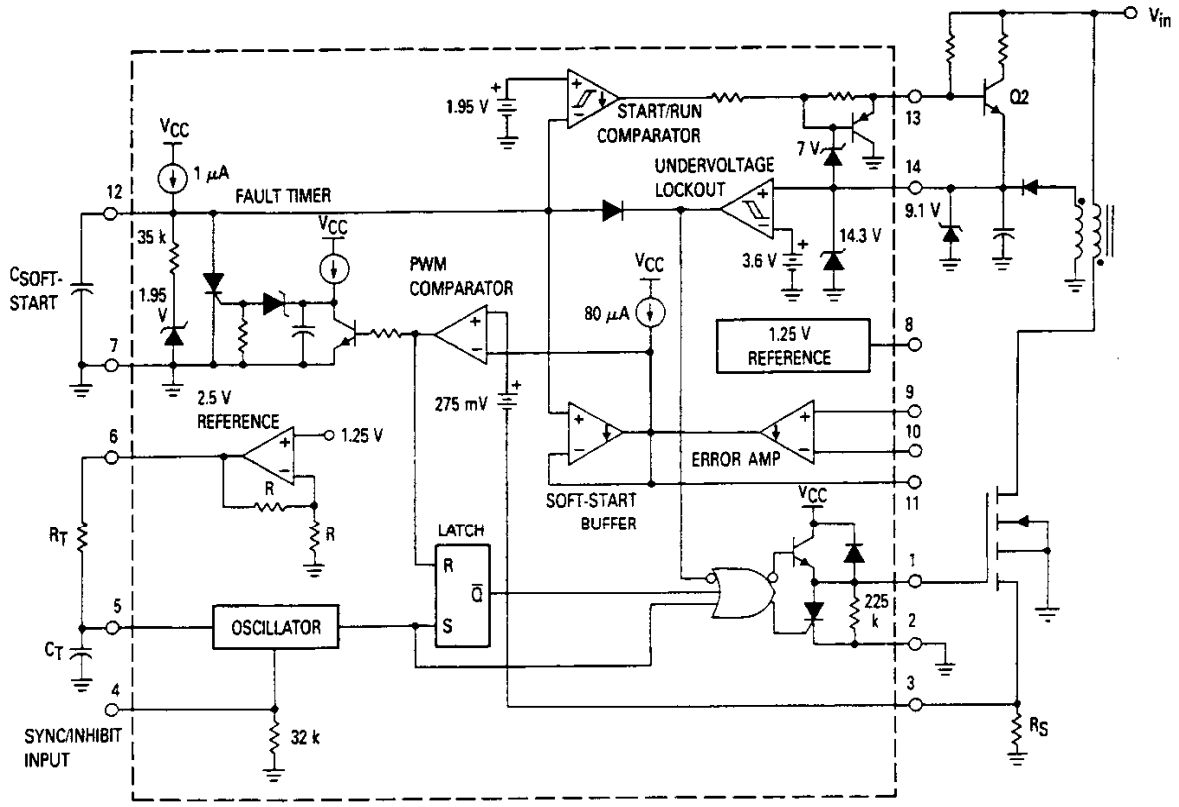

Figure 5. Gate Protection

at 25°C. It is intended to be used in conjunction with the Error Amp for output voltage regulation. An additional 2.5 volt reference is derived from the 1.25 volt bandgap by an internal Op amp that has a fixed gain of 2. It has a tolerance of ±5% at 25°C. Its primary purpose is to supply charging current for the oscillator's timing capacitor.

LOSSLESS CURRENT SENSING

Lossless current sensing is a new circuit technique that is particularly well suited to current-mode control. It is derived from the parallel nature of power MOSFETs and implemented with new devices called SENSEFETs. These new devices are five leaded power MOSFETs that have the usual Gate, Drain, and Source connections; plus Current Sensing and Kelvin Source pins. The Sense pin connects to a small fraction of many paralleled Source cells that make up a power MOSFET. The Kelvin connection provides a separate signal ground. A symbol and sense resistor connection are shown in Figure 6.

In the circuit of Figure 6, sense current is a small fraction of total drain current. Even at maximum rated drain current, sense current is only milliamps, allowing a signal level resistor to be used for R_S. Sense power is so small compared to using a power sense resistor that the circuit technique is called lossless current sensing.

Lossless current sensing is based upon the parallel nature of power MOSFETs, and the inherent tendency of individual paralleled cells in a monolithic structure to be well matched. Matching provides nearly equal on-resistance in each cell, and establishes a ratio between Sense current and Source current. When both Sense and Source leads are grounded this ratio approximates the cell ratio (n). In this situation, the Sense lead samples $1/(n+1)$ of a SENSEFET's total drain current.

Converting sense current to sense voltage in a resistor disturbs this ratio, but in a predictable way. Sense resistance attenuates sense current in proportion to the amount that it increases total resistance in the sense leg. It is tempting to model sense resistor interaction with the circuit in Figure 7. From this model you would expect sense current to halve when R_S and the sense section's on-resistance ($r_{DM(on)}$) are equal.

Although this is a reasonable first order approximation for low voltage devices, two significant deviations make an accurate calculation of sense current rather complex. One of these is a non-linearity that results from the square law behavior of power MOSFETs. As R_S and sense voltage are increased, the sense section's drain-source voltage is decreased and $r_{DM(on)}$ increases non-linearly. The result is an apparent cell ratio n' that increases with increasing sense voltage. An approximate expression for n' can be derived from the model in Figure 7 as follows:

$$n' = \frac{n}{1 - \frac{V_{sense}\,(V_{GS} - V_T - 1/2\,V_{sense})}{V_{DS(on)}\,(V_{GS} - V_T - 1/2\,V_{DS(on)})}}$$

where V_{GS} is the applied gate-to-source voltage, V_T is gate-to-source threshold voltage, and V_{sense} is the sense voltage.

The foregoing expression is approximately valid for low voltage SENSEFETs such as the MTP10N10M at sense voltages up to 25% of $V_{DS(on)}$. However, there is another level of complexity that is not taken into account by Figure 7. Although sense cells and power cells have a parallel drain connection, they are not paralleled at the physically available drain terminal. Figure 8 shows why. The drain voltage that a sense cell actually sees is influenced by high current flowing through the power section. Apparent drain voltage at the sense cell includes voltage drops across channel and pinch regions, but does not include voltage drop in the N-epitaxial layer that supports

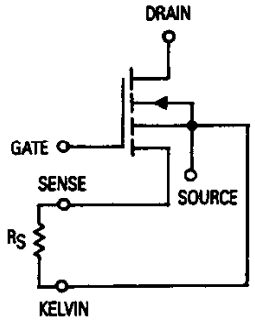

Figure 6. SENSEFET Symbol

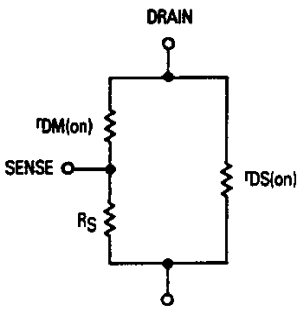

Figure 7. Current Sensing Model

breakdown. Therefore, a more appropriate model includes bulk resistance that is common to both power and sense cells. Figure 9 shows the resulting schematic.

Applying square law behavior to this model results in a rather complex calculation. Therefore, SENSEFET data sheets include curves of V_{sense} versus R_S at a fixed value of drain current and V_{sense} versus drain current for several values of sense resistance. Examples of these curves for an MTP10N10M, 10 amp/100 volt SENSEFET appear in Figures 10 and 11.

These curves illustrate a couple of interesting points. First, sense voltages are generally quite small. A 100 mV full load ramp voltage would not be unusual in a current-mode supply. Second, as the divergence in Figure 10 indicates, accuracy is maximized by minimizing R_S. In this case temperature tracking is almost perfect for values of R_S below 50 ohms, and diverges rapidly above 100

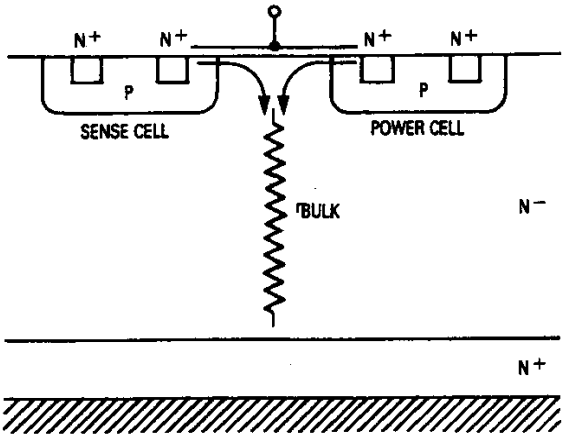

Figure 8. SENSEFET Cross-Sectional View

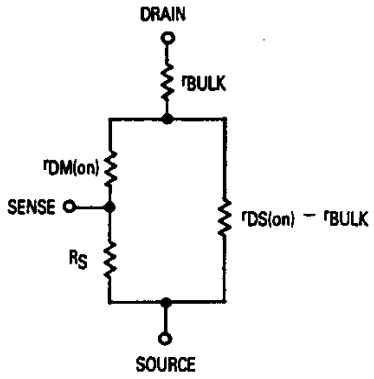

Figure 9. Refined Model

ohms. Initial tolerance follows a similar pattern. Below 20 ohms initial tolerance is within 6%, but increasing R_S to 2 kΩ increases this limit an estimated 25%.

The reason for this type of performance is simple. As R_S is minimized, the dependence of sense current upon matching within a monolithic device is maximized. On the other hand, as R_S is increased, sense current depends more and more on the ratio of a fixed external resistor to $r_{DM(on)}$, r_{BULK}, and $r_{DS(on)}$. Matching produces by far the best results.

USING THE MC34129 AND SENSEFETs TOGETHER

An example which illustrates how the MC34129 and SENSEFETs are used appears in Figure 12. This figure describes an isolated 12 volt to 5 volt current-mode supply, and is a convenient vehicle for describing how both parts work together.

Starting with the oscillator, R_T and C_T are selected for operating frequency and dead time. A combination of 13 k for R_T and 1500 pF for C_T produces 28 kHz operation with slightly less than 50% maximum duty cycle. Ramp voltage is generated by R_S and fed into the PWM comparator's non-inverting input at Pin 3. The ramp's magnitude is determined by the value of R_S, the amount of primary current (Ip) that is switched, and −120 μA of nominal input bias current that flows from Pin 3. With the aid of Figure 10,

$$V_{ramp} = 60\ mV/Amp \cdot Ip + 120\ \mu A \cdot 200\ \Omega$$
$$= 60\ mV/Amp \cdot Ip + 24\ mV$$

Knowing the relationship between V_{sense} and primary current, maximum short circuit current is set with voltage divider R1, R2. The output voltage from this divider is coupled through a unity gain Error Amp configuration to set the PWM comparator's upper trip point. To calculate the trip point, 275 mV of offset is added to the SENSEFET's output voltage. With the values shown, R1 and R2 set the upper trip point at 470 mV, and peak current is limited to approximately 2.8 amps.

Soft-start is provided with a 0.1 μF capacitor, which holds the output off for 27 ms, and allows full duty cycle after approximately 47 ms. The regulation loop is closed with an opto isolator which pulls down the voltage at Pin 9, thereby reducing peak primary current and also duty cycle. This configuration is advantageous in that it saves components. R1 and R2 are used to both limit peak current and provide a connection for the optoisolator.

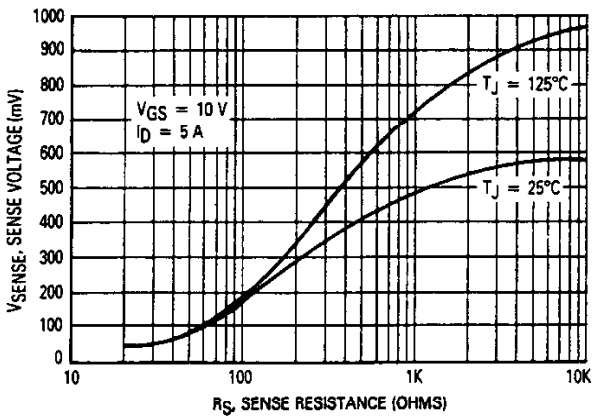

Figure 10. Sense Voltage versus Sense Resistance

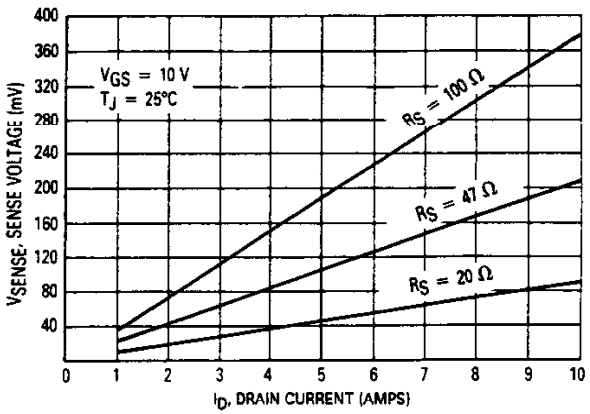

Figure 11. Drain Current versus Sense Voltage

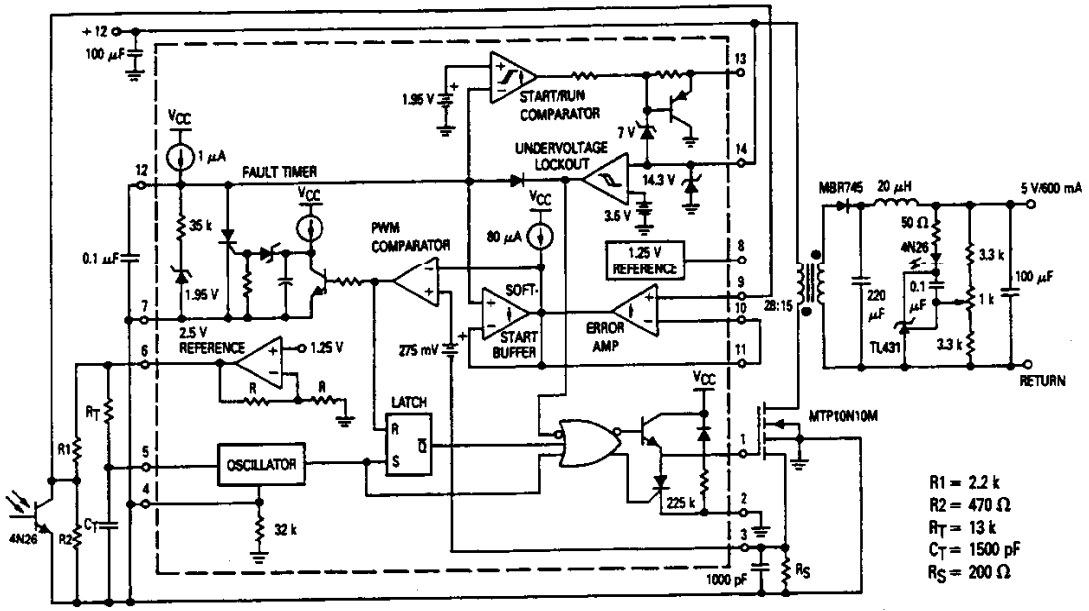

Figure 12. Application Example

SUBTLE CONSIDERATIONS

There are a number of subtle considerations that can be crucial in an MC34129/SENSEFET power supply. Several important issues are highlighted as follows.

Noise Suppression:

The MC34129 will drive a typical SENSEFET with transition times approaching 10 ns. At this speed, noise pickup in the current sensing circuitry can be a first order design issue. Layout, therefore, is critical. In addition, some filtering of the ramp input is usually desirable. To help with the layout problem, both MC34129 and SENSEFETs have separate power and signal ground pins. Use of these connections as indicated in Figure 12 can prevent noise related instability. At lower operating frequencies, series gate resistance can also be added to slow transition times, and create an optimum balance between switching losses and noise immunity.

Feedback:

The feedback configuration in Figure 12 has a number of interrelated constraints. One constraint is short circuit current. R1 and R2 are scaled to provide its desired value. These resistors are simultaneously subject to a 1 mA output current rating on the 2.5 volt reference. In addition, the opto transistor's collector works into an impedance determined by the parallel combination of R1 and R2. This configuration produces a voltage gain that influences loop gain, and therefore stability. With the components shown, a parallel combination of R1 and R2 that much exceeds 500 ohms tends to produce an open loop gain that is difficult to stabilize.

Opto Saturation:

In order to fully duty cycle the MC34129 back to zero, the opto transistor's collector has to pull Pin 9 below the voltage at the PWM comparator's non-inverting input. A 275 mV offset built into the MC34129 makes this relatively easy to do. However, the opto transistor's saturation voltage is a design consideration. Light load operation requires enough drive for the opto transistor to comfortably reach less than 275 mV of saturation voltage.

CONCLUSION

MC34129's and power SENSEFETs are significant new additions to the components available for current-mode control. By integrating power switching and current sense functions in a SENSEFET, and combining its features with the MC34129's control capabilities, simpler, more efficient, and more compact power supplies are possible.

Used together, these new components eliminate power sense resistors and make current-mode more attractive with respect to other architectures for switching power supplies. Both products will make a significant contribution in the shift toward current-mode topologies.

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