AN8420FBP (Under development)

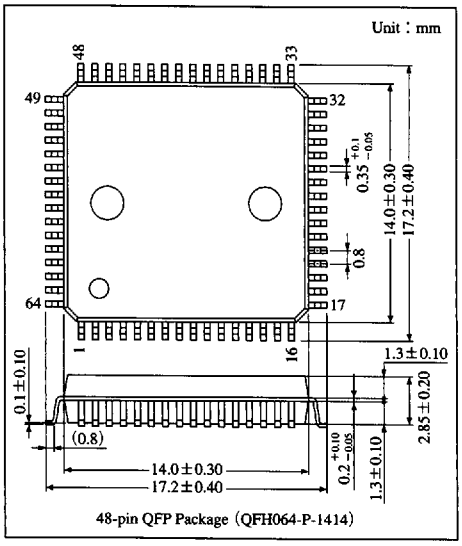
Spindle/Voice Coil Motor Drive IC

■ Overview

The AN8420FBP is an IC for the voice coil motor and the spindle motor drive of the hard disk drive system (HDD).

For the spindle motor drive, the acoustic noise level of the spindle motor can be greatly improved by the sensor-less soft switch system.

The voice coil motor drive consists of the power amp. circuits. Also, the AN8420FBP incorporates the auto-retraction circuit which uses the B-EMF of the spindle motor, and the reduced voltage detection circuit. Thus, it is optimum composition for HDD.



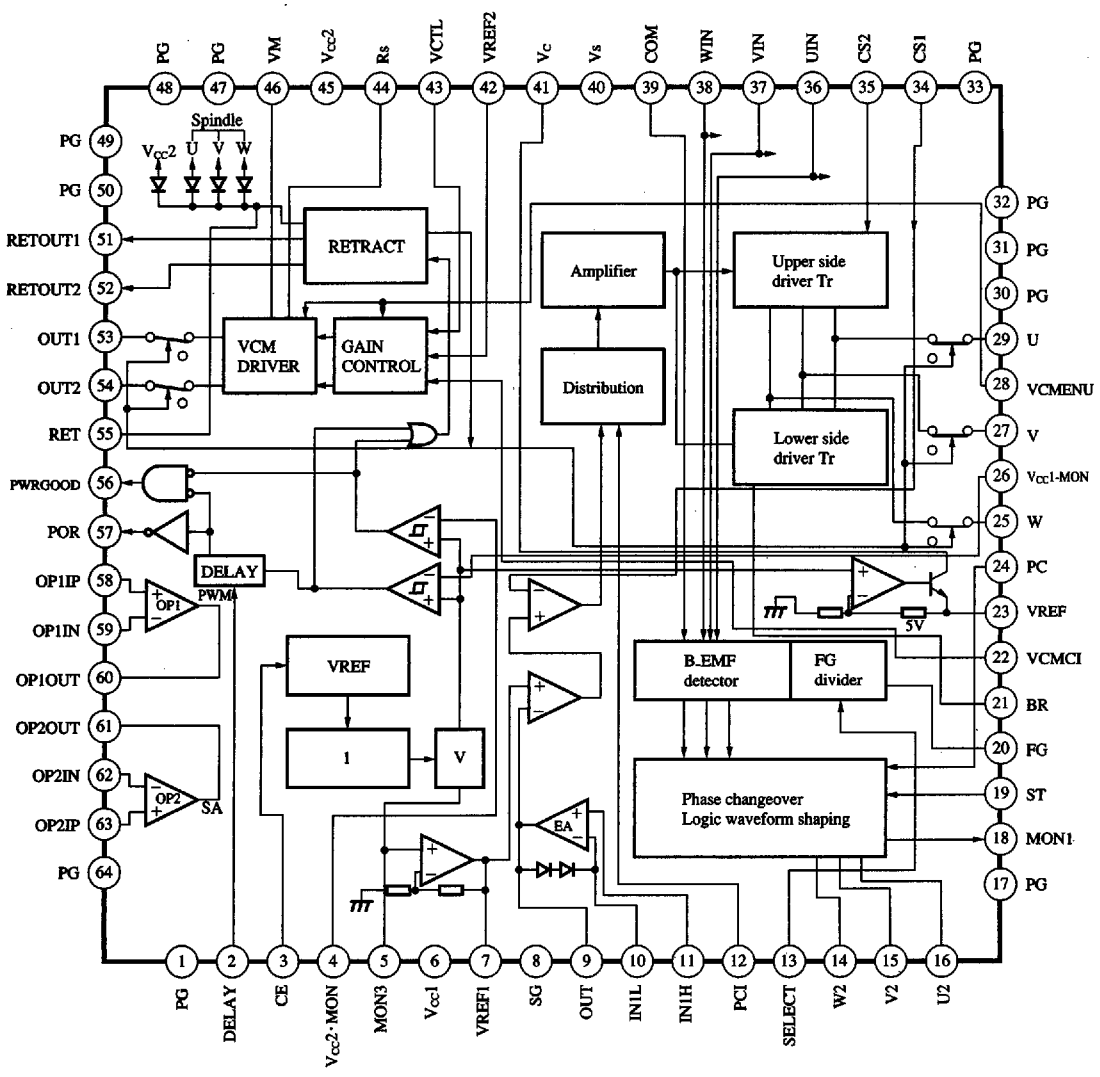
48-pin QFP Package (QFH064-P-1414)

■ Features

- Wide operating supply voltage range : The 5V and 12V systems supported
- Start circuit supported by the external clock input of spindle
- Spindle sensor-less function built-in
- Spindle snubber capacitor-less type supported
- Small VCM cross-over distortion
- Reduced voltage detection circuit built-in
- Auto-retraction current adjustable by external resistor

ICs for Motor

Block Diagram



■ Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC1}	6.0	V
Supply current	I_{CC}	———	mA
Supply voltage 2	V_{CC2}	15	V
Spindle motor supply voltage	V_S	15	V
Spindle motor output voltage	V_{OSPD}	15	V
Spindle motor peak output current	I_{opeak1}	1.5	A
Spindle motor max. output current	I_{omax1}	1.0	A
Voice coil motor output voltage	V_{OVCM}	15	V
Voice coil motor peak output current	I_{opeak2}	0.8	A
Voice coil motor max. output current	I_{omax2}	0.7	A
Retraction max. output current	I_{omax}	0.1	A
5V VREF max. output current	I_{omax}	50	mA
Interface input voltage	V_{I1}	−0.3 to V_{CC1}+0.3	V
V_{CC1} to MON, V_{CC2} to MON input voltage	V_{I2}	−0.3 to V_{CC1}+0.3	V
Power dissipation	P_D	———	mW
Operating ambient temperature	T_{opr}	−30 to +85	℃
Storage temperature	T_{stg}	−55 to +150	℃

■ Recommended Operating Range (Ta=25℃)

Parameter	Symbol	Range
Operating supply voltage 1	V_{CC1}	4.5V to 5.5V
Operating supply voltage 2	V_{CC2}	10.2V to 13.8V
SPD operating supply voltage	V_S	4.5V to V_{CC2}

■ Electrical Characteristics (V_{CC1}=5V, V_{CC2}=12V, V_S=12V, Ta=25±2℃)

Parameter	Symbol	Condition	min	typ	max	Unit
Sleep Mode						
I_{CC1} supply current	I_{sleep1}	$V_{CE}=V_{CC1}-0.8V$	—	—	0.8	mA
I_{CC2} supply current	I_{sleep2}	$V_{CE}=V_{CC1}-0.8V$ $I_{CC2}=I_{VCC2}+I_{VS}$	—	—	0.8	mA
Enable Mode						
I_{CC1} supply current	I_{stup1}	V_{CE}=0.8V V_{VCMENB}=2V	—	10	19	mA
I_{CC2} supply current	I_{stup2}	V_{CE}=0.8V V_{VCMENB}=2V	—	5	10	mA
I_{CC1} supply current	I_{stup3}	V_{CE}=0.8V V_{VCMENB}=0.8V	—	10	20	mA
I_{CC2} supply current	I_{stup4}	V_{CE}=0.8V V_{VCMENB}=0.8V	—	9	17	mA

■ Electrical Characteristics (cont.) (V_{CC1}=5V, V_{CC2}=12V, V_S=12V, Ta=25±2℃)

Parameter	Symbol	Condition	min	typ	max	Unit
SP-D Block						
B-EMF Detection System						
Common-mode input voltage range	V_{cmB}		0.4	—	V_{CC} −1.2	V
COM input bias current	I_{cont}	$U_{IN}=V_{IN}=W_{IN}$=2V V_{COM}=1.5V	−4	−0.6	4	μA
Detection sensitivity level	V_{DSL}		−20	1	20	mV
B-EMF detection resistance 1	Z_{R1}		10	20	30	kΩ
B-EMF detection R2	Z_{R2}		2.9	5.8	8.7	kΩ
B-EMF detection switching threshold voltage (High)	V_{MONIH}		1.12	1.4	1.68	V
B-EMF detection switching threshold voltage (Low)	V_{MONIH}		0.6	0.75	0.9	V
Logic Block						
U2, V2, W2 Terminal						
Logic check A	I_{APC}	ST=High=2.0V CLK Input to PC Terminal	8.5	12.0	15.7	μA
Logic check A	I_{BPC}	ST=High=2.0V CLK Input to PC Terminal	−13.5	−11.0	−7.5	μA
Logic check A	I_{ZPC}	ST=High=2.0V CLK Input to PC Terminal	−0.8	—	0.8	μA
Logic check B	I_{AD}	ST=Low=0.8V UIN, VIN, WIN Input	8.5	12.0	15.7	μA
Logic check B	I_{BD}	ST=Low=0.8V UIN, VIN, WIN Input	−13.5	−11.0	−7.5	μA
Logic check B	I_{ZD}	ST=Low=0.8V UIN, VIN, WIN Input	−0.8	—	0.8	μA
Sink/source/delta current	ΔI	$\Delta I=I_{BDSI}+I_{BDSO}$	0.2	—	3.5	μA
Sink current U2, V2, W2 relative error	ΔI_{SI}		−2.0	—	2.0	μA
Source current U2, V2, W2 relative error	ΔI_{SO}		−2.0.	—	2.0	μA
EA Block						
Open loop gain	A_{EAG}	f=1KHz	40	55	—	dB
Input bias current	I_{EAB}		−100	20	100	nA
V_{REF1} reference voltage	V_{REF1}		2.3	2.5	2.7	V
V_{REF1} output impedance	Z_{VREF1}	I_{out}=±1mA	—	—	40	Ω

■ Electrical Characteristics (cont.) (V_{CC1}=5V, V_{CC2}=12V, V_S=12V, Ta=25±2℃)

Parameter	Symbol	Condition	min	typ	max	Unit
Drive Output System						
Output saturation voltage (V_{SAT} Upper)	V_{SAT1}	I_{OUT}=−0.1A V_{CC2}=V_S=V_{CS}	—	0.9	—	V
Output saturation voltage (V_{SAT} Upper)	V_{SAT2}	I_{OUT}=−1A V_{CC2}=V_S=V_{CS}	—	1.1	—	V
Output saturation voltage (V_{SAT} Upper)	V_{SAT3}	I_{OUT}=−0.1A (V_S+V_{CS}) <V_{CC2}−1V	—	0.05	—	V
Output saturation voltage (V_{SAT} Upper)	V_{SAT4}	I_{OUT}=−1A (V_S+V_{CS}) <V_{CC2}−1V	—	0.47	—	V
Output saturation voltage (V_{SAT} Lower)	V_{SAT5}	I_{OUT}=0.1A	—	0.05	—	V
Output saturation voltage (V_{SAT} Lower)	V_{SAT6}	I_{OUT}=1A	—	0.38	—	V
Total output saturation voltage 1	V_{TOL1}	V_{TOL1}=V_{SAT1}+V_{SAT5}	—	0.95	1.1	V
Total output saturation voltage 2	V_{TOL2}	V_{TOL2}=V_{SAT2}+V_{SAT6}	—	1.48	2.0	V
Output leak current	I_{Leak}	PCI=0V	—	—	1.0	mA
Drive gain	G_D	R_{CS}=1Ω	0.03	0.37	0.41	V/V
Current limiter voltage	V_{CL}	R_{CS}=1Ω	0.24	0.27	0.3	V
Drive output lower fixed voltage	V_O	R_{CS}=1Ω V_{CS}=0.1V	—	0.2	1	V
Power-On Time Short Brake Block						
Saturation voltage (V_{SAT} Lower)	V_{BSAT}	I_{OUT}=100mA	—	0.05	0.5	V
Interface Input Block						
CE Terminal						
Input high voltage	V_{HCE}		V_{CC1} −0.8	—	V_{CC1}	V
Input low voltage	V_{LCE}		0	—	—	V
Input high current	I_{HCE}	V_{CE}=4.2V	−15	−4	0.8	μA
Input low current	I_{LCE}	V_{CE}=4.2V	−500	−180	—	μA
VCMENB, VCMCH, BRST, SELECT, PC Terminals						
Input high voltage	V_{HI}		2	—	V_{CC1}	V
Input low voltage	V_{LI}		0	—	0.8	V
Input high current	I_{HI}	V_I=2V	−2	—	2	μA
Input low current	I_{LI}	V_I=2V	−2	—	2	μA
Interface Output Block						
FG, POR, PWRGOOD						
Output high voltage	V_{HO}	I_S=−0.5mA	3.0	4.32	—	V
Output low voltage	V_{LO}	I_S=−0.5mA	—	0.048	0.5	V
Monitor Block						
MON3 reference voltage	V_{MON3}		1.180	1.245	1.304	V
Monitor Block : V_{CD}-MON						
Threshold voltage 1	$V_{Th1\ High}$		1.180	1.245	1.304	V
Hysteresis voltage 1	V_{hys1}		40	—	65	mV
Monitor Block : V_{CC2}-MON						
Threshold voltage 2	$V_{Th2\ High}$		1.180	1.245	1.304	V
Hysteresis voltage 2	V_{hys2}		40	—	65	mV

ICs for Motor

■ Electrical Characteristics (cont.) (V_{CC1}=5V, V_{CC2}=12V, V_S=12V, Ta=25±2℃)

Parameter	Symbol	Condition	min	typ	max	Unit
Monitor Block : Delay						
POR delay output time	T_{DELAY}	C=0.1 μF	20	—	80	mS
POR delay output current	I_{DPOR}	V_{CC1}-MON=1.5V V_{POR}=0.7V	1.2	—	3.8	μA
Retraction Block						
RET saturation voltage 1	$V_{RETSAT1}$	V_{CC1}-MON=1V R_{ETOUT2} : I_{RET}=50mA	—	0.24	0.5	V
RET saturation voltage 2	$V_{RETSAT2}$	V_{CC1}-MON=1V RET~R_{ETOUT1} : I_{RET}=50mA	—	0.93	1.5	V
RET voltage	V_{RET}	V_{CC1}-MON=1V V_{CC2}~R_{ETOUT1} : I_{RET}=50mA	—	0.99	1.5	V
Reference Voltage Block						
5VV_{REF} reference voltage	V_{5VVREF}		4.6	5	5.4	V
5VV_{REF} output impedance	Z_{5VVREF}	I_{OUT}=−25mA	—	—	20	Ω
VCM Block						
V_{CTL}, V_{REF2}			−5	—	5	μA
Input bias current	I_B		1.0	—	V_{CC2} −2	V
Common-mode input voltage range	V_{SD}		—	—	—	—
Drive Output System						
V/I transmission gain 1	gm1	V_{VCMCH}=2V R_S=1.0Ω	0.9	1.0	1.1	A/V
V/I transmission gain 2	gm2	V_{VCMCH}=0.8V R_S=1.0Ω	0.025	0.25	0.275	A/V
Input conversion offset voltage 1	Vofs1	V_{VCMCH}=2V, R_L=10.5Ω R_S=1.0Ω V_{CTL}=V_{ref2}=5.7V	−200	—	200	mV
Input conversion offset voltage 2	Vofs2	V_{VCMCH}=2V, R_L=10.5Ω R_S=1.0Ω V_{CTL}=V_{ref2}=5.7V	−200	—	200	mV
No-signal time output voltage	V_{oq}		5.45	5.8	6.15	V
Drive Output System						
Output saturation voltage (V_{SAT} Upper)	V_{SAT1}	I_{OUT}=200mA	—	0.85	—	V
Output saturation voltage (V_{SAT} Upper)	V_{SAT2}	I_{OUT}=700mA	—	1.2	—	V
Output saturation voltage (V_{SAT} Upper)	V_{SAT3}	I_{OUT}=200mA V_M<V_{CC2}−1V	—	0.15	—	V
Output saturation voltage (V_{SAT} Upper)	V_{SAT4}	I_{OUT}=700mA V_M<V_{CC2}−1V	—	0.5	—	V
Output saturation voltage (V_{SAT} Upper)	V_{SAT5}	I_{OUT}=200mA	—	0.25	—	V
Output saturation voltage (V_{SAT} Upper)	V_{SAT6}	I_{OUT}=700mA	—	0.5	—	V
Total output saturation voltage	V_{SAT7}	I_{OUT}=200mA V_{SAT7}=V_{SAT1}+V_{SAT5}	—	1.1	1.5	V
Total output saturation voltage	V_{SAT8}	I_{OUT}=700mA V_{SAT8}=V_{SAT2}+V_{SAT6}	—	1.7	2.3	V
Output bias current	I_M		—	4	10	mA

■ Electrical Characteristics (cont.) (V_{CC1}=5V, V_{CC2}=12V, V_S=12V, Ta=25±2℃)

Parameter	Symbol	Condition	min	typ	max	Unit
OP1, OP2						
Input bias current	I_{inop}		−100	—	100	nA
Input offset voltage	V_{osop}		−10	—	10	mV
Common-mode input voltage range	V_{cmop}		0	—	V_{CC2} −1.8	V
Open loop gain	Gop	f=1KHz	40	55	—	dB
Gain band width	Bop	Gop=0dB	100	500	—	kHz
Output high voltage	Vohop	Iout=−1mA	V_{CC2} −2	—	—	V
OP1 output low voltage	V_{olop1}	Iout=1mA	—	—	1.1	V
OP2 output low voltage	V_{olop2}	Iout=1mA	—	0.1	0.3	V

■ Electrical Characteristics (Design Reference Values) (Ta=25±2℃)

The following values are design reference values but not guaranteed ones.

Parameter	Symbol	Condition	Reference value	Unit
SPD Block				
EA Block				
Gain/Band width product	f_{GB}		1.0	MHz
Thermal Protection Circuit				
Thermal protection operation temperature	T_P		150	℃
Hysteresis temperature	T_H		25	℃
VCM Block				
Output gain band width 1	B_1	V_{VCMCH}=2.0V, gm=−3dB R_S=2Ω	68	KHz
Output gain band width 2	B_2	V_{VCMCH}=0.8V, gm=−3dB R_S=2Ω	73	KHz
Output distortion ratio 1	D_1	I_{OUT}=0.1Arms, R_L=10.5Ω V_{VCMCH}=2.0V, R_S=2Ω f=500Hz	0.5	%
Output distortion ratio 2	D_2	I_{OUT}=0.1Arms, R_L=10.5Ω V_{VCMCH}=0.8V, R_S=2Ω f=500Hz	0.5	%

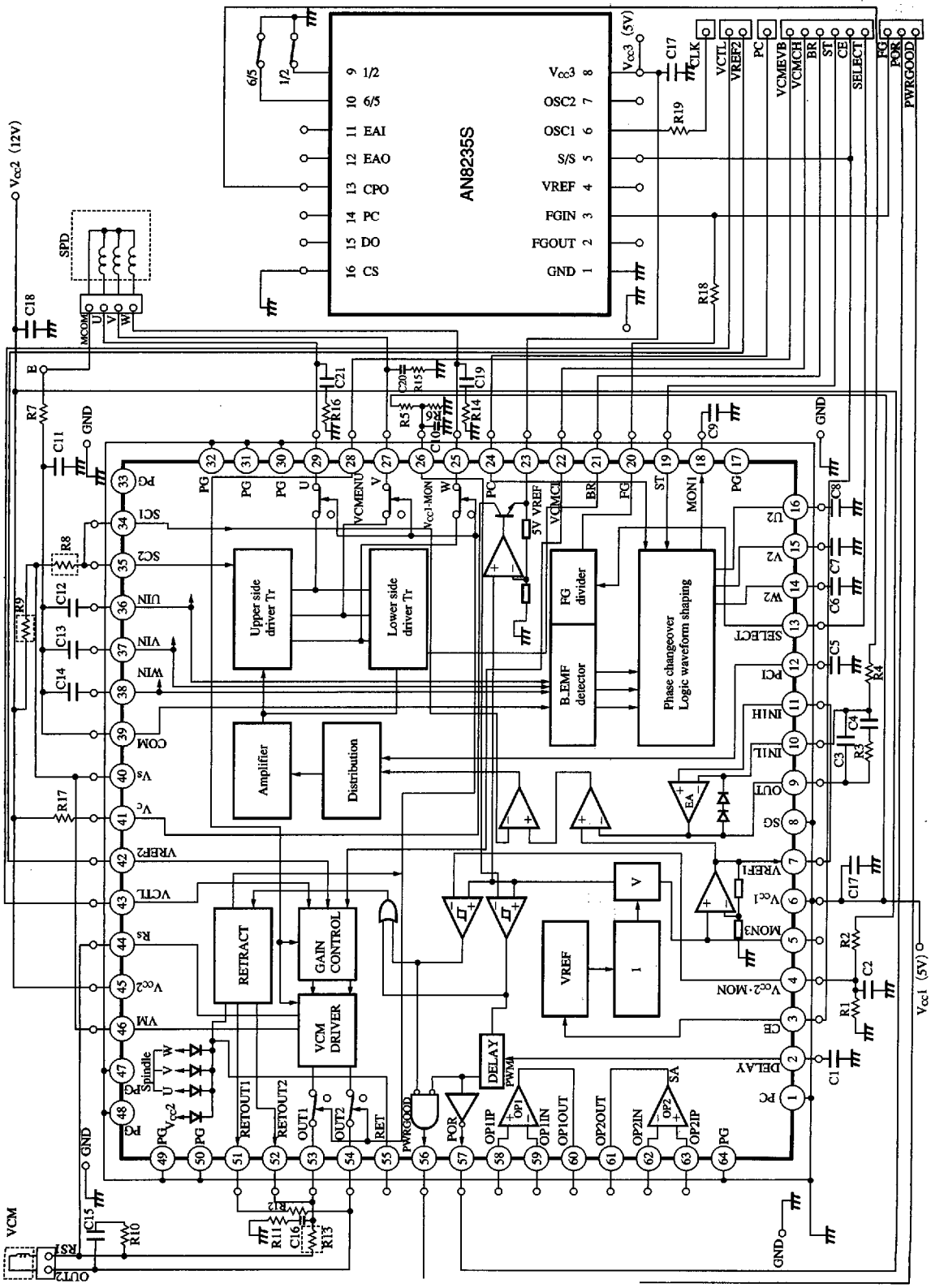
■ Pin Function Descriptions

Pin No.	Pin name	Terminal description	Function
1	PG	Power ground	Ground terminal for power block
2	DELAY	Delay setting terminal	Displays the "High" of PWRFGOOD output and POR output.
3	CE	Chip enabling terminal	"Low" input for enabling the IC operation and "High" input for stopping the circuit operation
4	V_{CC2}−MON	V_{CC2} monitor terminal	Monitors the voltage which is resistance-divided from the supply voltage of V_{CC2}.
5	MON3	Monitor terminal 3	Outputs the reference voltage of the V_{CC1} and V_{CC2} power supply monitor circuit.
6	V_{CC1}	Power supply terminal 1	Connects the 5V system power supply with power supply input of control block.
7	V_{REF1}	Reference voltage input terminal 1 (SPD)	Outputs the reference voltage of speed control block. The reference voltage output is $1/2V_{CC1}$.
8	SG	Signal ground	Ground terminal for signal block
9	OUT	Error amp. 1 output terminal	Output making the speed control
10	IN1L	Error amp. 1 reverse-phase input terminal	Inputs the speed control signal.
11	IN1H	Error amp. 1 normal-phase input terminal	Inputs the speed control signal.
12	PCI	Current feedback system phase compensation terminal	Compensates the phase for loop of the current feedback system.
13	SELECT	FG output switching terminal	Switching terminal for FG output. "LOW" input for FG output 1 and "High" input for FG output 1/4
14	W2	Trapezoidal wave shaping terminal (3)	U2, V2 and W2 generate the slope wave for synthesizing the trapezoidal wave.
15	V2	Trapezoidal wave shaping terminal (2)	U2, V2 and W2 generate the slope wave for synthesizing the trapezoidal wave.
16	U2	Trapezoidal wave shaping terminal (1)	U2, V2 and W2 generate the slope wave for synthesizing the trapezoidal wave.
17	PG	Power ground	Ground terminal for power block
18	MON1	Monitor terminal 1	Monitors the trapezoidal wave maximum voltage.
19	ST	SPD start terminal	"High" for ST synchronous operation mode. High→Low for start of SPD
20	FG	FG output terminal	FG-outputs.
21	BR	Short brake terminal	"High" at power-on to work the short brake for SPD.
22	VCMCH	Gain switching input terminal	Can switch the VCM gain between 1 and 1/2. "High" input for VCM gain to 1 "Low" input for VCM gain to 1/2
23	5V V_{REF}	5V V_{REF} terminal	Terminal outputting the reference voltage of 5V
24	PC	External clock input terminal	Input terminal for external clock when the SPD is used in synchronous operation mode
25	W	W-phase drive output terminal	Drives the W-phase of SPD.
26	V_{CC1}−MON	V_{CC1} monitor terminal	Monitors the voltage which is resistance-divided from the supply voltage of V_{CC1}.
27	V	V-phase drive output terminal	Drives the V-phase of SPD.
28	VCMENB	VCM enabling terminal	"Low" input to enable the VCM operation and "High" input to stop the VCM circuit operation
29	U	U-phase drive output terminal	Drives the U-Phase of SPD.
30~33	PG	Power ground	Ground terminal for power block
34	CS1	Drive current detection terminal 1	Detects the current flowing in the motor to limit the max. current.
35	CS2	Drive current detection terminal 2	Detects the current flowing in the motor to limit the max. current.
36	UIN	U-phase B_EMF detection terminal	Receives the B_EMF input of U-phase.
37	VIN	V-phase B_EMF detection terminal	Receives the B_EMF input of V-phase.
38	WIN	W-phase B_EMF detection terminal	Receives the B_EMF input of W-phase.
39	COM	Neutral point input terminal	Inputs the neutral point voltage of spindle motor.
40	VS	Motor drive power supply terminal (SPD)	When V_{CC2} is sufficiently high voltage, the surplus voltage is applied to V_{CE} of the source side output transistor.

■ Pin Function Descriptions (cont.)

Pin No.	Pin name	Terminal description	Function
41	V_C	$5VV_{REF}$ power supply terminal	Power supply terminal to make up the reference voltage of $5VV_{REF}$.
42	V_{REF2}	Reference voltage input terminal 2 (VCM)	Inputs the reference voltage.
43	V_{CTL}	Control input terminal	Inputs the control voltage.
44	R_S	Current detection terminal	Detects the current flowing in the VCM.
45	V_{CC2}	Power supply terminal 2	Connected to the 12V system power supply through the power supply input of power block (VCM).
46	V_M	Motor drive power supply terminal (VCM)	VM terminal for VCM
47~50	PG	Power ground	Ground terminal for the power block
51	RETOUT1	Retraction output terminal 1	Retraction output
52	RETOUT2	Retraction output terminal 2	Retraction output
53	OUT1	Amp. output terminal 1	Connects the current detection resistor between OUT1 and RS.
54	OUT2	Amp. output terminal 2	Connects the load coil between OUT2 and RS.
55	RET	Retraction monitor voltage terminal	Monitors the retraction voltage.
56	PWRGOOD	Power supply monitor output terminal 1	"High" output indicates that both of the supply voltages V_{CC1} and V_{CC2} reach the operation-able voltage.
57	POR	Power supply monitor output terminal 2	"High" output indicates that the supply voltage V_{CC1} reaches the operation-able voltage.
58	OP1IP	Operational amp. 1 normal-phase input terminal	Normal-phase input terminal for operational amp.
59	OP1IN	Operational amp. 1 reverse-phase input terminal	Reverse-phase input terminal for operational amp.
60	OP1OUT	Operational amp. 1 output terminal	Output terminal for operational amp.
61	OP2OUT	Operational amp. 2 output terminal	Output terminal for operational amp.
62	OP2IN	Operational amp. 2 reverse-phase input terminal	Reverse-phase input terminal for operational amp.
63	OP2IP	Operational amp. 1 normal-phase input terminal	Normal-phase input terminal for operational amp.
64	PG	Power ground	Ground terminal for power block

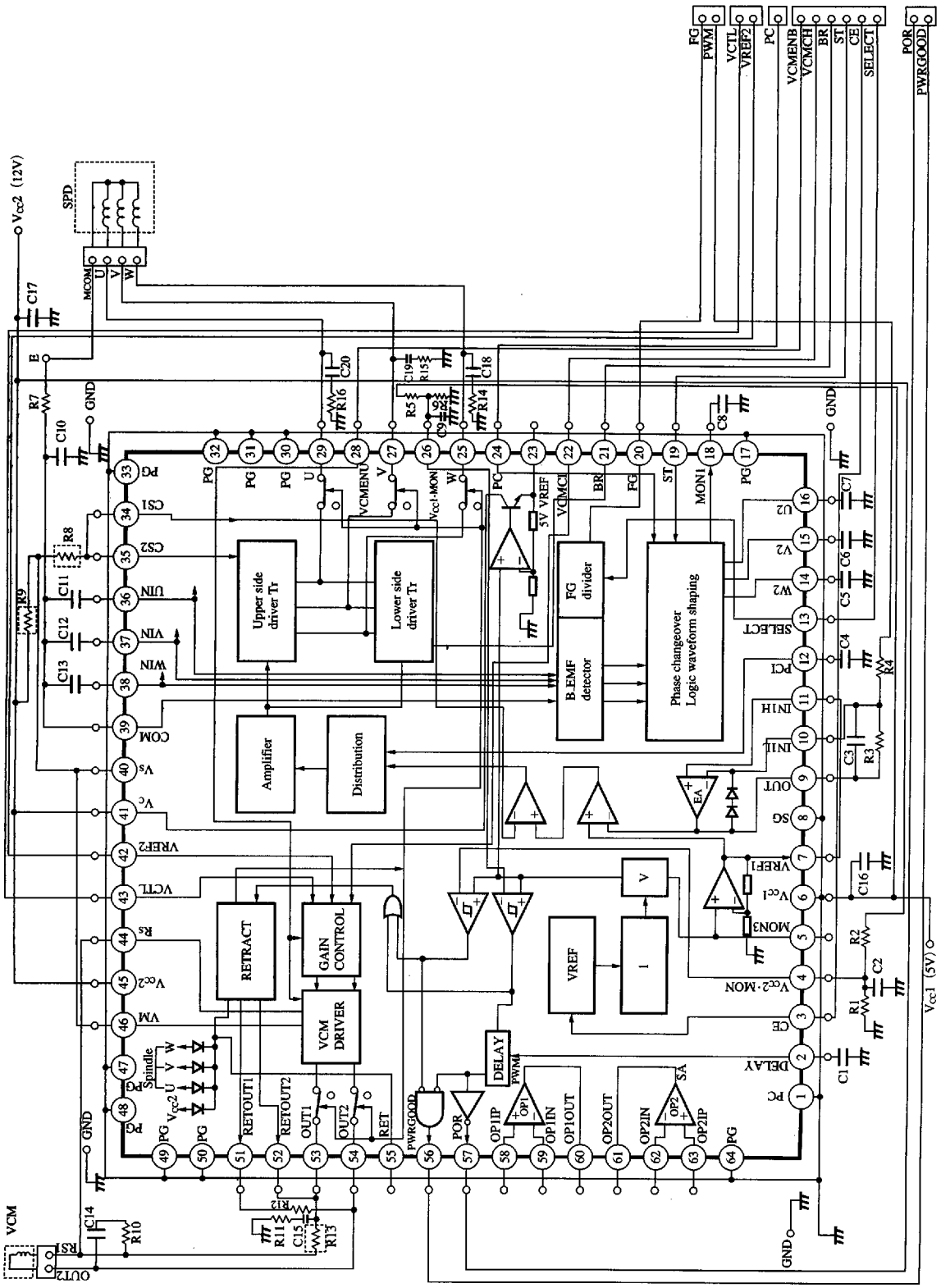
■ Board for Evaluation (1)



External Parts

Pin No.	Purpose	Recommended value
R1 R2	For LVD	R1=12kΩ R2=68kΩ
R3 R4	For speed control	—
R5 R6	For LVD	R5=12kΩ R6=4.7kΩ
R7	SPD common filter	330Ω
R8	SPD current sensing	— (0.27Ω)
R9	For power dissipation	— (0.33Ω)
R10 R11	For stability	R10=51Ω R11=10Ω
R12	Set retract current	— (20Ω)
R13	VCM current sensing	— (1.0Ω)
R14 R15 R16	For stability	— (22Ω)
R17	For power dissipation	— (120Ω) at25mA
R18 R19	Protection resister	10kΩ
C1	For POR delay	— (0.1μF)
C2	Filter	0.043μF
C3 C4	For speed control	—
C5	Control amp phase compensation	0.22μF
C6 C7 C8	Trapezoidal waveform shaping	— (0.022μF)
C9	Filter	0.001μF
C10	Filter	0.043μF
C11	SPD common filter	0.22μF
C12 C13 C14	B_EMF filter	— (0.033μF)
C15 C16	For stability	0.22μF
C17 C18	Power supply by-passing	≧1.0μF
C19 C20 C21	For stability	— (0.22μF)
C22	Power supply by-passing	— (0.001μF)

■ Board for Evaluation (2)



External Parts

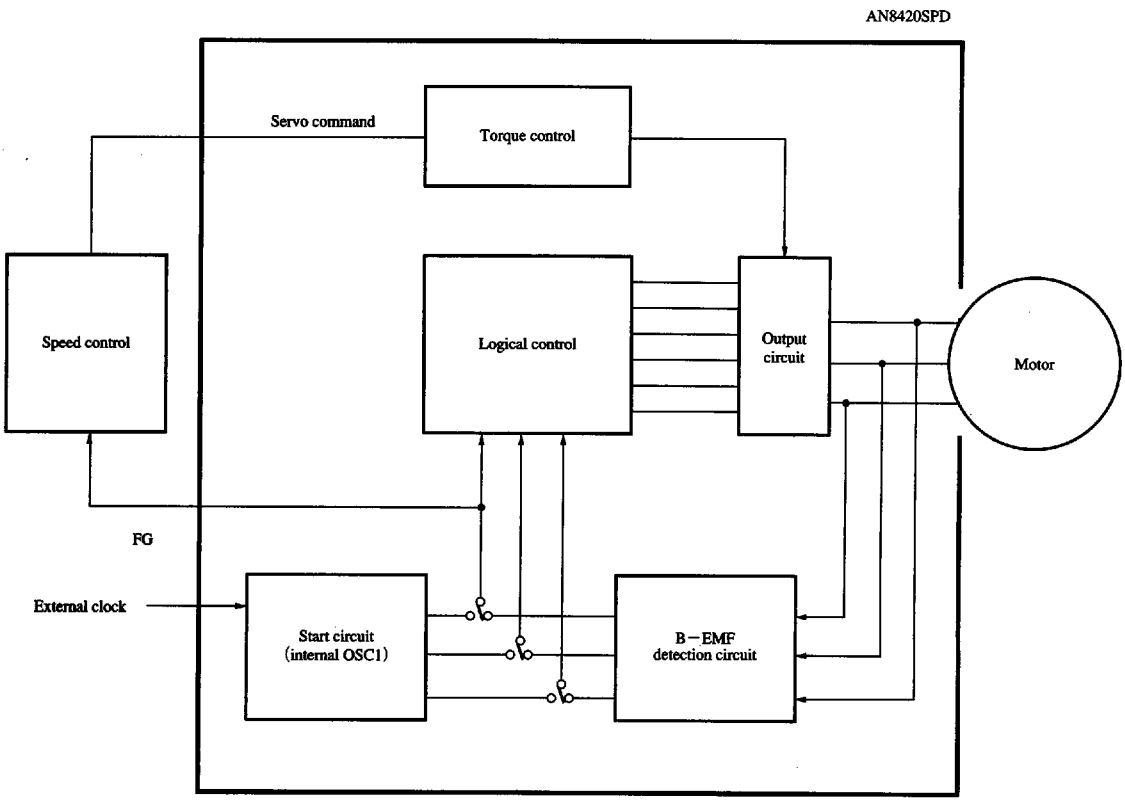
Pin No.	Purpose	Recommended value
R1 R2	For LVD	R1=12kΩ R2=68kΩ
R3 R4	For PWM	—
R5 R6	For LVD	R5=12kΩ R6=4.7kΩ
R7	SPD common filter	330Ω
R8	SPD current sensing	— (0.27Ω)
R9	For power dissipation	— (0.33Ω)
R10 R11	For stability	R10=51Ω R11=10Ω
R12	Set retract current	— (20Ω)
R13	VCM current sensing	— (1.0Ω)
R14 R15 R16	For stability	— (22Ω)
C1	For POR delay	— (0.1μF)
C2	Filter	0.043μF
C3	For PWM	—
C4	Control amp phase compensation	0.22μF
C5 C6 C7	Trapezoidal waveform shaping	— (0.022μF)
C8	Filter	0.01μF
C9	Filter	0.043μF
C10	SPD common filter	0.22μF
C11 C12 C13	B_EMF filter	— (0.033μF)
C14 C15	For stability	0.22μF
C16 C17	Power supply by-passing	≧0.1μF
C18 C19 C20	For stability	— (0.22μF)

■ Sensor-less Drive Block Application

1. Drive Principle for sensor-less IC (AN8420)

The drive circuit of the sensor-less motor detects the B−EMF which is generated in the motor coil and operates the circuit by using it as the rotor position signal.

The AN8420 consists of the three-phase full-wave drive circuit.

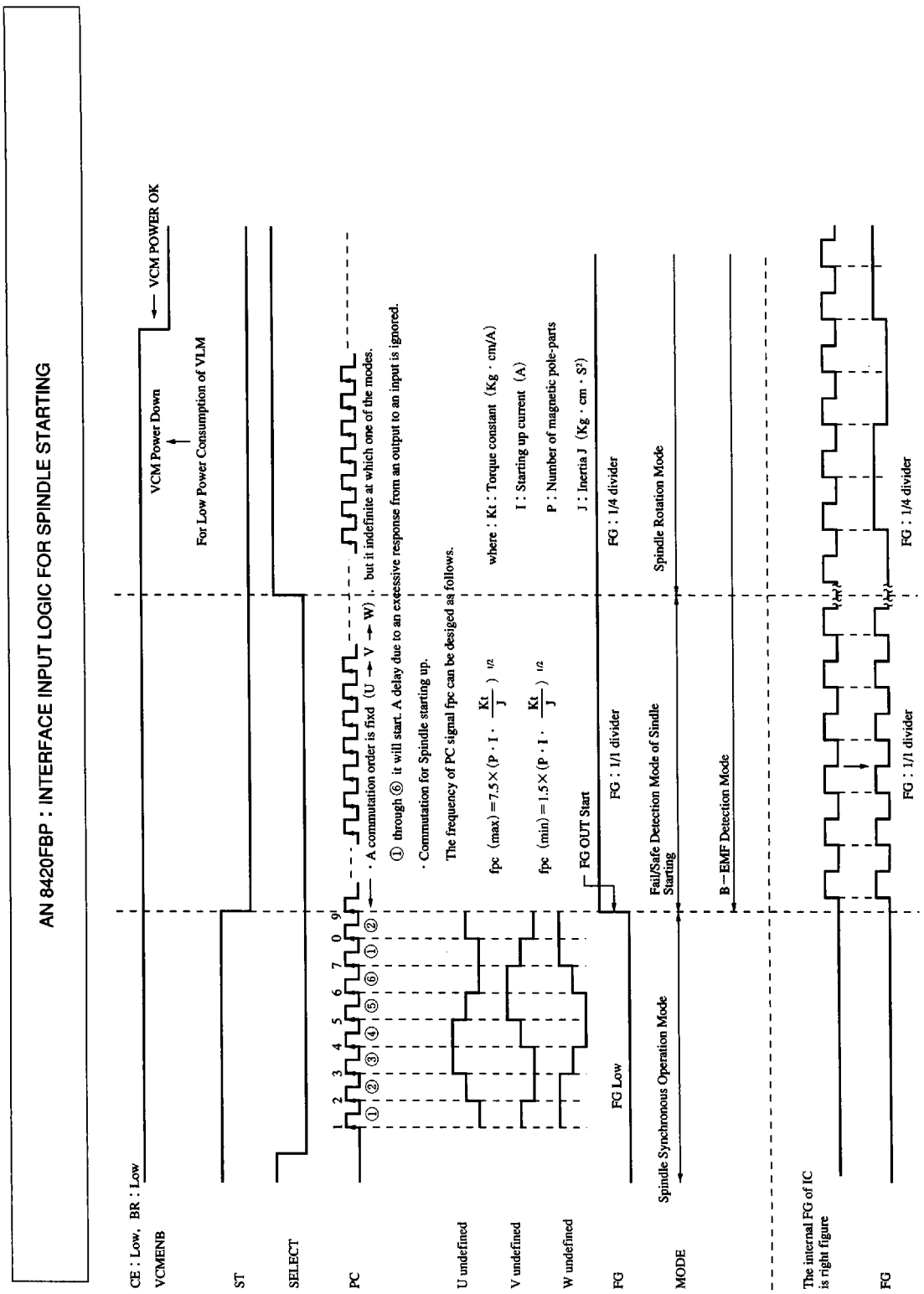


In order to start driving the sensor-less spindle motor for fixed commutation number, it excites the coil by force, timing with the internal OSC in the start circuit. This is called start mode.

In the start mode, the excitation is started in the fixed sequence, independent on the position of stator and rotor magnets. It may move slightly to reverse direction in some position, however, it should follow the normal direction sequence in view of the circuit. In the start mode, electromotive force (B−EMF) is generated in the coil. The detection circuit detects this electromagnetic force (B− EMF) and the logical control receives input of that force to start the output circuit. This is called the detection mode.

Adsorption of head on disk which requires large start torque of the motor can be reduced through harmonics excitation of the coil by the external clock.

AN 8420FBP : INTERFACE INPUT LOGIC FOR SPINDLE STARTING



• **Setting the commutation frequency in SPD start mode**

(1) OSC1 (Triangular wave oscillation terminal)

OSC1 is an oscillation terminal which sets the commutation frequency at operation start.

The commutation frequency at operation start is expressed by the following formula :

$$femf = \frac{fosc1}{48} = \frac{1}{48} \times \frac{5}{8} \times \frac{1}{C} \times \frac{1}{V_{TE}} \times I_{CH} \times K$$

where :

femf : Commutation frequency

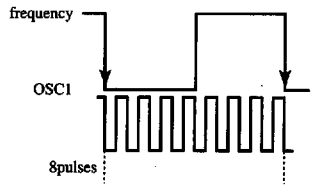
foscl : triangularwave oscillation

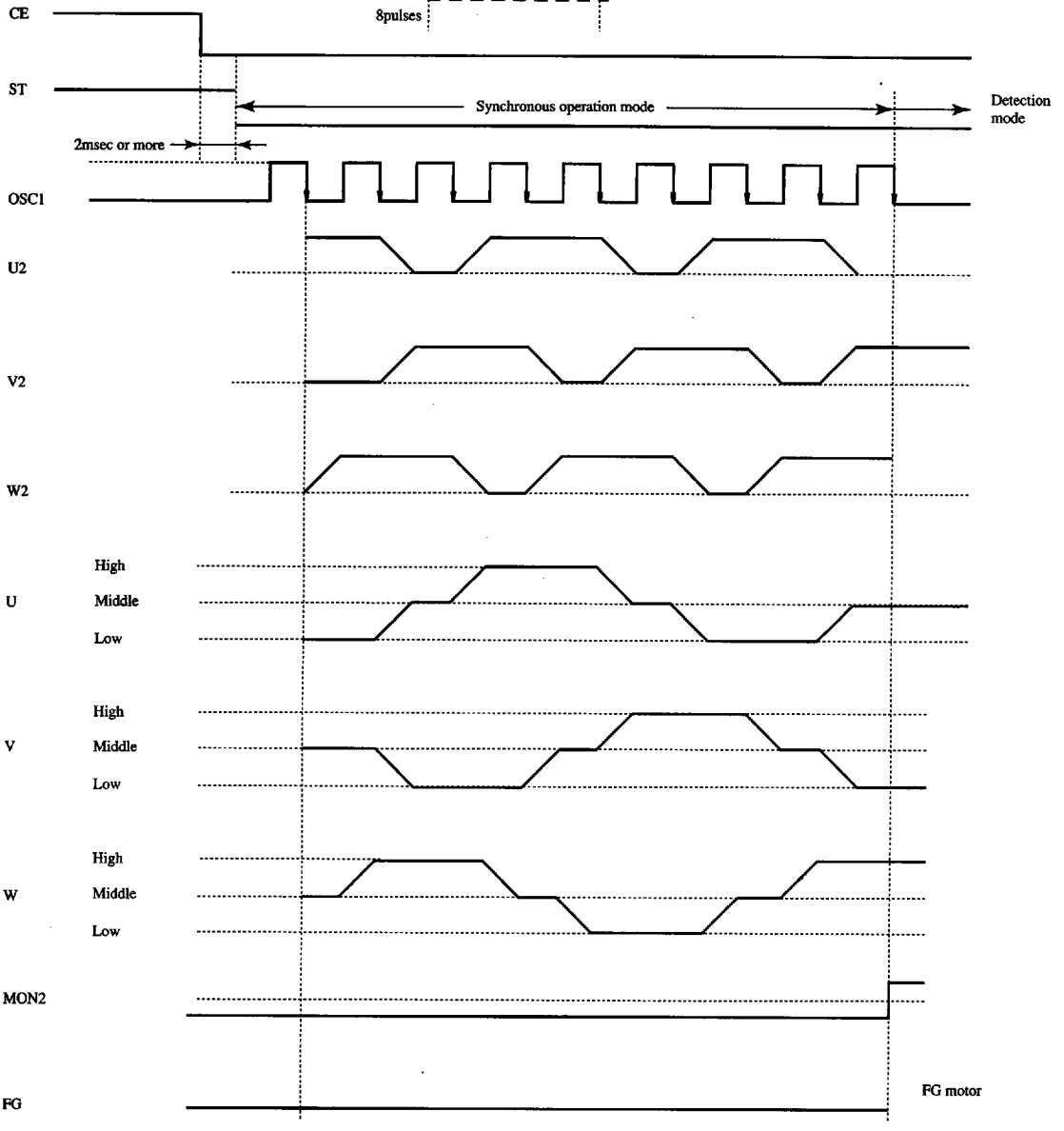
C : External capacitance

V_{TE} : Reference voltage inside IC (approx. 2.5V)

I_{CH} : Reference voltage inside IC (approx. 20 μA)

K : Dispersion factor





• **Filter for B−EMF detection and noise rejection**

(2) UIN, VIN and WIN (U-, V- and W-phase B−EMF detection terminals)

- In order to reject the noise such as of electromotive force which is generated from the motor, the capacitor for filter is connected.
- When the constant of the capacitor for filter is set too large, the optimum energization timing during the rated rotation of spindle motor is missed, and the consumption current during the rated rotation of spindle motor is increased. Therefore, the constant should be set, taking into consideration the relationship with the spindle motor.

The phase deviation from the optimum energization timing during the rated rotation due to improperly set CR time constant, θ can be given in the following simple calculation :

$$\theta = C \times R \times \frac{N \times P}{60 \times 2} \times 360 \ (DEG)$$

N : Rated rotation number (rpm)
P : Motor pole number
C : Time constant of B−EMF detection filter
R : Time constant of B−EMF detection filter (built in IC)

• **Automatic switching of B−EMF detection resistor with speed increased**

Fig. 1 shows the B−EMF detection block.

The B−EMF detection terminal of U-, V- and W-phase is connected with the drive output terminal of U-, V- and W-phase through the resistor (R1 = 20kΩ, typ.).

As shown in Fig.1, the resistor (R2 = 8kΩ, typ.) is connected with R1 in parallel by the trapezoidal wave maximum output.

Fig.2 illustrates the automatic switching by the MON1 of B−EMF detection.

When the speed of spindle motor is increased, the MON1, the maximum output of trapezoidal wave of U2, V2 and W2. is decreased, corresponding to the rotation number of spindle motor.

The auto-switching function for B−EMF detection resistance is provided in order not to increase the consumption current during the rated rotation when the time constant of the B−EMF detection filter should be set large because of desired spindle motor start.

When the speed of spindle motor is increased, the voltage of MON1, the maximum value of trapezoidal wave is decreased. Then, when the maximum value of trapezoidal wave reaches 0.9 V, the resistor which is connected between the B−EMF detection terminal of U-, V- and W-phase and the drive output terminal of U-, V- and W-phase, is switched to the value : R = R1/R2 ≒ 20kΩ/8kΩ ≒ approx. 5.7kΩ.

When the B−EMF detection resistor switching function by the MON1, the maximum value of trapezoidal wave is not used, the MON1 terminal should be connected to the GND or MON3 terminal.

The COMMON filter should be used when the voltage applied to the COM terminal exceeds the input voltage range.

B—EMF Detection Block Diagram

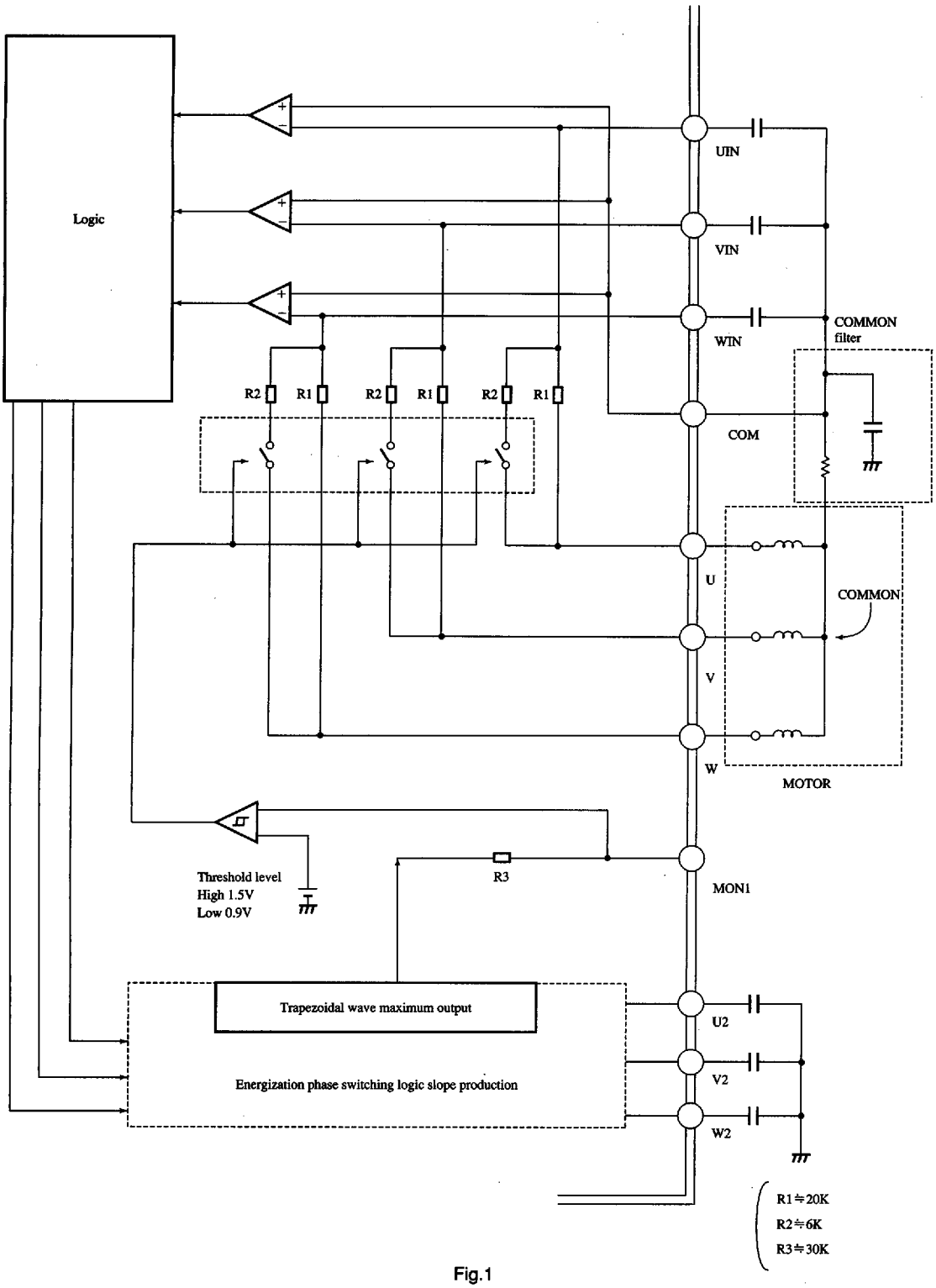


Fig.1

• **Auto-switching by MON1 of B−EMF detection**

Fig.2 illustrates the motor rotation number N and FG proportional to the motor rotation number when the speed of spindle motor is increased ; the voltage waveform of MON1, the trapezoidal wave maximum value ; and switching of resistance R built-in the IC of B−EMF detection filter.

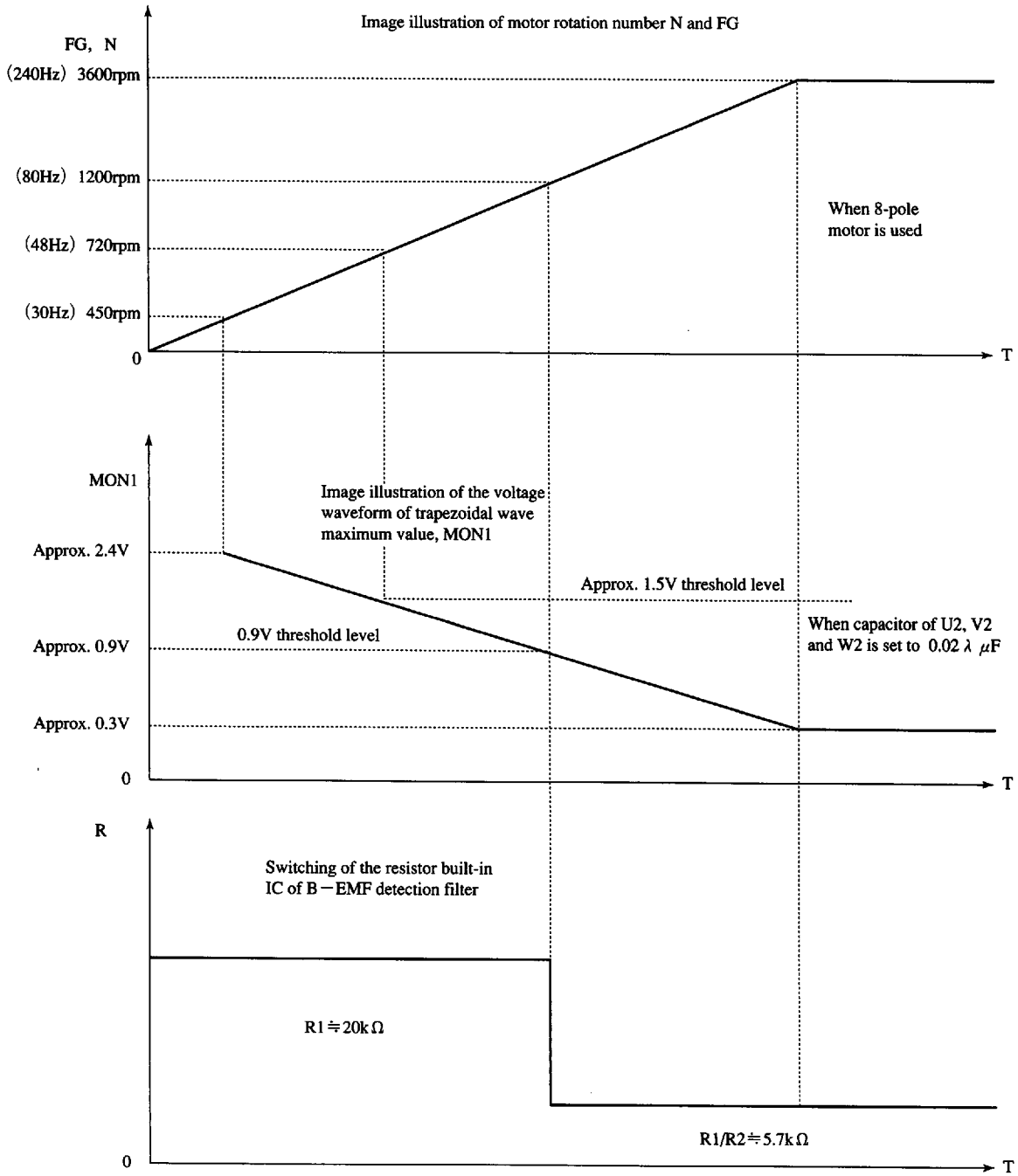


Fig.2

(3) Trapezoidal wave shaping terminal (Capacitor of U2, V2 and W2)

Its set constant is related with the number of poles of three-phase motor, as shown in the following :

Ex) When the motor with 8 poles is used :

$Q=CV=it\cdots$

- C : Capacitance value of capacitor of U2, V2 and W2
- V : DC voltage (200 to 400mV)
- i : Constant current ($10\,\mu A$)
- t : FG (three-phase pole) cycle $\times 1/6$

FG frequency under 3600 rpm of three-phase 8-pole motor :

$$FG=\frac{3600rpm}{60sec}\times\frac{8\text{-pole}}{2}$$

$$=240Hz$$

$$T=\frac{1}{240Hz}\fallingdotseq 4.17sec$$

$$t=\frac{1}{6}\times T\fallingdotseq 695\,\mu sec$$

$$Q=it=10\,\mu A\times 695\,\mu sec\fallingdotseq 6.95\times 10^{-9}\ (q)$$

Setting $V\fallingdotseq 316mV$ (DC = 200mV to 400mV),

$$C=\frac{it}{V}=\frac{6.95\times 10^{-9}}{316\times 10^{-3}}\fallingdotseq 0.022\,\mu F$$

Therefore, when it is used under the rated rotation number of 3600rpm in case of three-phase 8 poles motor, the capacitance value of capacitor of U2, V2 and W2 is $0.22\,\mu F$.

When a motor with 4, 6 or 12 poles is used, follow the above example to review the constant.

(4) Drive Amp.

The AN8420FBP is an IC of current drive type. The motor drive current I_a is determined by the voltage of OUT terminal, as shown in Fig.3.

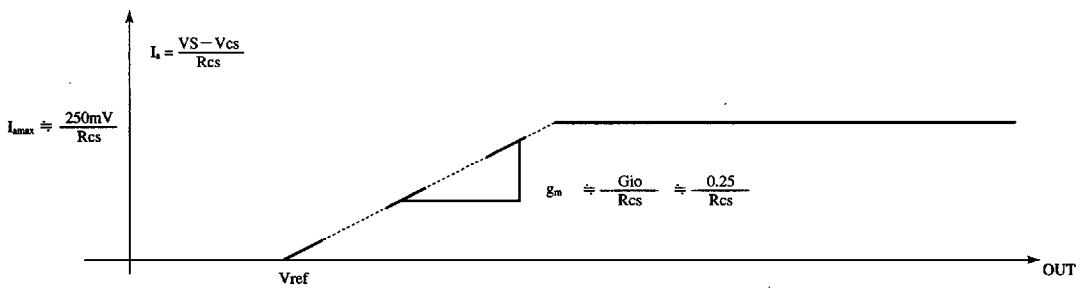
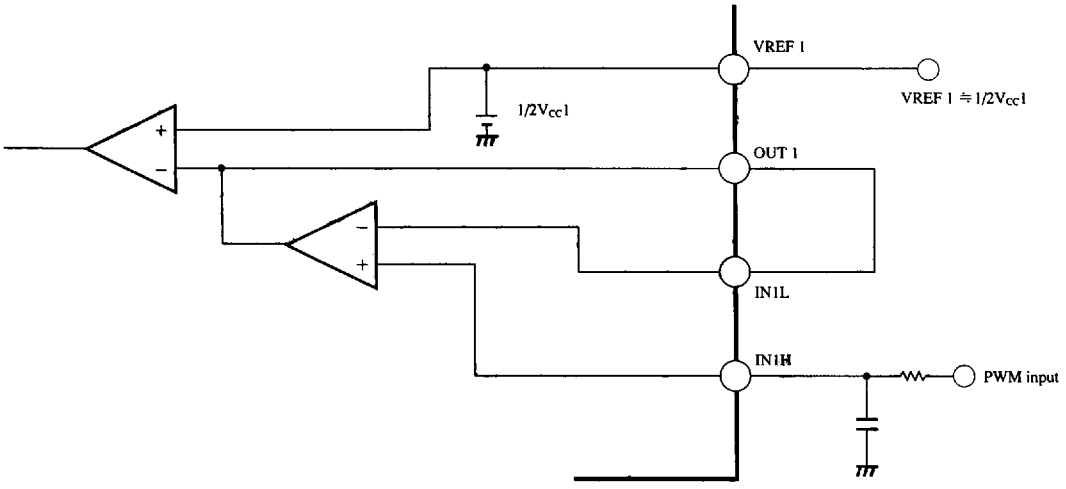


Fig.3 Drive Characteristics

(7) Servo circuit

The following shows an example of the servo circuit using the PWM input :

(Ex. 1) (In case of speed control for IN1H with DC voltage)



(Ex. 2) (In case of variable servo system gain)

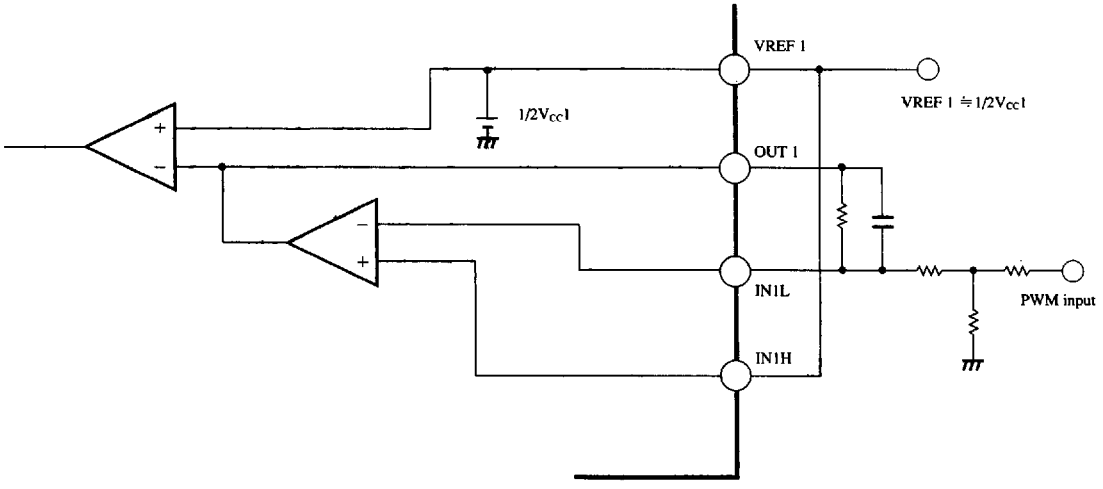


Fig.4

• VCM operation description

(8) Relationship among V_{CTL} (control voltage), $V_{REF}2$ (reference voltage) and output voltage

The following shows the relationship among V_{CTL}, $V_{REF}2$ and output voltage $V_{RS}1$:

(i) When VCMCH=High,

$V_{RS}1 = V_{CTL} - V_{REF}2$

(ii) When VCMCH=Low,

$$V_{RS}1 = \frac{V_{CTL} - V_{REF}2}{2}$$

Output current I_L flowing in the coil is :

$$I_L = \frac{V_{RS}1}{RS1}$$

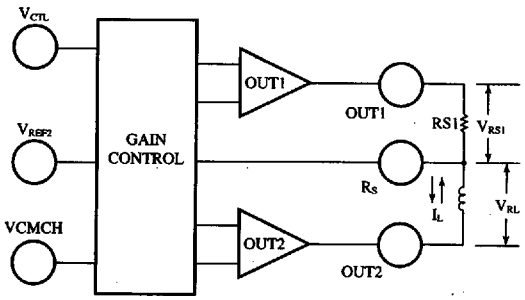


Fig.5

(9) Image illustration of the input and output DC characteristics

Fig.6 is the input and output characteristic chart, under the following condition ; V_{CC}=12V, R_S=2Ω, VCM (RL) =15Ω gm=0.5 (A/V).

The current flowing in the VCM when

$|V_{CTL} - V_{REF}| = 1.25V$: IL≒625mA

In addition, R_M resistor connected between $V_{CC}2$ and V_M terminals should be used when large load of power dissipation is applied to the package.

Refer to Fig.7.

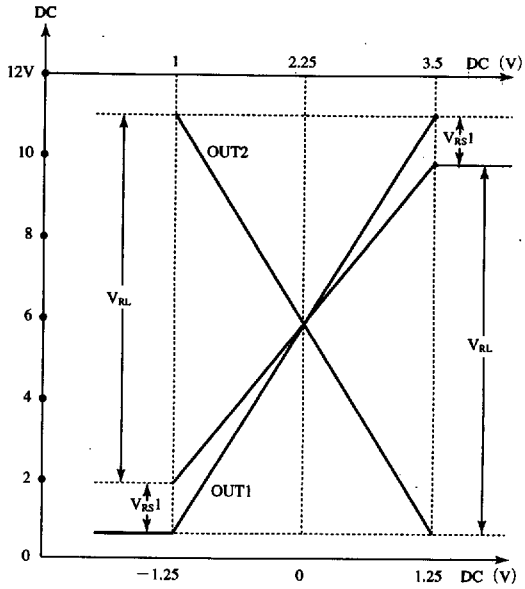


Fig.6

Diagram of monitor block, retraction block, and the AN8420VCM

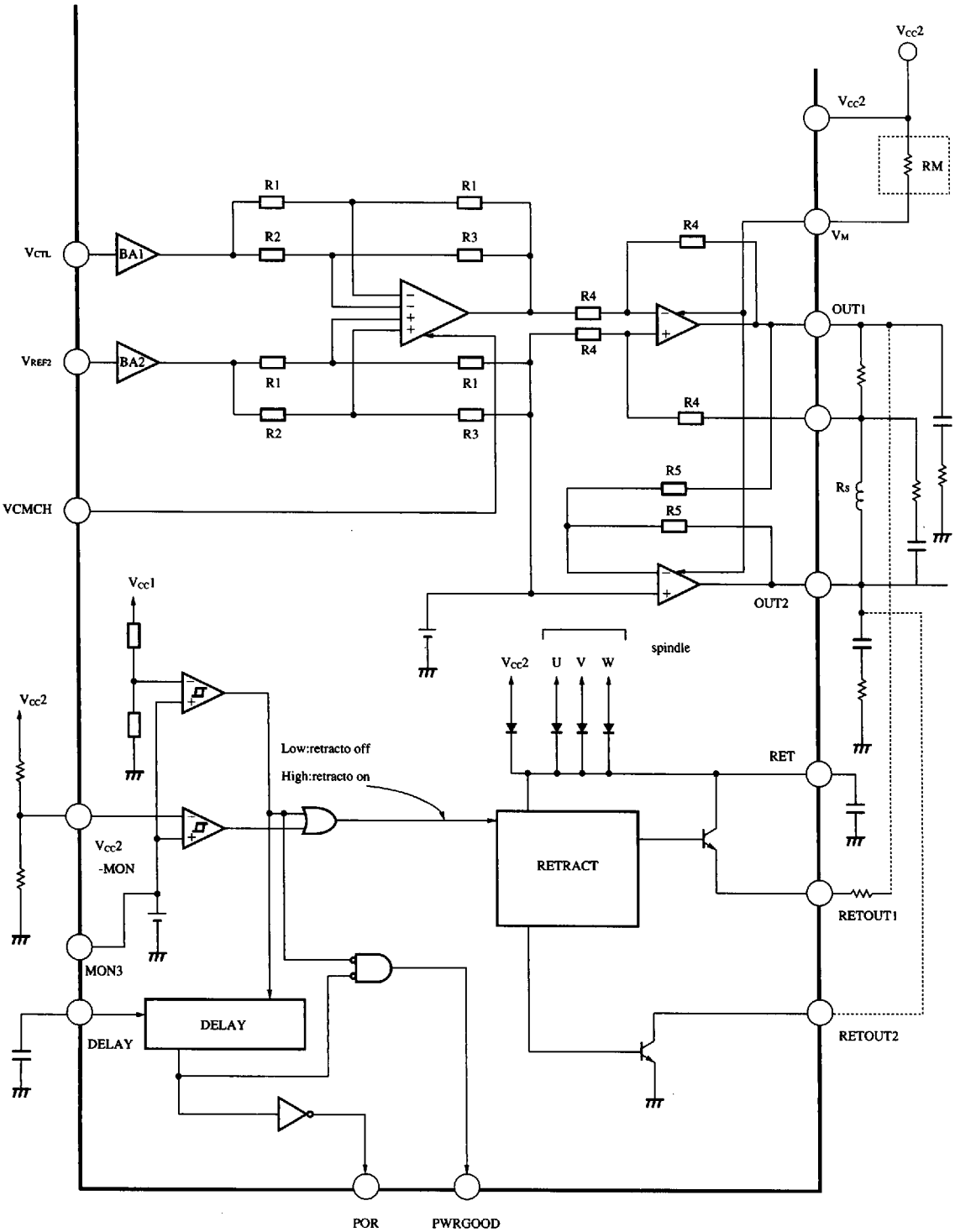


Fig.7

• Voltage monitor and retraction function

(10) Voltage monitor

By the voltage monitor function, $V_{CC}1$ and $V_{CC}2$ can be monitored.

The monitor function for $V_{CC}1$ which is built in the IC is related to the DELAY, PWRGOOD, POR and RETRACT functions.

The following shows the threshold level set by $V_{CC}1$ monitor :

($V_{CC}1$: L→H) V_{HDV}=4.40 (V) (typ)

($V_{CC}1$: H→L) V_{LDV}=4.25 (V) (typ)

The monitor function for $V_{CC}2$ which is set with external resistance is related to PWRGOOD, POR and RETRACT functions.

The following calculation gives the threshold level set by $V_{CC}2$ monitor :

$$V_{CC}2=\frac{R1+R2}{R1}\ V_{MON3}\quad (V_{CC}2 : L\rightarrow H)$$

$$V_{CC}2=\frac{R1+R2}{R1}\ (V_{MON3}-V\text{Hysteresis width})\quad (V_{CC}2 : H\rightarrow L)$$

V_{MON3}=1.2V (typ)
VHysteresis width=47.5mV (typ)

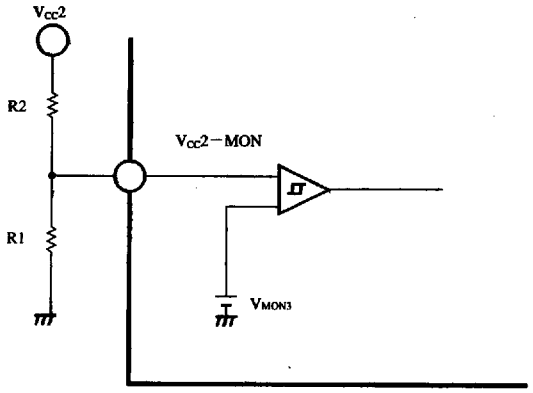


Fig.8

The following shows the image illustration of DELAY, PWRGOOD and POR by the voltage of $V_{CC}1$ and $V_{CC}2$.

(Ex. 1)

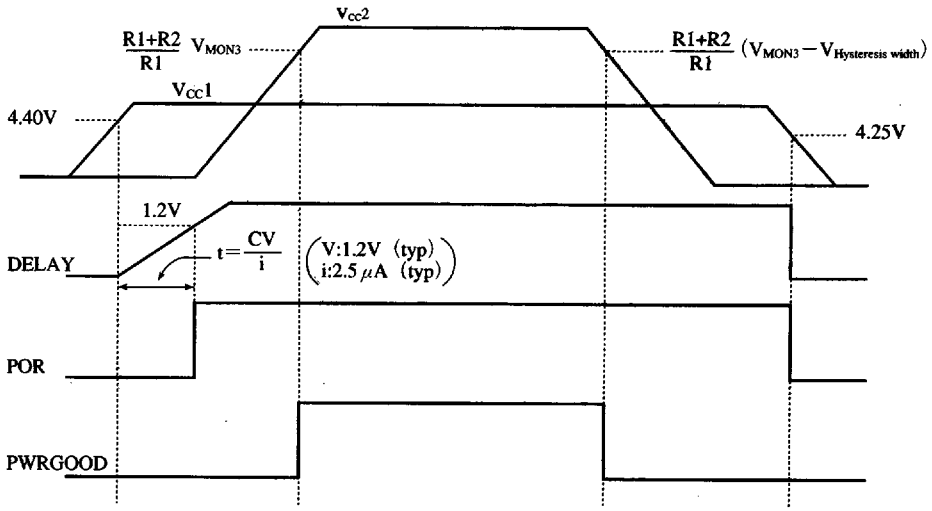


Fig.9

(Ex. 2)

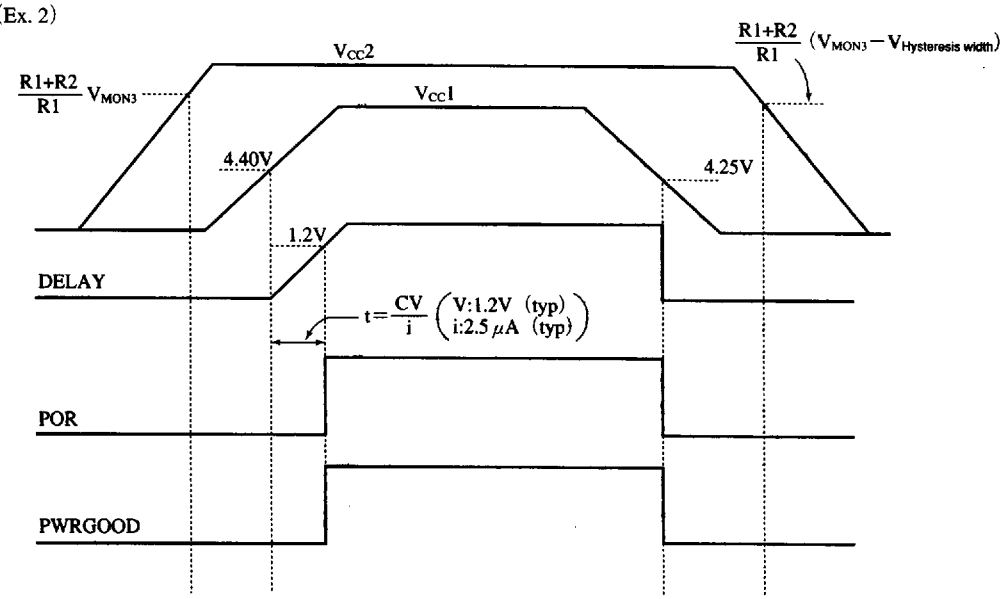

R1+R2 / R1 (V_MON3 − V_Hysteresis width)
Vcc2
R1+R2 / R1 V_MON3
Vcc1
4.40V
4.25V
1.2V
DELAY
t=CV/i (V:1.2V (typ) i:2.5μA (typ))
POR
PWRGOOD

Fig.10

• Retraction function

The AN8420FBP has the forced retraction function at power-on and the retraction function at power-off.

The retraction function at power-on uses the power supply of VCC2 and the back electromotive force of spindle motor. When "High" signal is applied to the forced retraction terminal, CRET, the retraction circuit starts operation. On the other hand, when "Low" signal is applied to it, the retraction circuit does not start operation.

The retraction function at power-off uses the back electromotive force of the motor.

In addition, the retraction current flows from the RETOUT1 terminal to the RETOUT2 terminal.

(Ex. 1) Image illustration of the terminal voltage at retraction

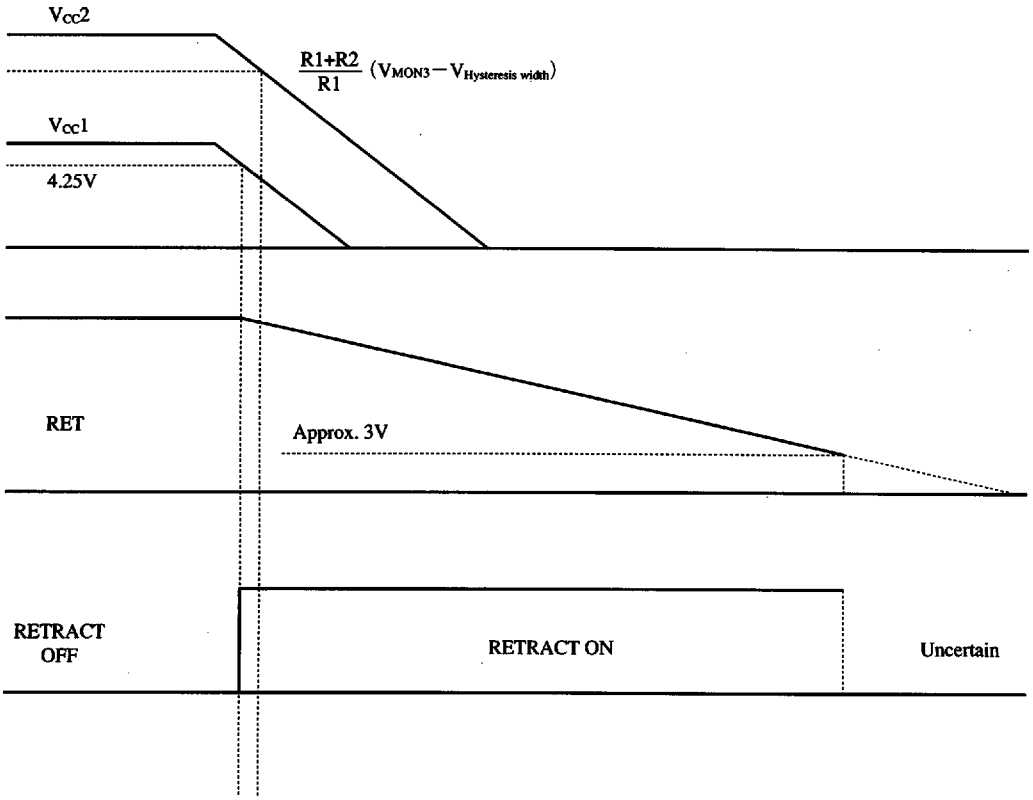


Fig.11

(Ex. 2)

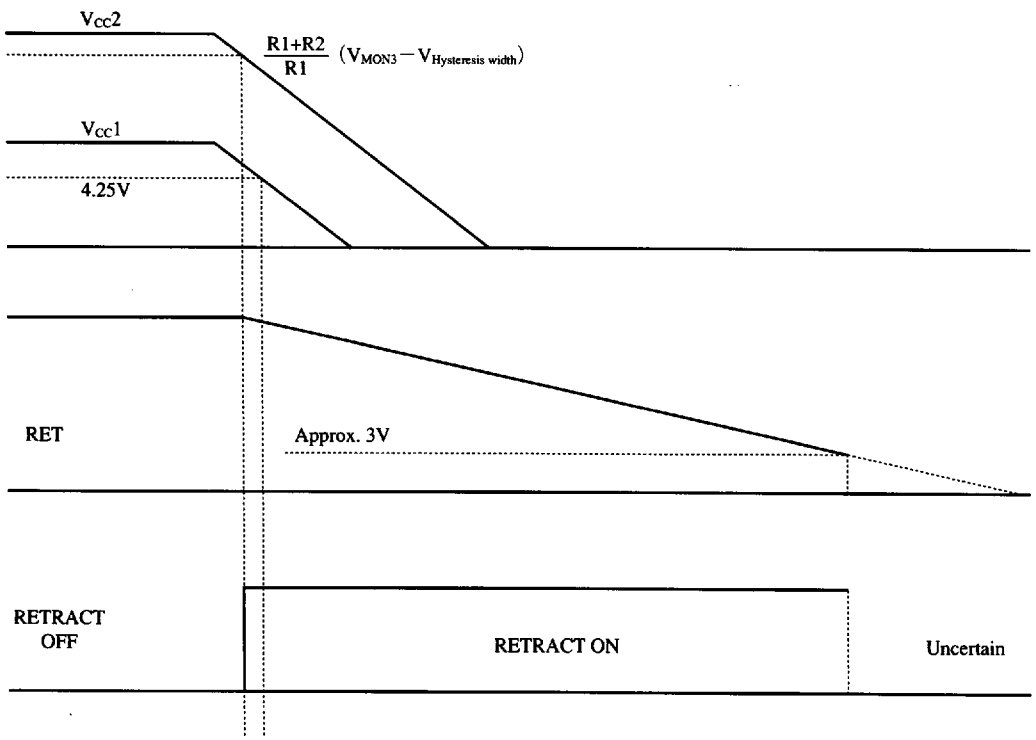


Fig.12

(Ex. 3)

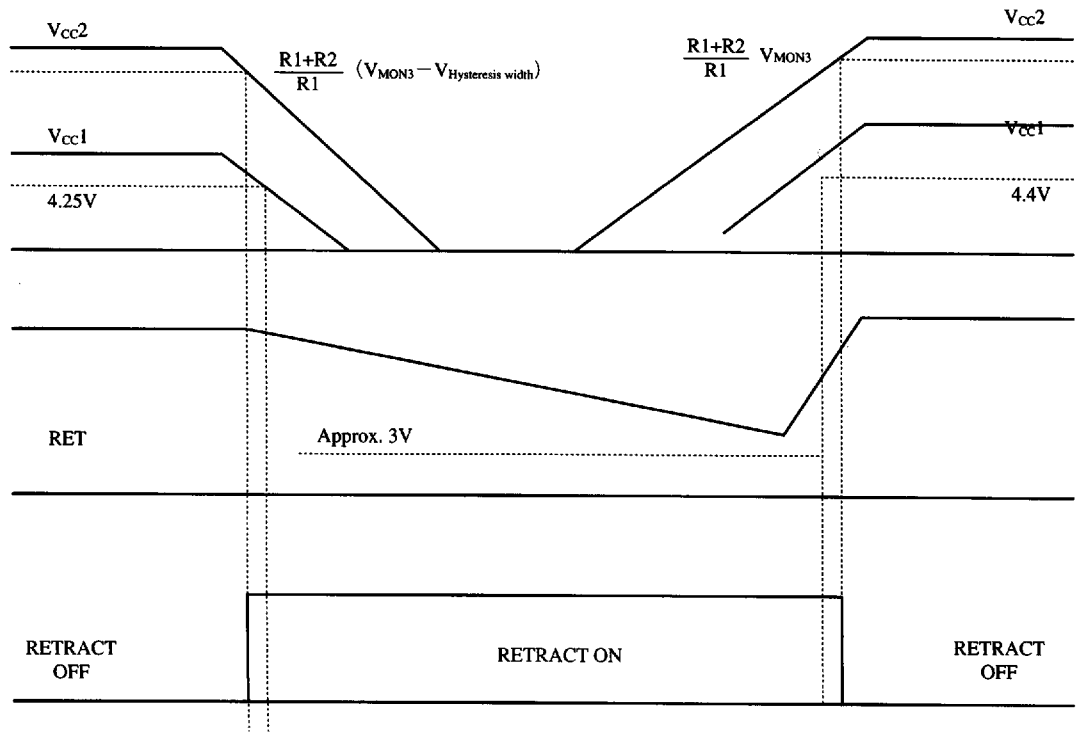


Fig.13