AN8130FBP

High Speed Low Power Consumption Bi-CMOS 10-Bit A/D Convertor

■ Overview

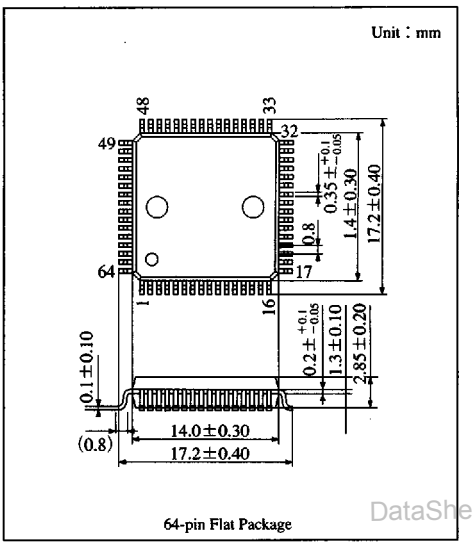
The AN830FBP is a 10-bit A/D convertor for image processing which employs the bi-CMOS process to realize the low consumption power.

■ Features

- 10-bit resolution
- Maximum conversion rate : 20 MSPS (min.)
- Sample holding circuit not required
- Low consumption power : 750 mW (typ.)
- S/H circuit built-in
- 2-step parallel type

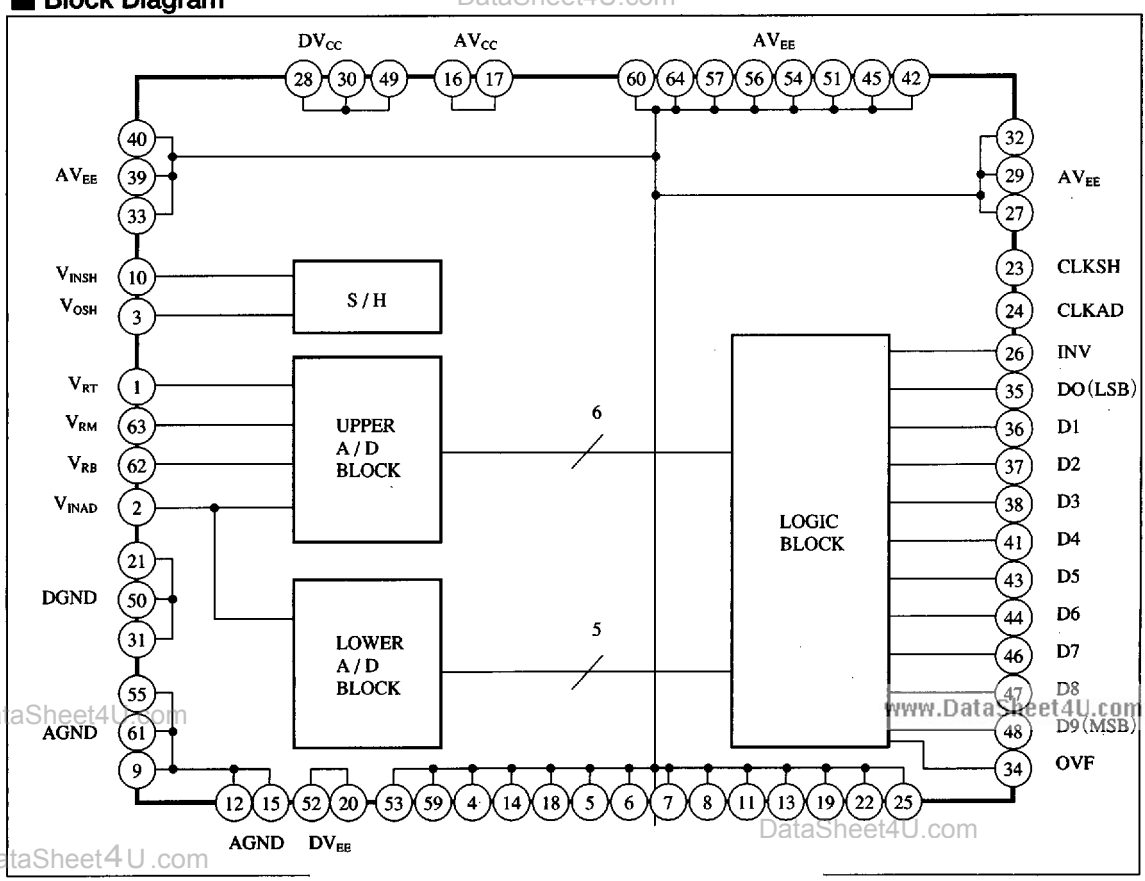
■ Application Field

- Digital video broadcasting such as D-STB
- Image equipment such as hi-vision device
- OA equipment such as image scanner
- Measuring equipment such as digital oscilloscope



64-pin Flat Package

■ Block Diagram



■ Major Characteristics (V_{CC}=5V, V_{EE}=−5V, Ta=25℃)

Parameter	Condition	Rating	Unit
Resolution		10	Bit
Input dynamic range		2	V_{P-P}
Linearity error	V_{IN}=2V_{P-P}	±1	LSB
Differential linearity error		±0.5	LSB
Maximum conversion rate		20	MSPS
Quantization noise (S/N)	f_{CLK}=20MHz, f_I=1MHz	52	dB
	f_{CLK}=20MHz, f_I=8MHz	47	dB
Differential gain (DG))	IRE standard 15kHz Sawtooth 40% subcarrier f_{CLK}=20MHz, Nolock	0.5	%
Differential phase (DP)		0.5	deg
Input band (BW)	V_{IN}=2V_{P-P}	10	MHz

■ Absolute Maximum Rating (Ta=25℃)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{EE}	−6 to +0.5	V
	V_{CC}	−0.5 to +6	V
Analogue input voltage	V_{IN}	V_{EE} to V_{CC}	V
Digital input voltage	V_{CLKSH}/V_{CLKAD}	−0.5 to V_{CC}+0.5	V
Digital output current	IOVF, ID0 to ID9	−15	mA
Reference voltage	V_{RB}/V_{RT}	V_{EE} to +0.5	V
Power dissipation*	P_D	1137	mW
Operating ambient temperature	T_{opr}	−20 to +70	℃
Storage temperature	T_{stg}	−55 to +150	℃

* Ta=70℃

■ Recommended Operating Conditions (Ta=25℃)

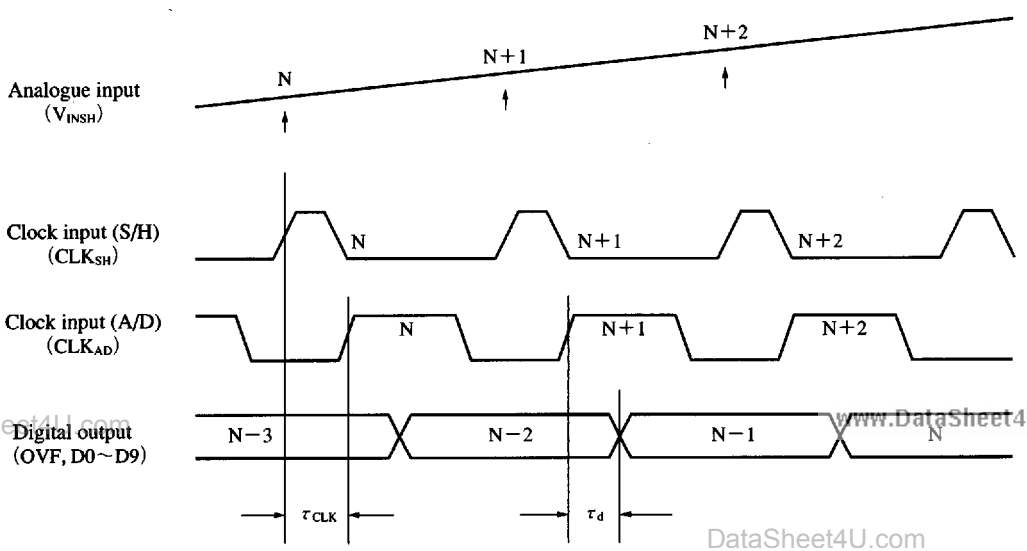
Parameter	Symbol	min	typ	max	Unit
Positive supply voltage	V_{CC}	4.75	5	5.25	V
Negative supply voltage	V_{EE}	−5.25	−5	−4.75	V
Reference voltage	V_{RT}	—	0	—	V
	V_{RB}	—	−2	—	V
Analogue input voltage	V_{IN}	V_{RB}	—	V_{RT}	V
Digital input voltage	V_{IH}	2	—	4	V
	V_{IL}	0	—	0.8	V
Digital output current	I_{OH}	—	−0.4	—	mA
	I_{OL}	—	1.6	—	mA
S/H clock input pulse width*	t_H	15	20	—	ns
A/D clock input pulse width *	t_H	35	40	—	ns

* f_{CLK}=16MHz

■ Electrical Characteristics (V_{CC}=5V, V_{EE}=−5V, Ta=25℃)

Parameter	Symbol	Condition	min	typ	max	Unit
Supply current	DI_{CC}		—	5	10	mA
	AI_{CC}		—	14	28	mA
	I_{EE}		−164	131	—	mA
Reference resistive current	I_{RT}	V_{RT}=0V	2.4	3	3.6	mA
	I_{RB}	V_{RB}=−2V	−3.6	−3	−2.4	mA
Input bias current	I_{IN}	V_{INSH}=−1V	—	10	100	μA
Clock input current	I_{IH}	V_{CLKAD}=V_{CLKSH}=2.7V	—	1	8	μA
	I_{IL}	V_{CLKAD}=V_{CLKSH}=0.4V	—	1	8	μA
Digital output voltage	V_{OH}	I_{OH}=−400μA	2.7	3.4	—	V
	V_{OL}	I_{OL}=1.6mA	—	—	0.4	V
Linearity error	E_L	V_{IN}=$2V_{p-p}$	—	±1	—	LSB
Differential linearity error	E_D	V_{IN}=$2V_{p-p}$	—	±0.5	±1	LSB
Maximum conversion rate	F_{CMAX}	V_{IN}=$2V_{p-p}$	20	—	—	MSPS
Quantization noise	S/N	f_{CLK}=16MHz, f_{IN}=1MHz	—	53	—	dB
		f_{CLK}=16MHz, f_{IN}=8MHz	—	49	—	dB
		f_{CLK}=20MHz, f_{IN}=1MHz	—	52	—	dB
		f_{CLK}=20MHz, f_{IN}=8MHz	—	47	—	dB
Differential gain	DG	IREstandard 15kHz Sawtooth 40% subcarrier f_{CLK}=20MHz, Nolock	—	0.5	1	%
Differential phase	DP		—	0.5	1	deg
Digital output delay	τ_d		—	33	—	ns
Clock delay	τ_{CLK}	f_{CLK}=16MHz	−5	0	5	ns
Input capacitance	C_{IN}		—	10	—	pF
Input offset voltage	V_{OFS}		—	0	—	V

■ Timing Chart



Output Code

Step	Input signal 2.000VFS 1.953mV STEP	Digital output M L OVF 9876543210
	$\overline{INV}$ = "H"	
000	−0.000000	0 0000000000
001	−0.001953	0 0000000001
.	.	.
.	.	.
.	.	.
511	−0.998047	0 0111111111
512	−1.000000	0 1000000000
513	−1.001953	0 1000000001
.	.	.
.	.	.
.	.	.
1023	−1.998047	0 1111111111
1024	−2.000000	1 1111111111

Pin Descriptions

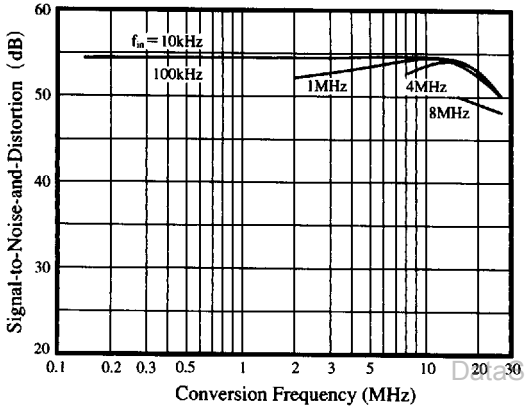
Pin No.	Symbol	Pin name	Standard waveform	Voltage level	Description
16, 17	AV_{CC}	Analogue positive power supply pin		5V	It is a power supply pin for analogue signal. Connect tantalum capacitor of several μF and ceramic capacitor of 0.1 μF as near as possible to this pin between this pin and AGND.
4, 5, 6 7, 8, 11 13, 14, 18 19, 22, 25 27, 29, 32 33, 39, 40 42, 45, 51 53, 54, 56 57, 59, 60 64	AV_{EE}	Analogue negative power supply pin		−5V	
28, 30 49	DV_{CC}	Digital positive power supply pin		5V	It is a power supply pin for digital circuit block. Connect tantalum capacitor of several μF and ceramic capacitor of 0.1 μF as near as possible to this pin between this pin and DGND.
20, 52	DV_{EE}	digital negative power supply pin		−5V	
9, 12 15, 55 61	AGND	analogue ground pin		0V	Connect the analogue ground and digital ground with the possible lowest impedance at one point as near as possible to the chip. Inserting ferrite fuse between above two grounds and connecting the AGND with the ground for power supply may decrease the noise.
21, 31 50	DGND	Digital ground pin		0V	

■ Pin Descriptions (cont.)

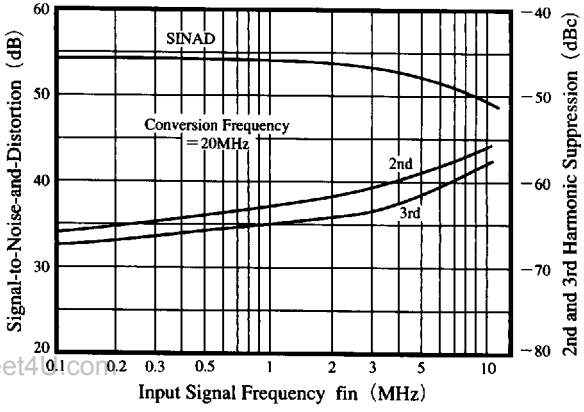
Pin No.	Symbol	Pin name	Standard waveform	Voltage level	Description
62	V_{RB}	Reference voltage low level		−2V	It is used to set the reference voltage of comparator. Normally, V_{RT} is given 0 V and V_{RB} is given -2 V. Connect tantalum capacitor of several μF and ceramic capacitor of 0.1 μF in parallel between each pin and analogue ground. V_{RM} is provided for linearity compensation which gives middle point potential. However, it is normally opened.
63	V_{RM}	Reference voltage middle point level		−1V	
1	V_{RT}	Reference voltage high level		0V	
26	INV	Digital output invert pin		TTL	Setting the INV pin to "L" level invert all the outputs (D0 - D9) but not the overflow output. This pin is set to "L" level with no connection and operates a synchronously with clock.
34	OVF	Overflow output		TTL	When overflow occurs, it becomes "H" level. This output is not affected by the INV pin
10	VIN_{SH}	Analogue input (S/H)		0~−2V	It is an input pin of analogue signal for sample holding circuit. Input capacitance is about 10 pF. However, in order to obtain good frequency characteristics, drive it by using a buffer with the possible largest driving capacity. The resistor of about 150 Ω should be inserted between this pin and AGND pin to make the frequency characteristics flat.
3	VO_{SH}	Analogue input (A/D)		0~−2V	It is an output for sample holding circuit.
2	VIN_{AD}	Analogue input (A/D)		0~−2V	It is an input pin of analogue signal for A/D conversion circuit. Normally, the sample holding output VO_{SH} is directly connected with it. When ringing is large, connect the inductor of about 0.3 μH and the resistor of about 150 Ω in series with it.
23 24	CLK_{SH} CLK_{AD}	Clock input (S/H), Clock input (A/D)	Refer to the timing chart.	TTL	It is a clock for A/D and S/H circuits. For their timing, refer to the attached sheet. Input the data of small jitter at TTL level. Take care to suppress the ringing, particularly overshoot. When CMOS is used, the high level should set 3.5 V or lower by resistive divider.
35 36 37 38 41 43 44 46 47 48	D0 D1 D2 D3 D4 D5 D6 D7 D8 D9	Digital output (LSB) Digital output Digital output Digital output Digital output Digital output Digital output Digital output Digital output Digital output (MSB)	Refer to the timing chart.	TTL	It is an output pin for the TTL level. In order to prevent the digital noise to entering into the analogue circuit, suppress the ringing as far as possible. It is effective to insert the ferrite beads or resistor of about 220 Ω between each pin and the input pin for IC of logic which receives it.
58	NC				Open it for use.

Characteristic Curve

Conversion Frequency and SINAD



Input Signal Frequency and SINAD/Distortion
(Conversion Frequency = 20 MHz)



Input Signal Frequency and SNR/DNL
(Conversion Frequency = 20MHz)