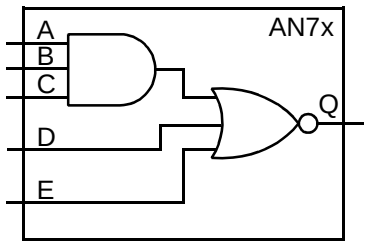
Description

AN7x is a family of AND-NOR circuits consisting of one 3-input AND gate into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
H	H	H	X	X	L
X	X	X	H	X	L
X	X	X	X	H	L
All other combinations					H

HDL Syntax

Verilog ..... AN7x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: AN7x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads		
	AN72	AN74	AN76
A	1.0	1.0	2.1
B	1.0	1.0	2.1
C	1.0	1.0	2.1
D	1.0	1.0	2.1
E	1.0	1.0	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN72	5.0	TBD	9.9
AN74	5.0	TBD	9.2
AN76	10.0	TBD	16.8

a. See page 2-15 for power equation.

AMI5HG 0.5 micron CMOS Gate Array

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

AN72	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.47 0.50	0.58 0.62	0.71 0.75	0.86 0.90	0.97 1.01
AN74	**Number of Equivalent Loads**		**1**	**8**	**15**	**22**	**30 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.41 0.50	0.54 0.62	0.65 0.73	0.74 0.84	0.84 0.96
AN76	**Number of Equivalent Loads**		**1**	**14**	**28**	**42**	**56 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.37 0.49	0.49 0.60	0.60 0.70	0.70 0.80	0.79 0.92

Delay will vary with input conditions. See page 2-17 for interconnect estimates.